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DOCUMENT CONTROL ADMINISTRATOR

FLUKE

HYDRA

2620A DATA ACQUISITION UNIT
2625A DATA LOGGER
2635A DATA BUCKET

Service Manual

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CAUTION

THIS IA AN IEC SAFETY CLASS 1 PRODUCT. BEFORE USING, THE GROUND WIRE IN THE LINE CORD OR THE REAR PANEL BINDING POST MUST BE CONNECTED FOR SAFETY.

INTERFERENCE INFORMATION

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept interference received, including interference that may cause undesired operation.

Declaration of the Manufacturer or Importer

We hereby certify that Fluke Models 2625A Data Logger, 2620A Data Acquisition Unit and 2635A Data Bucket are in compliance with the requirements of BMPT Vfg 243/1991 RFI suppressed. The normal operation of some equipment (e.g. signal generators) may be subject to specific restrictions. Please observe the notices in the users manual. The marketing and sale of the equipment was reported to the Central Office of Telecommunications Permits (BZT). The right to retest this equipment to verify compliance with the regulation was given to the BZT.

Bescheinigung des Hersteller/Importeurs

Hiermit wird bescheinigt, daß Fluke Models 2625A Data Logger, 2620A Data Acquisition Unit und 2635A Data Bucket in Übereinstimmung mit den Bestimmungen der BMPT-AmtsblVfg 243/1991 funk-entsört sind. Der vorschriftsmäßige Betrieb mancher Geräte (z.B. Meßsender) kann allerdings gewissen Einschränkungen unterliegen. Beachten Sie deshalb die Hinweise in der Bedienungsanleitung. Dem Bundesamt für Zulassungen in der Telekommunikation wurde das Inverkehrbringen dieses Gerätes angezeigt und die Berechtigung zur Überprüfung der Serie auf die Einhaltung der Bestimmungen eingeräumt.

Fluke Corporation

SAFETY TERMS IN THIS MANUAL

This instrument has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Electrical Measuring, Control and Laboratory Equipment. This User Manual contains information, warnings, and cautions that must be followed to ensure safe operation and to maintain the instrument in a safe condition. Use of this equipment in a manner not specified herein may impair the protection provided by the equipment.

The meter is designed for IEC 664, Installation Category II use. It is not designed for use in circuits rated over 4800VA.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

CAUTION statements identify conditions or practices that could result in damage to equipment.

SYMBOLS MARKED ON EQUIPMENT

⚡	DANGER – High voltage.
⏚	Ground (earth) terminal.
⏚	Protective ground (earth) terminal. Must be connected to safety earth ground when the power cord is not used.See Section 2.
⚠	Attention – refer to the manual. This symbol indicates that information about usage of a feature is contained in the manual. This symbol appears in the following two places on the instrument rear panel:

1. Ground Binding Post (left of line power connector). Refer to 'Using External DC Power' in Section 2.
2. Alarm Outputs/Digital I/O Connectors. Refer to Appendix A, Specifications.

AC POWER SOURCE

The instrument is intended to operate from an ac power source that will not apply more than 264V ac rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is required for safe operation.

DC POWER SOURCE

The instrument may also be operated from a 9 to 16V dc power source when either the rear panel ground binding post or the power cord grounding conductor is properly connected.

USE THE PROPER FUSE

To avoid fire hazard, use only a fuse identical in type, voltage rating, and current rating as specified on the rear panel fuse rating label.

GROUNDING THE INSTRUMENT

The instrument utilizes controlled overvoltage techniques that require the instrument to be grounded whenever normal mode or common mode ac voltages or transient voltages may occur. The enclosure must be grounded through the grounding conductor of the power cord, or if operated on battery with the power cord unplugged, through the rear panel ground binding post.

USE THE PROPER POWER CORD

Use only the power cord and connector appropriate for the voltage and plug configuration in your country.

Use only a power cord that is in good condition.

Refer cord and connector changes to qualified service personnel.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate the instrument in an atmosphere of explosive gas.

DO NOT REMOVE COVER

To avoid personal injury or death, do not remove the instrument cover. Do not operate the instrument without the cover properly installed. Normal calibration is accomplished with the cover closed, and there are no user-serviceable parts inside the instrument, so there is no need for the operator to ever remove the cover. Access procedures and the warnings for such procedures are contained in the Service Manual. Service procedures are for qualified service personnel only.

DO NOT ATTEMPT TO OPERATE IF PROTECTION MAY BE IMPAIRED

If the instrument appears damaged or operates abnormally, protection may be impaired. Do not attempt to operate it. When in doubt, have the instrument serviced.

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Section 1

Introduction and Specifications

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INTRODUCTION 1-1.

Hydra measures analog inputs of dc and ac volts, thermocouple and RTD temperatures, resistance, and frequency. It features 21 measurement input channels. In addition, it contains eight digital input/output lines, one totalizing input, one external scan trigger input, and four alarm output lines. Hydra is fully portable and can be ac or dc powered. An RS-232 computer interface is standard. An optional IEEE-488 computer interface is available for the Hydra Data Acquisition Unit (2620A) only.

The Hydra Data Logger (2625A) adds substantial measurement memory capabilities. The RS-232 computer interface is standard, but IEEE-488 capability is not available for the Hydra Data Logger.

The Hydra Data Bucket (2635A) adds more flexible storage for instrument setups and measurement data by adding a PCMCIA memory card and interface. The amount of storage can be easily changed by selecting a memory card of the appropriate size for the job.

The Hydra instruments share many features and functions. The term “instrument” is used to refer to all three instruments. The model number (2620A, 2625A, or 2635A) is used when discussing features unique to one instrument.

The instrument is designed for bench-top, field service, and system applications. A dual vacuum-fluorescent display uses combinations of alphanumeric characters and descriptive annunciators to provide prompting and measurement information during setup and operation modes.

Some features provided by the instrument are listed in Table 1-1.

OPTIONS AND ACCESSORIES 1-2.

The following items can be installed either at the factory or in the field:

- Option 2620A-05K (IEEE-488 Interface Kit) consists of a printed circuit assembly, connecting cable, and mounting hardware. This field-installable kit gives the 2620A Hydra Data Acquisition Unit IEEE-488 interface capabilities. IEEE-488 computer interface commands are virtually identical to RS-232 interface commands. (The 2625A and 2635A cannot be equipped with an IEEE-488 Interface.)
- Accessory 2620A-100 (Connector Kit).

The instrument can be mounted in a standard 19-inch rack panel on either the right-hand or left-hand side using the Fluke M00-200-634 Rackmount Kit.

Accessories are listed in Table 1-2.

OPERATING INSTRUCTIONS 1-3.

Full operating instructions are provided in the Hydra User Manual (2620A or 2625A) and in the Hydra Data Bucket User Manual (2635A). Refer to the User Manual as necessary during the maintenance and repair procedures presented in this Service Manual.

ORGANIZATION OF THE SERVICE MANUAL 1-4.

This manual focuses on performance tests, calibration procedures, and component-level repair of each of the instruments. To that end, manual sections are often interdependent; effective troubleshooting of the 2620A or 2625A may require not only reference to the troubleshooting procedures in Section 5, but also some understanding of the detailed Theory of Operation in Section 2 and some tracing of circuit operation in the Schematic Diagrams presented in Section 8. For the 2635A, effective troubleshooting may require not only reference to the troubleshooting procedures in Section 5A, but also some understanding of the detailed Theory of Operation in Section 2A and some tracing of circuit operation in the Schematic Diagrams presented in Section 8.

Often, scanning the table of contents will yield an appropriate place to start using the manual. A comprehensive table of contents is presented at the front of the manual; local tables of contents are also presented at the beginning of each section for ease of reference. If you know the topic name, the index at the end of the manual is probably a good place to start.

The following section descriptions serve to introduce the manual:

SECTION 1. INTRODUCTION AND SPECIFICATIONS

Introduces the instrument, describing its features, options, and accessories. This section also discusses use of the Service Manual and the various conventions used in describing the circuitry. Finally, a complete set of specifications is presented.

SECTION 2. THEORY OF OPERATION (2620A and 2625A)

This section first categorizes these instrument's circuitry into functional blocks, with a description of each block's role in overall operation. A detailed circuit description is then given for each block. These descriptions explore operation to the component level and fully support troubleshooting procedures defined in Section 5.

SECTION 2A. THEORY OF OPERATION (2635A)

This section first categorizes the instrument's circuitry into functional blocks, with a description of each block's role in overall operation. A detailed circuit description is then given for each block. These descriptions explore operation to the component level and fully support troubleshooting procedures defined in Section 5A.

SECTION 3. GENERAL MAINTENANCE

Provides maintenance information covering handling, cleaning, and fuse replacement. Access and reassembly procedures are also explained in this section.

SECTION 4. PERFORMANCE TESTING AND CALIBRATION

This section provides performance verification procedures, which relate to the specifications presented in Section 1. To maintain these specifications, a full calibration procedure is also presented.

SECTION 5. DIAGNOSTIC TESTING AND TROUBLESHOOTING (2620A and 2625A)

The troubleshooting procedures presented in this section rely closely on both the Theory of Operation presented in Section 2, the Schematic Diagrams shown in Section 8, and the access information provided in Section 3.

SECTION 5A. DIAGNOSTIC TESTING AND TROUBLESHOOTING (2635A)

The troubleshooting procedures presented in this section rely closely on both the Theory of Operation presented in Section 2A, the Schematic Diagrams shown in Section 8, and the access information provided in Section 3.

SECTION 6. LIST OF REPLACEABLE PARTS

Includes parts lists for all standard assemblies. Information on how and where to order parts is also provided.

SECTION 7. IEEE-488 OPTION (2620A only)

This section describes the IEEE-488 option. Included are specifications, theory of operation, maintenance, and a list of replaceable parts. Schematic diagrams for this option are included at the end of the overall Service Manual (Section 8).

SECTION 8. SCHEMATIC DIAGRAMS

Includes schematic diagrams for all standard and optional assemblies. A list of mnemonic definitions is also included to aid in identifying signal name abbreviations.

CONVENTIONS 1-5.

Throughout the manual set, certain notational conventions are used. A summary of these conventions follows:

- Instrument Reference

  The Hydra Data Acquisition Unit (Model 2620A), the Hydra Data Logger (Model 2625A), and the Hydra Data Bucket (Model 2635A) share many features and functions. The term Hydra refers to any of these instruments. The model number (e.g., 2620A, 2625A, or 2635A) is used when features unique to one instrument are being described.

- Printed Circuit Assembly

  The term "pca" is used to represent a printed circuit board and its attached parts.

- Signal Logic Polarity

  On schematic diagrams, a signal name followed by a "*" is active (or asserted) low. Signals not so marked are active high.

- Circuit Nodes

  Individual pins or connections on a component are specified with a dash (-) following the assembly and component reference designators. For example, pin 19 of U30 on assembly A1 would be A1U30-19.

- User Notation

  For front panel operation,

  XXX An uppercase word or symbol without parentheses indicates a button to be pressed by the user. Buttons can be pressed in four ways:

  1. Press a single button to select a function or operation.
  2. Press a combination of buttons, one after the other.
  3. Press and hold down a button, then press another button.
  4. Press multiple buttons simultaneously.

For computer interface operation,

XXX	An uppercase word without parentheses identifies a command by name.
<XXX>	Angle brackets around all uppercase letters mean press the <XXX> key.
(xxx)	When associated with a keyword, a lowercase word in parentheses indicates an input required by the user.

Table 1-1. Hydra Features

- Channel Scanning

  Can be continuous scanning, scanning at an interval time, single scans, or triggered (internal or external) scans.
- Channel Monitoring

  Make measurements on a single channel and view these measurements on the display.
- Channel Scanning and Monitoring

  View measurements made for the monitor channel while scanning of all active channels continues.
- Multi-Function Display

  Left (numeric) display shows measurement readings; also used when setting numeric parameters.

  Right (alphanumeric) display used for numeric entries, channel number selection and display, status information, and operator prompts.
- Front-Panel Operation

  Almost all operations can be readily controlled with the buttons on the front panel.
- Measurement Input Function and Range

  Volts dc (VDC), volts ac (VAC), frequency (Hz), and resistance (Ω) inputs can be specified in a fixed measurement range. Autoranging, which allows the instrument to use the measurement range providing the optimum resolution, can also be selected.
- Temperature Measurement

  Thermocouple types J, K, E, T, N, R, S, B, and Hoskins Engineering Co. type C are supported. Also, DIN/IEC 751 (Pt 385) Platinum RTDs are supported.
- Totalize Events on the Totalizing Input
- Alarms Limits and Digital Output Alarm Indication
- 4-Terminal Resistance Measurements (Ch. 1 .. 10)
- RS-232 Computer Interface Operation
- Measurement Rate Selection
- Nonvolatile Memory

  Storage of minimum, maximum, and most recent measurements for all scanned channels.

  Storage of Computer Interface setup, channel configurations, and calibration values.
- Features unique to the 2625A Data Logger.

  Storage of measurement data: storage for 2047 scans of up to 21 channels, representing up to 42,987 readings.
- Features unique to the 2635A Data Bucket.

  Internal storage of measurement data for 100 scans of up to 21 channels, representing up to 2,100 readings.

  Memory card storage of instrument setup configurations so that instrument may be quickly set up to do different tasks.

  Memory card storage of measurement data for up to 4,800 scans of 10 channels on a 256K-byte card or up to 19,800 scans of 10 channels on a 1M-byte memory card.

  Enhanced RS-232 interface with higher baud rates and hardware flow control using the Clear to Send modem control signal.

Table 1-2. Accessories

MODEL	DESCRIPTION
80i-410 80i-1010	Clamp-On DC/AC Current Probes
80J-10	Current Shunt
2620A-05K	Field-installable IEEE-488 Option kit (Hydra Data Acquisition Unit only.)
2620A-100	Extra I/O Connector Set: Includes Universal Input Module, Digital I/O and Alarm Output Connectors.
262XA-801	Diconix(R) 80-column serial printer.
263XA-803	Memory Card Reader for IBM-PC or compatible personal computer. Card reader is external to the PC and connects to a PC parallel port (LPT1, LPT2, etc.). (2635A Data Bucket only).
263XA-804	256K-Byte Memory Card (2635A Data Bucket only). (This card is supplied with the instrument.)
263XA-805	1M-Byte Memory Card (2635A Data Bucket only).
26XXA-901	Hydra Logger Applications Package (Version 3.0)
C40	Soft carrying case. Provides padded protection for the instrument. Includes a pocket for the manual and pouch for the line cord.
M00-200-634	Rackmount Kit. Provides standard 19-inch rack mounting for one instrument (right or left side.)
PM 8922	Switchable X1, X10 passive probe.
RS40	Shielded RS-232 terminal interface cable. Connects the instrument to any terminal or printer with properly configured DTE connector (DB-25 socket), including an IBM PC(R), IBM PC/XT(R) or IBM PS/2 (models 25, 30, 50, P60, 70, and 80).
RS41	Shielded RS-232 modem cable. Connects the instrument to a modem with properly configured DB-25 male pin connector. Use an RS40 and an RS41 cable in series to connect with an IBM PC/AT(R).
RS42	Shielded serial printer cable. Contact Fluke for list of compatible printers.
TL20	Industrial test lead set.
TL70A	Test lead set (one set is supplied with the instrument).
Y8021	Shielded IEEE-488 one-meter (39.4 inches) cable, with plug and jack at each end.
Y8022	Shielded IEEE-488 two-meter (78.8 inches) cable, with plug and jack at each end.
Y8023	Shielded IEEE-488 four-meter (13 feet) cable, with plug and jack at each end.
Y9109	Binding post to BNC plug.

Footnote:
IBM PC, IBM PC/XT, and IBM PC/AT are registered trademarks of International Business Machines

SPECIFICATIONS

1-6.

Table 1-3 contains the specifications for the 2620A and 2625A.

Table 1-4 contains the specifications for the 2635A.

Table 1-3. 2620A/2625A Specifications

The instrument specifications presented here are applicable within the conditions listed in the Environmental portion of this specification.

The specifications state total instrument accuracy following calibration, including:

- A/D errors
- Linearization conformity
- Initial calibration errors
- Isothermality errors
- Relay thermal emf's
- Reference junction conformity
- Temperature coefficients
- Humidity errors

Sensor inaccuracies are not included in the accuracy figures.

Accuracies at Ambient Temperatures Other Than Specified

To determine typical accuracies at temperatures intermediate to those listed in the specification tables, linearly interpolate between the applicable 0°C to 60°C and 18°C to 28°C accuracy specifications.

Response Times

Refer to Typical Scanning Rate and Maximum Autoranging Time later in this table.

DC VOLTAGE INPUTS

	Resolution	
Range	**Slow**	**Fast**
300 mV	10 µV	0.1 mV
3V	0.1 mV	1 mV
30V	1 mV	10 mV
300V	10 mV	0.1V

Range	Accuracy ±(% ± V)				
	18°C to 28°C			0°C to 60°C	
	90 Days, Slow	1 Year, Slow	1 Year, Fast	1 Year, Slow	1 Year, Fast
300 mV	0.026%+20 µV	0.031%+20 µV	0.047%+0.2 mV	0.070%+20 µV	0.087%+0.2 mV
3V	0.028%+0.2 mV	0.033%+0.2 mV	0.050%+2 mV	0.072%+0.2 mV	0.089%+2 mV
30V	0.024%+2 mV	0.029%+2 mV	0.046%+20 mV	0.090%+2 mV	0.107%+20 mV
300V	0.023%+20 mV	0.028%+20 mV	0.045%+0.2V	0.090%+20 mV	0.107%+0.2V

Input Impedance

100 MΩ minimum in parallel with 150 pF maximum for all ranges 3V and below
10 MΩ in parallel with 100 pF maximum for the 30V and 300V ranges

Normal Mode Rejection

53 dB minimum at 60 Hz ±0.1%, slow rate
47 dB minimum at 50 Hz ±0.1%, slow rate

Common Mode Rejection

120 dB minimum at dc, 1 kΩ imbalance, slow rate
120 dB minimum at 50 or 60 Hz ±0.1%, 1 kΩ imbalance, slow rate

Maximum Input

300V dc or ac rms on any range for channels 0, 1, and 11
150V dc or ac rms for channels 2 to 10 and 12 to 20
Voltage ratings between channels must not be exceeded

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of this table.

Table 1-3. 2620A/2625A Specifications (cont)

THERMOCOUPLE INPUTS

Thermocouple		Accuracy (±°C)*				
		18°C to 28°C			0°C to 60°C	
Type	Temperature (°C)	90 Days Slow	1 Year Slow	1 Year Fast	1 Year Slow	1 Year Fast
J	-100.00	0.49	0.53	1.00	0.73	1.22
	0.00	0.38	0.40	0.77	0.53	0.91
	760.00	0.49	0.54	0.97	0.91	1.35
K	-100.00	0.57	0.60	1.20	0.82	1.43
	0.00	0.42	0.44	0.88	0.57	1.02
	1000.00	0.73	0.80	1.46	1.36	2.03
	1372.00	0.95	1.05	1.89	1.85	2.70
N	-100.00	0.66	0.69	1.48	0.90	1.70
	0.00	0.51	0.53	1.14	0.66	1.29
	400.00	0.46	0.49	0.99	0.72	1.23
	1300.00	0.75	0.83	1.53	1.45	2.16
E	-100.00	0.50	0.53	0.99	0.75	1.22
	0.00	0.36	0.38	0.72	0.52	0.86
	500.00	0.40	0.43	0.77	0.71	1.05
	1000.00	0.58	0.65	1.11	1.16	1.63
T	-150.00	0.79	0.84	1.66	1.16	1.99
	0.00	0.42	0.45	0.89	0.58	1.04
	400.00	0.37	0.40	0.74	0.61	0.97
R	250.00	0.96	0.98	2.48	1.14	2.65
	1000.00	0.86	0.91	2.10	1.29	2.48
	1767.00	1.14	1.24	2.65	1.96	3.38
S	250.00	1.01	1.03	2.62	1.20	2.80
	1000.00	0.97	1.02	2.37	1.42	2.77
	1767.00	1.29	1.39	3.02	2.17	3.80
B	600.00	1.26	1.28	3.52	1.40	3.64
	1000.00	0.92	0.95	2.48	1.16	2.69
	1820.00	0.97	1.03	2.41	1.51	2.89
C	0.00	0.76	0.78	1.87	0.92	2.01
	500.00	0.66	0.69	1.53	0.96	1.81
	1000.00	0.85	0.91	1.90	1.41	2.41
	1850.00	1.47	1.61	3.18	2.70	4.29
	2316.00	2.30	2.53	4.93	4.35	6.77

* Sensor inaccuracies are not included.

Table 1-3. 2620A/2625A Specifications (cont)

THERMOCOUPLE INPUTS (cont.)

Input Impedance

100 MΩ minimum in parallel with 150 pF maximum

Common Mode and Normal Mode Rejection

See Specifications, DC Voltage Inputs

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of this table.

Open Thermocouple Detect

Small ac signal injection and detection scheme before each measurement detects greater than 1 to 4 kΩ as open. Performed on each channel unless defeated by computer command.

RTD INPUTS

Type

DIN/IEC 751, 100Ω Platinum

RTD Temperature (°C)	1 Year, 4-Wire Accuracy (±°C)					
	Resolution		18°C to 28°C		0°C to 60°C	
	Slow	Fast	Slow	Fast	Slow	Fast
-200.00	0.02	0.1	0.08	0.49	0.12	0.54
0.00	0.02	0.1	0.21	0.67	0.50	0.96
100.00	0.02	0.1	0.27	0.75	0.69	1.17
300.00	0.02	0.1	0.41	0.92	1.10	1.60
600.00	0.02	0.1	0.65	1.21	1.77	2.33

2-Wire Accuracy

For 2-wire sensors with R0 = 100Ω: degrade accuracy by 5.0°C per lead-ohm, plus degrade accuracy an additional 4°C for channels 1 to 20 and 0.05°C for channel 0.

Maximum Current Through Sensor

1 mA

Typical Full Scale Voltage

0.22V

Maximum Open Circuit Voltage

3.2V

Maximum Sensor Temperature

600°C nominal

999.99°F is the maximum that can be displayed when using °F.

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of this table.

Table 1-3. 2620A/2625A Specifications (cont)

AC VOLTAGE INPUTS (TRUE RMS AC VOLTAGE, AC-COUPLED INPUTS)

Range	Resolution		Minimum Input for Rated Accuracy
	Slow	Fast	
300 mV	10 µV	100 µV	20 mV
3V	100 µV	1 mV	200 mV
30V	1 mV	10 mV	2V
300V	10 mV	100 mV	20V

1 Year Accuracy ±(%±V)

Frequency	18°C to 28°C		0°C to 60°C	
	Slow	Fast	Slow	Fast
300 mV Range				
20 Hz - 50 Hz	1.43% + 0.25 mV	1.43% + 0.4 mV	1.54% + 0.25 mV	1.54% + 0.4 mV
50 Hz - 100 Hz	0.30% + 0.25 mV	0.30% + 0.4 mV	0.41% + 0.25 mV	0.41% + 0.4 mV
100 Hz - 10 kHz	0.17% + 0.25 mV	0.17% + 0.4 mV	0.28% + 0.25 mV	0.28% + 0.4 mV
10 kHz - 20 kHz	0.37% + 0.25 mV	0.37% + 0.4 mV	0.68% + 0.25 mV	0.68% + 0.4 mV
20 kHz - 50 kHz	1.9% + 0.30 mV	1.9% + 0.5 mV	3.0% + 0.30 mV	3.0% + 0.5 mV
50 kHz - 100 kHz	5.0% + 0.50 mV	5.0% + 1.0 mV	7.0% + 0.50 mV	7.0% + 1.0 mV
3V Range				
20 Hz - 50 Hz	1.42% + 2.5 mV	1.42% + 4 mV	1.53% + 2.5 mV	1.53% + 4 mV
50 Hz - 100 Hz	0.29% + 2.5 mV	0.29% + 4 mV	0.40% + 2.5 mV	0.40% + 4 mV
100 Hz - 10 kHz	0.14% + 2.5 mV	0.14% + 4 mV	0.25% + 2.5 mV	0.25% + 4 mV
10 kHz - 20 kHz	0.22% + 2.5 mV	0.22% + 4 mV	0.35% + 2.5 mV	0.35% + 4 mV
20 kHz - 50 kHz	0.6% + 3.0 mV	0.6% + 5 mV	0.9% + 3.0 mV	0.9% + 5 mV
50 kHz - 100 kHz	1.0% + 5.0 mV	1.0% + 10 mV	1.4% + 5.0 mV	1.4% + 10 mV
30V Range				
20 Hz - 50 Hz	1.43% + 25 mV	1.43% + 40 mV	1.58% + 25 mV	1.58% + 40 mV
50 Hz - 100 Hz	0.29% + 25 mV	0.29% + 40 mV	0.45% + 25 mV	0.45% + 40 mV
100 Hz - 10 kHz	0.15% + 25 mV	0.15% + 40 mV	0.30% + 25 mV	0.30% + 40 mV
10 kHz - 20 kHz	0.22% + 25 mV	0.22% + 40 mV	0.40% + 25 mV	0.40% + 40 mV
20 kHz - 50 kHz	0.9% + 30 mV	0.9% + 50 mV	1.1% + 30 mV	1.1% + 50 mV
50 kHz - 100 kHz	2.0% + 50 mV	2.0% + 100 mV	2.2% + 50 mV	2.2% + 100 mV
300V Range				
20 Hz - 50 Hz	1.42% + 0.25V	1.42% + 0.4V	1.57% + 0.25V	1.57% + 0.4V
50 Hz - 100 Hz	0.29% + 0.25V	0.29% + 0.4V	0.44% + 0.25V	0.44% + 0.4V
100 Hz - 10 kHz	0.14% + 0.25V	0.14% + 0.4V	0.29% + 0.25V	0.29% + 0.4V
10 kHz - 20 kHz	0.22% + 0.25V	0.22% + 0.4V	0.38% + 0.25V	0.38% + 0.4V
20 kHz - 50 kHz	0.9% + 0.30V	0.9% + 0.5V	1.0% + 0.30V	1.0% + 0.5V
50 kHz - 100 kHz	2.5% + 0.50V	2.5% + 1.0V	2.6% + 0.50V	2.6% + 1.0V

Table 1-3. 2620A/2625A Specifications (cont)

AC VOLTAGE INPUTS (TRUE RMS AC VOLTAGE, AC-COUPLED INPUTS) (cont.)

Maximum Frequency	Input at Upper Frequency
20 Hz - 50 Hz	300V rms
50 Hz - 100 Hz	300V rms
100 Hz - 10 kHz	200V rms
10 kHz - 20 kHz	100V rms
20 kHz - 50 kHz	40V rms
50 kHz - 100 kHz	20V rms

Input Impedance

1 MΩ in parallel with 100 pF maximum

Maximum Crest Factor

3.0 maximum
2.0 for rated accuracy

Crest Factor Error

Non-sinusoidal input signals with crest factors between 2 and 3 and pulse widths 100 µs and longer add 0.2% to the accuracy specifications.

Common Mode Rejection

80 dB minimum at 50 or 60 Hz ±0.1%, 1 kΩ imbalance, slow rate

Maximum AC Input

300V rms or 424V peak on channels 0, 1, and 11
150V rms or 212V peak on channels 2 to 10 and 12 to 20
Voltage ratings between channels must not be exceeded
2×10^6 Volt-Hertz product on any range, normal mode input
1×10^6 Volt-Hertz product on any range, common mode input

DC Component Error

SCAN and first MONitor measurements will be incorrect if the dc signal component exceeds 60 counts in slow rate or 10 counts in fast rate. To measure ac with a dc component present, MONitor the input and wait 5 seconds before recording the measurement.

Using Channel 0

When measuring voltages above 100V rms, the rear Input Module must be installed to obtain the rated accuracy.

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of this table.

Table 1-3. 2620A/2625A Specifications (cont)

OHMS INPUTS

Range	Resolution		Typical Full Scale Voltage	Maximum Current Through Unknown	Maximum Open Circuit Voltage
	Slow	Fast			
300Ω	10 mΩ	0.1Ω	0.22V	1 mA	3.2V
3 kΩ	0.1Ω	1Ω	0.25V	110 µA	1.5V
30 kΩ	1Ω	10Ω	0.29V	13 µA	1.5V
300 kΩ	10Ω	100Ω	0.68V	3.2 µA	3.2V
3 MΩ	100Ω	1 kΩ	2.25V	3.2 µA	3.2V
10 MΩ	1 kΩ	10 kΩ	2.72V	3.2 µA	3.2V

4-Wire Accuracy ±(% ± Ω)					
RANGE	18°C to 28°C			0°C to 60°C	
	90 Days, Slow	1 Year, Slow	1 Year, Fast	1 Year, Slow	1 Year, Fast
300Ω Range	0.056%+20 mΩ	0.060%+20 mΩ	0.060%+0.2Ω	0.175%+20 mΩ	0.175%+0.2Ω
3 kΩ Range	0.053%+0.2Ω	0.057%+0.2Ω	0.057%+2Ω	0.172%+0.2Ω	0.172%+2Ω
30 kΩ Range	0.055%+2Ω	0.059%+2Ω	0.059%+20Ω	0.176%+2Ω	0.176%+20Ω
300 kΩ Range	0.053%+20Ω	0.057%+20Ω	0.057%+200Ω	0.184%+20Ω	0.184%+200Ω
3 MΩ Range	0.059%+200Ω	0.063%+200Ω	0.063%+2 kΩ	0.203%+200Ω	0.203%+2 kΩ
10 MΩ Range	0.115%+2 kΩ	0.120%+2 kΩ	0.200%+30 kΩ	0.423%+2 kΩ	0.423%+30 kΩ

2-wire Accuracy

Add 1.5Ω to accuracy specifications for channels 1 to 20, and add 20 mΩ for channel 0. Lead wire resistances are not included.

Input Protection

300V dc or ac rms on all ranges

Crosstalk Rejection

Refer to “Crosstalk Rejection” at the end of this table.

FREQUENCY INPUTS

Frequency Range

15 Hz to greater than 1 MHz

Range	Resolution		Accuracy ±(%±Hz)	
	Slow	Fast	Slow	Fast
15 Hz - 900 Hz	0.01 Hz	0.1 Hz	0.05% + 0.02 Hz	0.05% + 0.2 Hz
9 kHz	0.1 Hz	1 Hz	0.05% + 0.1 Hz	0.05% + 1 Hz
90 kHz	1 Hz	10 Hz	0.05% + 1 Hz	0.05% + 10 Hz
900 kHz	10 Hz	100 Hz	0.05% + 10 Hz	0.05% + 100 Hz
1 MHz	100 Hz	1 kHz	0.05% + 100 Hz	0.05% + 1 kHz

Table 1-3. 2620A/2625A Specifications (cont)

FREQUENCY INPUTS (cont.)

Sensitivity

Frequency	Level (Sine Wave)
15 Hz - 100 kHz	100 mV rms
100 kHz - 300 kHz	150 mV rms
300 kHz - 1 MHz	2V rms
Above 1 MHz	Not specified

Maximum AC Input

300V rms or 424V peak on channels 0, 1, and 11
150V rms or 212V peak on channels 2 to 10 and 12 to 20
Voltage ratings between channels must not be exceeded

2 x 10^6 Volt-Hertz product on any range, normal mode input
1 x 10^6 Volt-Hertz product on any range, common mode input

Crosstalk Rejection

Refer to “Crosstalk Rejection” at the end of this table.

TYPICAL SCANNING RATE

(Channels per Second, for 1, 10, and 20 Channel Scans with Shorted Inputs)

CHANNELS:		SLOW			FAST		
		1	10	20	1	10	20
VDC	300 mV	1.8	3.8	4.1	2.4	13.4	17.8
	3V	1.8	3.8	4.1	2.4	13.4	17.8
	30V	1.8	3.8	4.1	2.4	13.3	17.7
	150/300V	1.8	3.8	4.1	2.4	13.2	17.5
	AUTO	1.8	3.6	3.8	2.4	11.0	13.7
°F (TEMP)	J	1.0	3.3	3.8	2.1	11.2	15.8
	PT	1.8	3.6	3.8	2.3	8.1	9.4
VAC	300 mV	1.0	1.5	1.5	1.3	2.4	2.5
	3V	1.0	1.5	1.5	1.3	2.4	2.5
	30V	1.0	1.5	1.5	1.3	2.4	2.5
	150/300V	1.0	1.5	1.5	1.3	2.4	2.5
	AUTO	1.0	1.5	1.5	1.3	2.3	2.4
OHMS	300Ω	1.8	3.6	3.8	2.3	8.1	9.4
	3 kΩ	1.8	3.6	3.8	2.3	8.1	9.4
	30 kΩ	1.8	3.6	3.8	2.3	8.1	9.4
	300 kΩ	1.2	1.9	1.9	1.9	4.7	5.1
	3 MΩ	1.1	1.6	1.7	1.8	4.0	4.3
	10 MΩ	1.1	1.6	1.6	1.7	3.8	4.0
	AUTO	1.8	3.6	3.8	2.3	8.1	9.4
	AUTO (open)	1.1	1.6	1.6	1.7	3.8	4.0
FREQ	any	1.1	1.5	1.5	1.1	1.6	1.7

Table 1-3. 2620A/2625A Specifications (cont)

MAXIMUM AUTORANGING TIME (Seconds per Channel)

FUNCTION	RANGE CHANGE	SLOW	FAST
VDC	300 mV to 150V	0.25	0.19
	150V to 300 mV	0.25	0.18
VAC	300 mV to 150V	1.40	1.10
	150V to 300 mV	1.40	1.10
OHMS	300Ω to 10.0 MΩ	1.70	0.75
	10.0 MΩ to 300Ω	1.50	0.60

TOTALIZING INPUTS

Input Voltage	30V maximum -4V minimum 2V peak minimum signal
Isolation	None dc-coupled
Threshold	1.4V
Hysteresis	500 mV
Input Debouncing	None or 1.66 ms
Rate	0 to 5 kHz with debouncing off
Maximum Count	65,535

DIGITAL INPUTS

Input Voltage	30V maximum -4V minimum
Isolation	None dc-coupled
Threshold	1.4V
Hysteresis	500 mV

TRIGGER INPUT

Input Voltages	contact closure and TTL compatible "high" = 2.0V min, 7.0V max "low" = -0.6V min, 0.8V max
Isolation	None dc-coupled
Minimum Pulse Width	5 µs
Maximum Frequency	5 Hz
Specified Conditions	The instrument must be in the quiescent state, with no interval scans in process, no commands in the queue, no RS-232 or IEEE interface activity, and no front panel activity if the latency and repeatability performance is to be achieved. For additional information, refer to Section 5.
Maximum Latency	Latency is measured from the edge of the trigger input to the start of the first channel measurement for the Specified Conditions (above). 480 ms for fast rate, scanning DCV, ACV, ohms, and frequency only 550 ms for fast rate, scanning any thermocouple or 100 mV dc channels 440 ms for slow rate, scanning DCV, ACV, ohms, and frequency only 890 ms for slow rate, scanning any thermocouple or 100 mV dc channels
Repeatability	3 ms for the Specified Conditions (above)

Table 1-3. 2620A/2625A Specifications (cont)

DIGITAL AND ALARM OUTPUTS	
Output Logic Levels	
Logical "zero":	0.8V max for an Iout of -1.0 mA (1 LSTTL load)
Logical "one":	3.8V min for an Iout of 0.05 mA (1 LSTTL load)
For non-TTL loads:	
Logical "zero":	1.8V max for an Iout of -20 mA 3.25V max for an Iout of -50 mA
Isolation	None
REAL-TIME CLOCK AND CALENDAR	
Accuracy	Within 1 minute per month for 0°C to 50°C range
Battery Life	10 years minimum for Operating Temperature range
ENVIRONMENTAL	
Warmup Time	1 hour to rated specifications 15 minutes when relative humidity is kept below 50% (non-condensing)
Operating Temperature	0°C to 60°C (32°F to 140°F)
Storage Temperature	-40°C to +75°C (-40°F to +167°F) Instrument storage at low temperature extremes may necessitate adding up to 0.008% to the dc voltage and ac voltage accuracy specifications. Alternatively, any resulting shift can be compensated for by recalibrating the instrument.
Relative Humidity (Non-Condensing)	90% maximum for 0°C to 28°C (32°F to 82.4°F), 75% maximum for 28°C to 35°C (82.4°F to 95°F), 50% maximum for 35°C to 60°C (95°F to 140°F), (Except 70% maximum for 0°C to 35°C (32°F to 95°F) for the 300 kΩ, 3 MΩ, and 10 MΩ ranges.)
Altitude	
Operating:	3,050m (10,000 ft) maximum
Non-operating:	12,200m (40,000 ft) maximum
Vibration	0.7G at 15 Hz 1.3G at 25 Hz 3G at 55 Hz
Shock	30G half sine per Mil-T-28800 Bench handling per Mil-T-28800
GENERAL	
Channel Capacity	21 Analog Inputs 4 Alarm Outputs 8 Digital I/O (Inputs/Outputs)
Measurement Speed	
Slow rate:	4 readings/second nominal
Fast rate:	17 readings/second nominal
1.5 readings/second nominal for ACV and high-Ω inputs	
For additional information, refer to Typical Scanning Rate and Maximum Autoranging Time.	

Table 1-3. 2620A/2625A Specifications (cont)

Memory Life	10 years minimum over Operating Temperature range Stores: real-time clock, set-up configuration, and measurement data
Common Mode Voltage	300V dc or ac rms maximum from any analog input (channel) to earth provided that channel to channel maximum voltage ratings are observed.
Voltage Ratings	Channels 0, 1, and 11 are rated at 300V dc or ac rms maximum from a channel terminal to earth and from a channel terminal to any other channel terminal. Channels 2 to 10 and 12 to 20 are rated at 150V dc or ac rms maximum from a channel terminal to any other channel terminal within channels 2 to 10 and 12 to 20.
Size	9.3 cm high, 21.6 cm wide, 31.2 cm deep (3.67 in high, 8.5 in wide, 12.28 in deep)
Weight	Net, 2.95 kg (6.5 lbs) Shipping, 4.0 kg (8.7 lbs)
Power	90 to 264V ac (no switching required), 50 and 60 Hz, 10 VA maximum. 9V dc to 16V dc, 10W maximum. If both sources are applied simultaneously, ac is used if it exceeds approximately 8.3 times dc. Automatic switchover occurs between ac and dc without interruption. (At 120V ac the equivalent dc voltage is ~14.5V.)
Standards	Complies with IEC 1010, UL 1244 and CSA Bulletin 556B Complies with ANSI/ISA-S82.01-1988 and CSA C22.2 No.231 when common mode voltages and channel 0, 1, and 11 inputs are restricted to 250V dc or ac rms maximum. Complies with VDE 0871B when shielded cables are used. Complies with FCC-15B, at the Class A level when shielded cables are used.
RS-232-C	
Connector:	9 pin male (DB-9P)
Signals:	TX, RX, DTR, GND
Modem Control:	full duplex
Baud rates:	300, 600, 1200, 2400, 4800, and 9600
Data format:	8 data bits, no parity bit, one stop bit, or 7 data bits, one parity bit (odd or even), one stop bit
Flow control:	XON/XOFF
Echo:	on/off
2625A DATA STORAGE	
Storage	2047 Scans
Each scan includes:	• Time stamp • Readings for all defined analog input channels • Status of the four alarm outputs • Status of the eight digital I/O • Totalizer count
Memory	Battery-backed static RAM
Memory life:	5 years minimum at 25°C

Table 1-3. 2620A/2625A Specifications (cont)

2620A OPTIONS

IEEE-488 (Option -05K)

Capability codes:	SH1, AH1, T5, L4, SR1, RL1, PP0, DC1, DT1, E1, TE0, LE0 and C0

Complies with IEEE-488.1 standard

CROSSTALK REJECTION

AC signals can have effects on other channels (Crosstalk). These effects are discussed here by measurement function. These numbers should only be considered as references. Since Crosstalk can be introduced into a measurement system in many places, each setup must be considered individually.

The effect of Crosstalk could be much better than shown for "Typical"; in extreme cases, the effect could be worse than the "Worst Case" numbers. In general, the "Worst Case" information assumes that none of the guidelines for minimizing Crosstalk (User Manual Section 5) have been followed; the "Typical" information assumes that the guidelines have been followed where reasonable.

These numbers assume that input L (low) is tied to earth ground; refer to "Using Shielded Wiring" in Section 5 of the User Manual. For dc volts and thermocouple temperature measurements, a source impedance of 1 kΩ in series with the H (high) input is assumed (except where otherwise noted.)

AC Signal Crosstalk in a DC Voltage Channel

$$\text{DCV Error Ratio (CTRR)} = \left[\frac{VDC\,(error)}{VAC\;rms}\right]$$

Frequency	Worst cast	Typical
50, 60 Hz, ±0.1%:	1.1×10^{-7}	2.0×10^{-8}
Other Frequencies:	3.8×10^{-6}	8.6×10^{-7}

For example, to find the typical effect of a 300V ac signal at 60 Hz on another channel for the 300 mV range, you would calculate: $300 \times 2.0 \times 10^{-8} = 0.01$ mV.

AC Signal Crosstalk into an AC Voltage Channel

$$\text{ACV Error Ratio} = \left[\frac{VAC\;rms\,(error)}{VAC\;rms\,(crosstalk)\;x\;Frequency\,(crosstalk)}\right]$$

Range	Ratio (worst case)	Ratio (typical)
300.00 mV	$4.8 \times 10^{-8}\left[\frac{V}{V\,x\,Hz}\right]$	$1.4 \times 10^{-8}\left[\frac{V}{V\,x\,Hz}\right]$
3.0000V	$1.1 \times 10^{-7}\left[\frac{V}{V\,x\,Hz}\right]$	$3.0 \times 10^{-8}\left[\frac{V}{V\,x\,Hz}\right]$
30.000V	$1.2 \times 10^{-6}\left[\frac{V}{V\,x\,Hz}\right]$	$2.6 \times 10^{-7}\left[\frac{V}{V\,x\,Hz}\right]$
150.00/300.00V	$1.2 \times 10^{-5}\left[\frac{V}{V\,x\,Hz}\right]$	$3.4 \times 10^{-6}\left[\frac{V}{V\,x\,Hz}\right]$

For example, to find the typical effect of a 60 Hz, 220V ac signal on another channel for the the 300 mV range, you would calculate: $220 \times 60 \times 1.4 \times 10^{-8} = 0.18$ mV.

Table 1-3. 2620A/2625A Specifications (cont)

AC Signal Crosstalk into an Ohms Channel

AC Frequency = 50, 60 Hz, ±0.1%

$$\text{OHMS Error Ratio} = \left[\frac{Ohms\ (error)}{VAC\ rms\ (crosstalk)}\right]$$

Range	Ratio (worst case)	Ratio (typical)
300.00Ω	$3.3 \times 10^{-5}\left[\frac{Ohms}{VAC\ rms}\right]$	No Effect
3.000 kΩ	$2.4 \times 10^{-6}\left[\frac{kOhms}{VAC\ rms}\right]$	$6.7 \times 10^{-7}\left[\frac{kOhms}{VAC\ rms}\right]$
30.000 kΩ	$3.1 \times 10^{-4}\left[\frac{kOhms}{VAC\ rms}\right]$	$8.4 \times 10^{-5}\left[\frac{kOhms}{VAC\ rms}\right]$
300.00 kΩ	$5.6 \times 10^{-3}\left[\frac{kOhms}{VAC\ rms}\right]$	$3.7 \times 10^{-3}\left[\frac{kOhms}{VAC\ rms}\right]$
3.0000 MΩ	$3.8 \times 10^{-4}\left[\frac{MOhms}{VAC\ rms}\right]$	$3.8 \times 10^{-5}\left[\frac{MOhms}{VAC\ rms}\right]$
10.000 MΩ	$1.4 \times 10^{-3}\left[\frac{MOhms}{VAC\ rms}\right]$	$4.3 \times 10^{-4}\left[\frac{MOhms}{VAC\ rms}\right]$

For example, to find the typical effect of a 60 Hz, 100V ac signal on another channel for the 30 kΩ range, you would calculate: $100 \times 8.4 \times 10^{-5} = 0.008$ kΩ.

AC Signal Crosstalk into a Temperature Channel

Frequency = 50, 60 Hz

$$\text{TEMPERATURE Error Ratio} = \left[\frac{{}^\circ C\ (error)}{VAC\ rms\ (crosstalk)}\right]$$

Type	Worst case	Typical
Types J, K, E, T, N:	$2.7 \times 10^{-3}\left[\frac{{}^\circ C}{VAC\ rms}\right]$	$5.0 \times 10^{-4}\left[\frac{{}^\circ C}{VAC\ rms}\right]$
Types R. S, B, C:	$1.1 \times 10^{-2}\left[\frac{{}^\circ C}{VAC\ rms}\right]$	$2.0 \times 10^{-3}\left[\frac{{}^\circ C}{VAC\ rms}\right]$
Type PT (RTD):	$8.6 \times 10^{-5}\left[\frac{{}^\circ C}{VAC\ rms}\right]$	No Effect

AC Signal Crosstalk into a Frequency Channel

Frequency measurements are unaffected by Crosstalk as long as the voltage-frequency product is kept below the following limits:

	Worst Case	Typical
V x Hz Product Limit	3.7×10^{4} (V x Hz)	1.0×10^{6} (V x Hz)

[1] These values assume no more than 1000 pF of capacitance between either end of the resistor (HI and LOW) and earth ground.

Table 1-4. 2635A Specifications

The instrument specifications presented here are applicable within the conditions listed in the Environmental portion of this specification.

The specifications state total instrument accuracy following calibration, including:

- A/D errors
- Linearization conformity
- Initial calibration errors
- Isothermality errors
- Relay thermal emf's
- Reference junction conformity
- Temperature coefficients
- Humidity errors·

Sensor inaccuracies are not included in the accuracy figures.

Accuracies at ambient Temperatures Other Than Specified

To determine typical accuracies at temperatures intermediate to those listed in the specification tables, linearly interpolate between the applicable 0°C to 60°C and 18°C to 28°C accuracy specifications.

Response Times

Refer to Typical Scanning Rate and Maximum Autoranging Time later in this table.

DC VOLTAGE INPUTS

	Resolution	
Range	**Slow**	**Fast**
90 mV*	1 µV	10 µV
300 mV	10 µV	0.1 mV
3V	0.1 mV	1 mV
30V	1 mV	10 mV
150/300V	10 mV	0.1V
900 mV* **	10 µV	0.1 mV

* Not used in Autoranging.

** Computer interface only (see FUNC command).

Range	**Accuracy ±(% ± V)**				
	18°C to 28°C			**0°C to 60°C**	
	90 Days, Slow	**1 Year, Slow**	**1 Year, Fast**	**1 Year, Slow**	**1 Year, Fast**
90 mV*	0.29% + 7 uV	0.034% + 7 µV	0.054% + 20 µV	0.074% + 7 µV	0.094% + 20 µV
300 mV	0.026%+20 µV	0.031%+20 µV	0.047%+0.2 mV	0.070%+20 µV	0.087%+0.2 mV
3V	0.028%+0.2 mV	0.033%+0.2 mV	0.050%+2 mV	0.072%+0.2 mV	0.089%+2 mV
30V	0.024%+2 mV	0.029%+2 mV	0.046%+20 mV	0.090%+2 mV	0.107%+20 mV
150/300V	0.023%+20 mV	0.028%+20 mV	0.045%+0.2V	0.090%+20 mV	0.107%+0.2V
900 mV* **	0.026% + 20 µV	0.031% + 21 µV	0.047% + 0.2 mV	0.070% + 20 µV	0.087% + 0.2 mV

* Not used in Autoranging.

** Computer interface only (see FUNC command).

Table 1-4. 2635A Specifications (cont)

Input Impedance

100 MΩ minimum in parallel with 150 pF maximum for all ranges 3V and below
10 MΩ in parallel with 100 pF maximum for the 30V and 300V ranges

Normal Mode Rejection

53 dB minimum at 60 Hz ±0.1%, slow rate
47 dB minimum at 50 Hz ±0.1%, slow rate

Common Mode Rejection

120 dB minimum at dc, 1 kΩ imbalance, slow rate
120 dB minimum at 50 or 60 Hz ±0.1%, 1 kΩ imbalance, slow rate

Maximum Input

300V dc or ac rms on any range for channels 0, 1, and 11
150V dc or ac rms for channels 2 to 10 and 12 to 20
Voltage ratings between channels must not be exceeded

Crosstalk Rejection

Refer to “Crosstalk Rejection” at the end of Table 1-3.

Table 1-4. 2635A Specifications (cont)

THERMOCOUPLE INPUTS

Temperature Measurements - Accuracy (Thermocouples) (IPTS-68)

Thermocouple		Accuracy (±°C)*				
		18°C to 28°C			0°C to 60°C	
Type	Temperature (°C)	90 Days Slow	1 Year Slow	1 Year Fast	1 Year Slow	1 Year Fast
J	-100 to -30	0.44	0.45	0.87	0.54	1.05
	-30 to 150	0.40	0.42	0.78	0.58	1.00
	150 to 760	0.52	0.56	0.99	0.92	1.39
K	-100 to -25	0.53	0.54	1.08	0.64	1.27
	-25 to 120	0.46	0.47	0.92	0.63	1.14
	120 to 1000	0.94	1.00	1.66	1.54	2.27
	1000 to 1372	1.24	1.34	2.16	2.11	3.01
N	-100 to -25	0.65	0.66	1.39	0.75	1.57
	-25 to 120	0.57	0.58	1.20	0.70	1.37
	120 to 410	0.54	0.56	1.10	0.77	1.32
	410 to 1300	1.16	1.23	1.93	1.83	2.58
E	-100 to -25	0.44	0.46	0.86	0.55	1.05
	-25 to 350	0.43	0.45	0.76	0.66	1.02
	350 to 650	0.49	0.53	0.89	0.85	1.27
	650 to 1000	0.78	0.85	1.31	1.34	1.85
T	-150 to 0	0.72	0.73	1.46	0.83	1.68
	0 to 120	0.48	0.49	0.93	0.60	1.11
	120 to 400	0.45	0.48	0.82	0.68	1.07
R	250 to 400	1.02	1.04	2.54	1.17	2.71
	400 to 1000	1.09	1.13	2.37	1.49	2.71
	1000 to 1767	1.60	1.69	3.08	2.39	3.80
S	250 to 1000	1.19	1.24	2.70	1.26	3.00
	1000 to 1400	1.43	1.49	2.86	2.01	3.40
	1400 to 1767	1.78	1.88	3.48	2.61	4.25
B	600 to 1200	1.42	1.43	3.67	1.57	3.82
	1200 to 1550	1.36	1.40	2.70	1.78	3.09
	1550 to 1820	1.62	1.68	3.06	2.17	3.55
C	0 to 150	0.81	0.82	1.90	0.93	2.08
	150 to 650	0.81	0.85	1.71	1.16	2.07
	650 to 1000	1.05	1.11	2.10	1.59	2.63
	1000 to 1800	2.04	2.17	3.69	3.19	4.78
	1800 to 2316	3.29	3.51	5.87	5.26	7.72

* Sensor inaccuracies are not included.

Table 1-4. 2635A Specifications (cont)

THERMOCOUPLE INPUTS

Temperature Measurements - Accuracy (Thermocouples) (ITS-90)

Thermocouple		Accuracy (±°C)*				
		18°C to 28°C			0°C to 60°C	
Type	**Temperature (°C)**	**90 Days Slow**	**1 Year Slow**	**1 Year Fast**	**1 Year Slow**	**1 Year Fast**
J	-100 to -30	0.44	0.45	0.88	0.54	1.06
	-30 to 150	0.41	0.43	0.79	0.59	1.01
	150 to 760	0.51	0.55	0.98	0.91	1.39
K	-100 to -25	0.54	0.55	1.10	0.65	1.28
	-25 to 120	0.47	0.49	0.94	0.65	1.16
	120 to 1000	0.75	0.82	1.47	1.35	2.08
	1000 to 1372	1.11	1.21	2.03	1.98	2.88
N	-100 to -25	0.66	0.67	1.41	0.77	1.58
	-25 to 120	0.57	0.58	1.20	0.69	1.37
	120 to 410	0.51	0.53	1.07	0.67	1.27
	410 to 1300	0.81	0.88	1.58	1.48	2.23
E	-100 to -25	0.46	0.47	0.87	0.57	1.06
	-25 to 350	0.40	0.41	0.75	0.62	0.98
	350 to 650	0.49	0.53	0.89	0.86	1.27
	650 to 1000	0.59	0.65	1.11	1.14	1.65
T	-150 to 0	0.70	0.72	1.45	0.82	1.67
	0 to 120	0.48	0.49	0.93	0.60	1.11
	120 to 400	0.40	0.43	0.78	0.63	1.02
R	250 to 400	0.96	0.98	2.48	1.13	2.66
	400 to 1000	0.92	0.94	2.32	1.27	2.54
	1000 to 1767	1.17	1.26	2.69	1.98	3.43
S	250 to 1000	1.01	1.03	2.61	1.39	2.80
	1000 to 1400	1.03	1.09	2.45	1.61	3.00
	1400 to 1767	1.32	1.41	3.06	2.17	3.85
B	600 to 1200	1.30	1.31	3.56	1.45	3.71
	1200 to 1550	0.90	0.94	2.32	1.31	2.62
	1550 to 1820	1.01	1.07	2.44	1.56	2.94
C	0 to 150	0.80	0.81	1.89	0.92	2.07
	150 to 650	0.71	0.75	1.62	1.06	1.97
	650 to 1000	0.86	0.92	1.90	1.39	2.43
	1000 to 1800	1.42	1.55	3.07	2.57	4.16
	1800 to 2316	2.34	2.56	4.92	4.32	6.78

* Sensor inaccuracies are not included.

Table 1-4. 2635A Specifications (cont)

THERMOCOUPLE INPUTS (cont.)

Input Impedance

100 MΩ minimum in parallel with 150 pF maximum

Common Mode and Normal Mode Rejection

See Specifications, DC Voltage Inputs

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of Table 1-3.

Open Thermocouple Detect

Small ac signal injection and detection scheme before each measurement detects greater than 1 to 4 kΩ as open. Performed on each channel unless defeated by computer command.

RTD INPUTS

Type

DIN/IEC 751, 100Ω Platinum

RTD Temperature (°C)	1 Year, 4-Wire Accuracy (±°C)					
	Resolution		18°C to 28°C		0°C to 60°C	
	Slow	Fast	Slow	Fast	Slow	Fast
-200.00	0.02	0.1	0.08	0.49	0.12	0.54
0.00	0.02	0.1	0.21	0.67	0.50	0.96
100.00	0.02	0.1	0.27	0.75	0.69	1.17
300.00	0.02	0.1	0.41	0.92	1.10	1.60
600.00	0.02	0.1	0.65	1.21	1.77	2.33

2-Wire Accuracy

For 2-wire sensors with R0 = 100Ω: degrade accuracy by 5.0°C per lead-ohm, plus degrade accuracy an additional 4°C for channels 1 to 20 and 0.05°C for channel 0.

Maximum Current Through Sensor

1 mA

Typical Full Scale Voltage

0.22V

Maximum Open Circuit Voltage

3.2V

Maximum Sensor Temperature

600°C nominal

999.99°F is the maximum that can be displayed when using °F.

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of Table 1-3.

Table 1-4. 2635A Specifications (cont)

AC VOLTAGE INPUTS (TRUE RMS AC VOLTAGE, AC-COUPLED INPUTS)

Range	Resolution		Minimum Input for Rated Accuracy
	Slow	Fast	
300 mV	10 µV	100 µV	20 mV
3V	100 µV	1 mV	200 mV
30V	1 mV	10 mV	2V
150/300V	10 mV	100 mV	20V

1 Year Accuracy ±(%±V)

Frequency	18°C to 28°C		0°C to 60°C	
	Slow	Fast	Slow	Fast
300 mV Range				
20 Hz - 50 Hz	1.43% + 0.25 mV	1.43% + 0.4 mV	1.54% + 0.25 mV	1.54% + 0.4 mV
50 Hz - 100 Hz	0.30% + 0.25 mV	0.30% + 0.4 mV	0.41% + 0.25 mV	0.41% + 0.4 mV
100 Hz - 10 kHz	0.17% + 0.25 mV	0.17% + 0.4 mV	0.28% + 0.25 mV	0.28% + 0.4 mV
10 kHz - 20 kHz	0.37% + 0.25 mV	0.37% + 0.4 mV	0.68% + 0.25 mV	0.68% + 0.4 mV
20 kHz - 50 kHz	1.9% + 0.30 mV	1.9% + 0.5 mV	3.0% + 0.30 mV	3.0% + 0.5 mV
50 kHz - 100 kHz	5.0% + 0.50 mV	5.0% + 1.0 mV	7.0% + 0.50 mV	7.0% + 1.0 mV
3V Range				
20 Hz - 50 Hz	1.42% + 2.5 mV	1.42% + 4 mV	1.53% + 2.5 mV	1.53% + 4 mV
50 Hz - 100 Hz	0.29% + 2.5 mV	0.29% + 4 mV	0.40% + 2.5 mV	0.40% + 4 mV
100 Hz - 10 kHz	0.14% + 2.5 mV	0.14% + 4 mV	0.25% + 2.5 mV	0.25% + 4 mV
10 kHz - 20 kHz	0.22% + 2.5 mV	0.22% + 4 mV	0.35% + 2.5 mV	0.35% + 4 mV
20 kHz - 50 kHz	0.6% + 3.0 mV	0.6% + 5 mV	0.9% + 3.0 mV	0.9% + 5 mV
50 kHz - 100 kHz	1.0% + 5.0 mV	1.0% + 10 mV	1.4% + 5.0 mV	1.4% + 10 mV
30V Range				
20 Hz - 50 Hz	1.43% + 25 mV	1.43% + 40 mV	1.58% + 25 mV	1.58% + 40 mV
50 Hz - 100 Hz	0.29% + 25 mV	0.29% + 40 mV	0.45% + 25 mV	0.45% + 40 mV
100 Hz - 10 kHz	0.15% + 25 mV	0.15% + 40 mV	0.30% + 25 mV	0.30% + 40 mV
10 kHz - 20 kHz	0.22% + 25 mV	0.22% + 40 mV	0.40% + 25 mV	0.40% + 40 mV
20 kHz - 50 kHz	0.9% + 30 mV	0.9% + 50 mV	1.1% + 30 mV	1.1% + 50 mV
50 kHz - 100 kHz	2.0% + 50 mV	2.0% + 100 mV	2.2% + 50 mV	2.2% + 100 mV
150/300V Range				
20 Hz - 50 Hz	1.42% + 0.25V	1.42% + 0.4V	1.57% + 0.25V	1.57% + 0.4V
50 Hz - 100 Hz	0.29% + 0.25V	0.29% + 0.4V	0.44% + 0.25V	0.44% + 0.4V
100 Hz - 10 kHz	0.14% + 0.25V	0.14% + 0.4V	0.29% + 0.25V	0.29% + 0.4V
10 kHz - 20 kHz	0.22% + 0.25V	0.22% + 0.4V	0.38% + 0.25V	0.38% + 0.4V
20 kHz - 50 kHz	0.9% + 0.30V	0.9% + 0.5V	1.0% + 0.30V	1.0% + 0.5V
50 kHz - 100 kHz	2.5% + 0.50V	2.5% + 1.0V	2.6% + 0.50V	2.6% + 1.0V

Table 1-4. 2635A Specifications (cont)

AC VOLTAGE INPUTS (TRUE RMS AC VOLTAGE, AC-COUPLED INPUTS) (cont.)

Maximum Frequency	Input at Upper Frequency
20 Hz - 50 Hz	300V rms
50 Hz - 100 Hz	300V rms
100 Hz - 10 kHz	200V rms
10 kHz - 20 kHz	100V rms
20 kHz - 50 kHz	40V rms
50 kHz - 100 kHz	20V rms

Input Impedance

1 MΩ in parallel with 100 pF maximum

Maximum Crest Factor

3.0 maximum

2.0 for rated accuracy

Crest Factor Error

Non-sinusoidal input signals with crest factors between 2 and 3 and pulse widths 100 µs and longer add 0.2% to the accuracy specifications.

Common Mode Rejection

80 dB minimum at 50 or 60 Hz ±0.1%, 1 kΩ imbalance, slow rate

Maximum AC Input

300V rms or 424V peak on channels 0, 1, and 11

150V rms or 212V peak on channels 2 to 10 and 12 to 20

Voltage ratings between channels must not be exceeded

2 x 10^6 Volt-Hertz product on any range, normal mode input

1 x 10^6 Volt-Hertz product on any range, common mode input

DC Component Error

SCAN and first MONitor measurements will be incorrect if the dc signal component exceeds 60 counts in slow rate or 10 counts in fast rate. To measure ac with a dc component present, MONitor the input and wait 5 seconds before recording the measurement.

Using Channel 0

When measuring voltages above 100V rms, the rear Input Module must be installed to obtain the rated accuracy.

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of Table 1-3.

Table 1-4. 2635A Specifications (cont)

OHMS INPUTS

Range	Resolution		Typical Full Scale Voltage	Maximum Current Through Unknown	Maximum Open Circuit Voltage
	Slow	Fast			
300Ω	10 mΩ	0.1Ω	0.22V	1 mA	3.2V
3 kΩ	0.1Ω	1Ω	0.25V	110 µA	1.5V
30 kΩ	1Ω	10Ω	0.29V	13 µA	1.5V
300 kΩ	10Ω	100Ω	0.68V	3.2 µA	3.2V
3 MΩ	100Ω	1 kΩ	2.25V	3.2 µA	3.2V
10 MΩ	1 kΩ	10 kΩ	2.72V	3.2 µA	3.2V

4-Wire Accuracy ±(% ± Ω)

RANGE	18°C to 28°C			0°C to 60°C	
	90 Days, Slow	1 Year, Slow	1 Year, Fast	1 Year, Slow	1 Year, Fast
300Ω Range	0.056%+20 mΩ	0.060%+20 mΩ	0.060%+0.2Ω	0.175%+20 mΩ	0.175%+0.2Ω
3 kΩ Range	0.053%+0.2Ω	0.057%+0.2Ω	0.057%+2Ω	0.172%+0.2Ω	0.172%+2Ω
30 kΩ Range	0.055%+2Ω	0.059%+2Ω	0.059%+20Ω	0.176%+2Ω	0.176%+20Ω
300 kΩ Range	0.053%+20Ω	0.057%+20Ω	0.057%+200Ω	0.184%+20Ω	0.184%+200Ω
3 MΩ Range	0.059%+200Ω	0.063%+200Ω	0.063%+2 kΩ	0.203%+200Ω	0.203%+2 kΩ
10 MΩ Range	0.115%+2 kΩ	0.120%+2 kΩ	0.200%+30 kΩ	0.423%+2 kΩ	0.423%+30 kΩ

2-wire Accuracy

Add 1.5Ω to accuracy specifications for channels 1 to 20, and add 20 mΩ for channel 0. Lead wire resistances are not included.

Input Protection

300V dc or ac rms on all ranges

Crosstalk Rejection

Refer to “Crosstalk Rejection” at the end of Table 1-3.

FREQUENCY INPUTS

Frequency Range

15 Hz to greater than 1 MHz

Range	Resolution		Accuracy ±(%±Hz)	
	Slow	Fast	Slow	Fast
15 Hz - 900 Hz	0.01 Hz	0.1 Hz	0.05% + 0.02 Hz	0.05% + 0.2 Hz
9 kHz	0.1 Hz	1 Hz	0.05% + 0.1 Hz	0.05% + 1 Hz
90 kHz	1 Hz	10 Hz	0.05% + 1 Hz	0.05% + 10 Hz
900 kHz	10 Hz	100 Hz	0.05% + 10 Hz	0.05% + 100 Hz
1 MHz	100 Hz	1 kHz	0.05% + 100 Hz	0.05% + 1 kHz

Table 1-4. 2635A Specifications (cont)

FREQUENCY INPUTS (cont.)

Sensitivity

Frequency	Level (Sine Wave)
15 Hz - 100 kHz	100 mV rms
100 kHz - 300 kHz	150 mV rms
300 kHz - 1 MHz	2V rms
Above 1 MHz	Not specified

Maximum AC Input

300V rms or 424V peak on channels 0, 1, and 11
150V rms or 212V peak on channels 2 to 10 and 12 to 20
Voltage ratings between channels must not be exceeded

2×10^6 Volt-Hertz product on any range, normal mode input
1×10^6 Volt-Hertz product on any range, common mode input

Crosstalk Rejection

Refer to “Crosstalk Rejection” at the end of Table 1-3.

TYPICAL SCANNING RATE

(Channels per Second, for 1, 10, and 20 Channel Scans with Shorted Inputs)

CHANNELS:		SLOW			FAST		
		1	10	20	1	10	20
VDC	300 mV	1.8	3.8	4.1	2.1	13.3	17.8
	3V	1.8	3.8	4.1	2.1	13.3	17.8
	30V	1.8	3.8	4.1	2.1	13.3	17.7
	150/300V	1.8	3.8	4.1	2.1	13.2	17.5
	AUTO	1.8	3.6	3.8	2.1	11.1	13.7
°F (TEMP)	J	1.0	3.3	3.8	2.1	11.7	16.0
	PT	1.8	3.6	3.8	2.3	8.1	9.4
VAC	300 mV	1.0	1.5	1.5	1.3	2.4	2.5
	3V	1.0	1.5	1.5	1.3	2.4	2.5
	30V	1.0	1.5	1.5	1.3	2.4	2.5
	150/300V	1.0	1.5	1.5	1.3	2.4	2.5
	AUTO	1.0	1.5	1.5	1.3	2.3	2.4
OHMS	300Ω	1.8	3.6	3.8	2.3	8.1	9.4
	3 kΩ	1.8	3.6	3.8	2.3	8.1	9.4
	30 kΩ	1.8	3.6	3.8	2.3	8.1	9.4
	300 kΩ	1.2	1.9	1.9	1.9	4.7	5.1
	3 MΩ	1.1	1.6	1.7	1.8	4.0	4.3
	10 MΩ	1.1	1.6	1.6	1.7	3.7	4.0
	AUTO	1.8	3.6	3.8	2.3	8.1	9.4
	AUTO (open)	1.1	1.6	1.6	1.7	3.8	4.0
FREQ	any	1.1	1.5	1.5	1.1	1.6	1.7

Table 1-4. 2635A Specifications (cont)

MAXIMUM AUTORANGING TIME (Seconds per Channel)

FUNCTION	RANGE CHANGE	SLOW	FAST
VDC	300 mV to 150V	0.25	0.19
	150V to 300 mV	0.25	0.18
VAC	300 mV to 150V	1.40	1.10
	150V to 300 mV	1.40	1.10
OHMS	300Ω to 10.0 MΩ	1.70	0.75
	10.0 MΩ to 300Ω	1.50	0.60

TOTALIZING INPUTS

Input Voltage	30V maximum -4V minimum 2V peak minimum signal
Isolation	None dc-coupled
Threshold	1.4V
Hysteresis	500 mV
Input Debouncing	None or 1.75 ms
Rate	0 to 5 kHz with debouncing off
Maximum Count	65,535

DIGITAL INPUTS

Input Voltage	30V maximum -4V minimum
Isolation	None dc-coupled
Threshold	1.4V
Hysteresis	500 mV

TRIGGER INPUT

Input Voltages	contact closure and TTL compatible "high" = 2.0V min, 7.0V max "low" = -0.6V min, 0.8V max
Isolation	None dc-coupled
Minimum Pulse Width	5 µs
Maximum Frequency	5 Hz
Specified Conditions	The instrument must be in the quiescent state, with no interval scans in process, no commands in the queue, no RS-232 activity, and no front panel activity if the latency and repeatability performance is to be achieved. For additional information, refer to Section 5.
Maximum Latency	Latency is measured from the edge of the trigger input to the start of the first channel measurement for the Specified Conditions (above). 540 ms for fast rate, scanning DCV, ACV, ohms, and frequency only 610 ms for fast rate, scanning any thermocouple or 100 mV dc channels 500 ms for slow rate, scanning DCV, ACV, ohms, and frequency only 950 ms for slow rate, scanning any thermocouple or 100 mV dc channels
Repeatability	3 ms for the Specified Conditions (above)

Table 1-4. 2635A Specifications (cont)

DIGITAL AND ALARM OUTPUTS	
Output Logic Levels	
Logical "zero":	0.8V max for an Iout of -1.0 mA (1 LSTTL load)
Logical "one":	3.8V min for an Iout of 0.05 mA (1 LSTTL load)
For non-TTL loads:	
Logical "zero":	1.8V max for an Iout of -20 mA 3.25V max for an Iout of -50 mA
Isolation	None
REAL-TIME CLOCK AND CALENDAR	
Accuracy	Within 1 minute per month for 0°C to 50°C range
Battery Life	>10 unpowered instrument years for 0°C to 28°C (32°F to 82.4°F). >3 unpowered instrument years for 0°C to 50°C (32°F to 122°F). >2 unpowered instrument years for 50°C to 70°C (122°F to 158°F).
ENVIRONMENTAL	
Warmup Time	1 hour to rated specifications 15 minutes when relative humidity is kept below 50% (non-condensing)
Operating Temperature	0°C to 60°C (32°F to 140°F)
Storage Temperature	-40°C to +70°C (-40°F to +158°F) Instrument storage at low temperature extremes may necessitate adding up to 0.008% to the dc voltage and ac voltage accuracy specifications. Alternatively, any resulting shift can be compensated for by recalibrating the instrument.
Relative Humidity (Non-Condensing)	90% maximum for 0°C to 28°C (32°F to 82.4°F), 75% maximum for 28°C to 35°C (82.4°F to 95°F), 50% maximum for 35°C to 60°C (95°F to 140°F), (Except 70% maximum for 0°C to 35°C (32°F to 95°F) for the 300 kΩ, 3 MΩ, and 10 MΩ ranges.)
Altitude	
Operating:	3,050m (10,000 ft) maximum
Non-operating:	12,200m (40,000 ft) maximum
Vibration	0.7G at 15 Hz 1.3G at 25 Hz 3G at 55 Hz
Shock	30G half sine per Mil-T-28800 Bench handling per Mil-T-28800

Table 1-4. 2635A Specifications (cont)

GENERAL	
Channel Capacity	21 Analog Inputs 4 Alarm Outputs 8 Digital I/O (Inputs/Outputs)
Measurement Speed	
Slow rate:	4 readings/second nominal
Fast rate:	17 readings/second nominal
1.5 readings/second nominal for ACV and high-Ω inputs	
For additional information, refer to Typical Scanning Rate and Maximum Autoranging Time.	
Nonvolatile Memory Life	>10 unpowered instrument years for 0°C to 28°C (32°F to 82.4°F). >3 unpowered instrument years for 0°C to 50°C (32°F to 122°F). >2 unpowered instrument years for 50°C to 70°C (122°F to 158°F).
Common Mode Voltage	300V dc or ac rms maximum from any analog input (channel) to earth provided that channel to channel maximum voltage ratings are observed.
Voltage Ratings	Channels 0, 1, and 11 are rated at 300V dc or ac rms maximum from a channel terminal to earth and from a channel terminal to any other channel terminal. Channels 2 to 10 and 12 to 20 are rated at 150V dc or ac rms maximum from a channel terminal to any other channel terminal within channels 2 to 10 and 12 to 20.
Size	9.3 cm high, 21.6 cm wide, 31.2 cm deep (3.67 in high, 8.5 in wide, 12.28 in deep)
Weight	Net, 2.95 kg (6.5 lbs) Shipping, 4.0 kg (8.7 lbs)
Power	90 to 264V ac (no switching required), 50 and 60 Hz, 10 VA maximum. 9V dc to 16V dc, 10W maximum. If both sources are applied simultaneously, ac is used if it exceeds approximately 8.3 times dc. Automatic switchover occurs between ac and dc without interruption. (At 120V ac the equivalent dc voltage is ~14.5V.)
Standards	Complies with IEC 1010, UL 1244 and CSA Bulletin 556B Complies with ANSI/ISA-S82.01-1988 and CSA C22.2 No.231 when common mode voltages and channel 0, 1, and 11 inputs are restricted to 250V dc or ac rms maximum. Complies with Vfg. 243/1991 when shielded cables are used. Complies with FCC-15B, at the Class B level when shielded cables are used.

Table 1-4. 2635A Specifications (cont)

RS-232-C	
Connector:	9 pin male (DB-9P)
Signals:	TX, RX, DTR, DSR, RTS, CTS, GND
Modem Control:	full duplex
Baud rates:	300, 600, 1200, 2400, 4800, 9600, 19200, and 38400
Data format:	8 data bits, no parity bit, one stop bit, or 7 data bits, one parity bit (odd or even), one stop bit
Flow control:	XON/XOFF (Software) and CTS (Hardware)
Echo:	on/off

Section 2

Theory of Operation (2620A/2625A)

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INTRODUCTION 2-1.

The theory of operation begins with a general overview of the instrument and progresses to a detailed description of the circuits of each pca.

The instrument is first described in general terms with a Functional Block Description. Then, each block is detailed further (often to the component level) with Detailed Circuit Descriptions. Refer to Section 8 of this manual for full schematic diagrams. The Interconnect Diagram in this section (Figure 2-1) illustrates physical connections among pca's.

Signal names followed by a '*' are active (asserted) low. All other signals are active high.

FUNCTIONAL BLOCK DESCRIPTION 2-2.

Refer to Figure 2-2, Overall Functional Block Diagram, during the following functional block descriptions.

Main PCA Circuitry 2-3.

The following paragraphs describe the major circuit blocks on the Main PCA.

POWER SUPPLY 2-4.

The Power Supply functional block provides voltages required by the vacuum-fluorescent display (-30V dc, -5.0V dc, and filament voltage of 5.4V ac), the inguard circuitry (-5.4V dc VSS, +5.3V dc VDD, and +5.6V dc VDDR), and outguard digital circuitry of +5.1V dc (VCC).

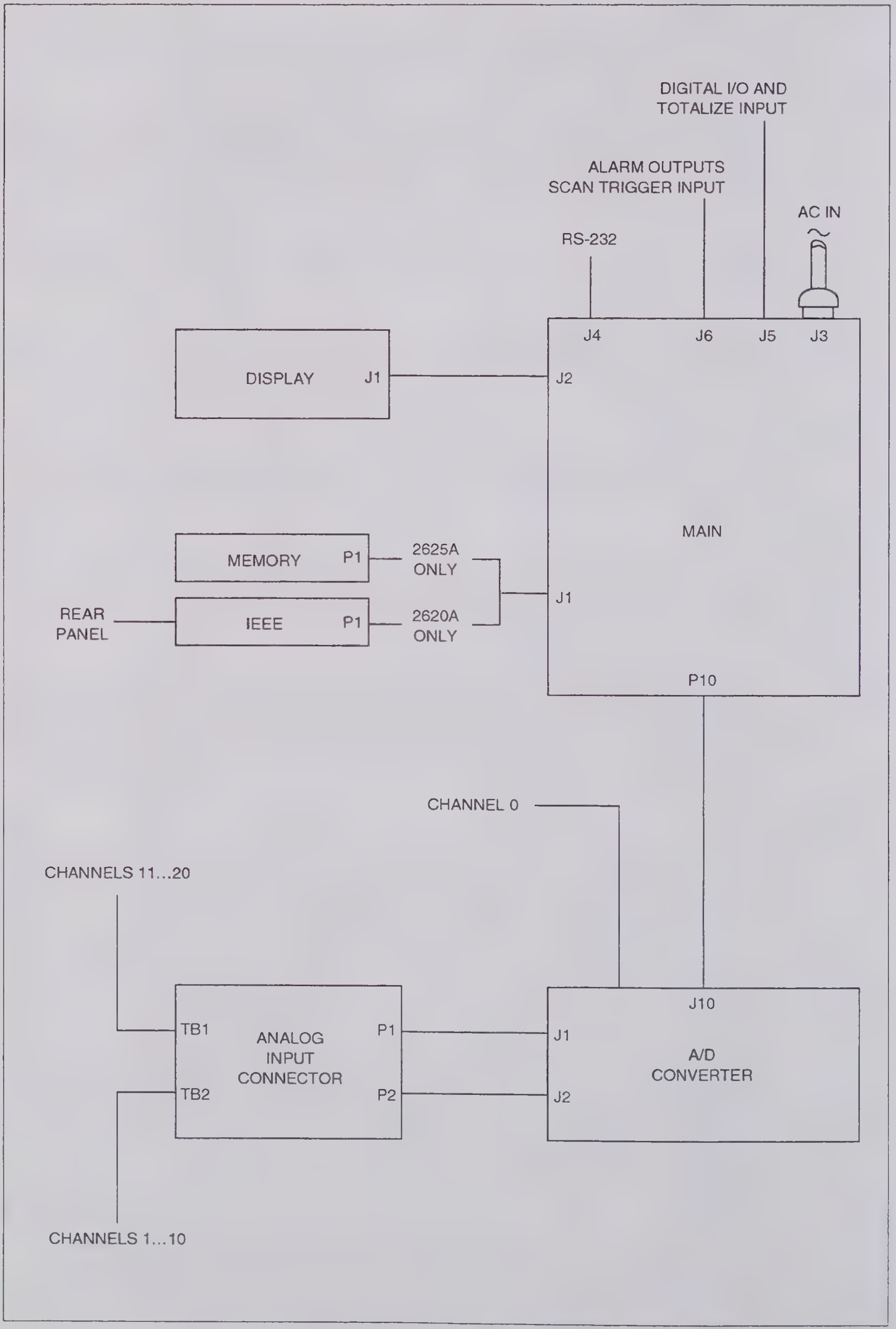
Within the Power Supply, the Raw DC Supply converts ac line voltage to dc levels. The 5V Switching Supply converts this raw dc to 5.1V ±0.25V dc, which is used by the Inverter in generating the above-mentioned outputs. The Power Fail Detector monitors the Raw DC Supply and provides a power supply status signal to the Microprocessor in the Digital Kernel.

DIGITAL KERNEL 2-5.

The Digital Kernel functional block is responsible for the coordination of all activities within the instrument. This block requires power supply voltages from the Power Supply and reset signals from the Display Assembly.

Specifically, the Digital Kernel Microprocessor performs the following functions:

- Executes the instructions in ROM.
- Stores temporary data in RAM.
- Stores instrument configuration and calibration data in nonvolatile RAM and EEPROM.
- Communicates with the microcontroller on the A/D Converter PCA via the Serial Communication (Guard Crossing) block.
- Communicates with the Display Controller to display readings and user interface information.
- Scans the user interface keyboard found on the Display Assembly.
- Communicates via the RS-232 interface and optional IEEE-488 interfaces.
- Reads digital inputs and changes digital and alarm outputs.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J2
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ANALOG INPUT CONNECTOR
P1
J1
J10
A/D CONVERTER
TB2
P2
J2
CHANNELS 1...10

Figure 2-1. Interconnect Diagram

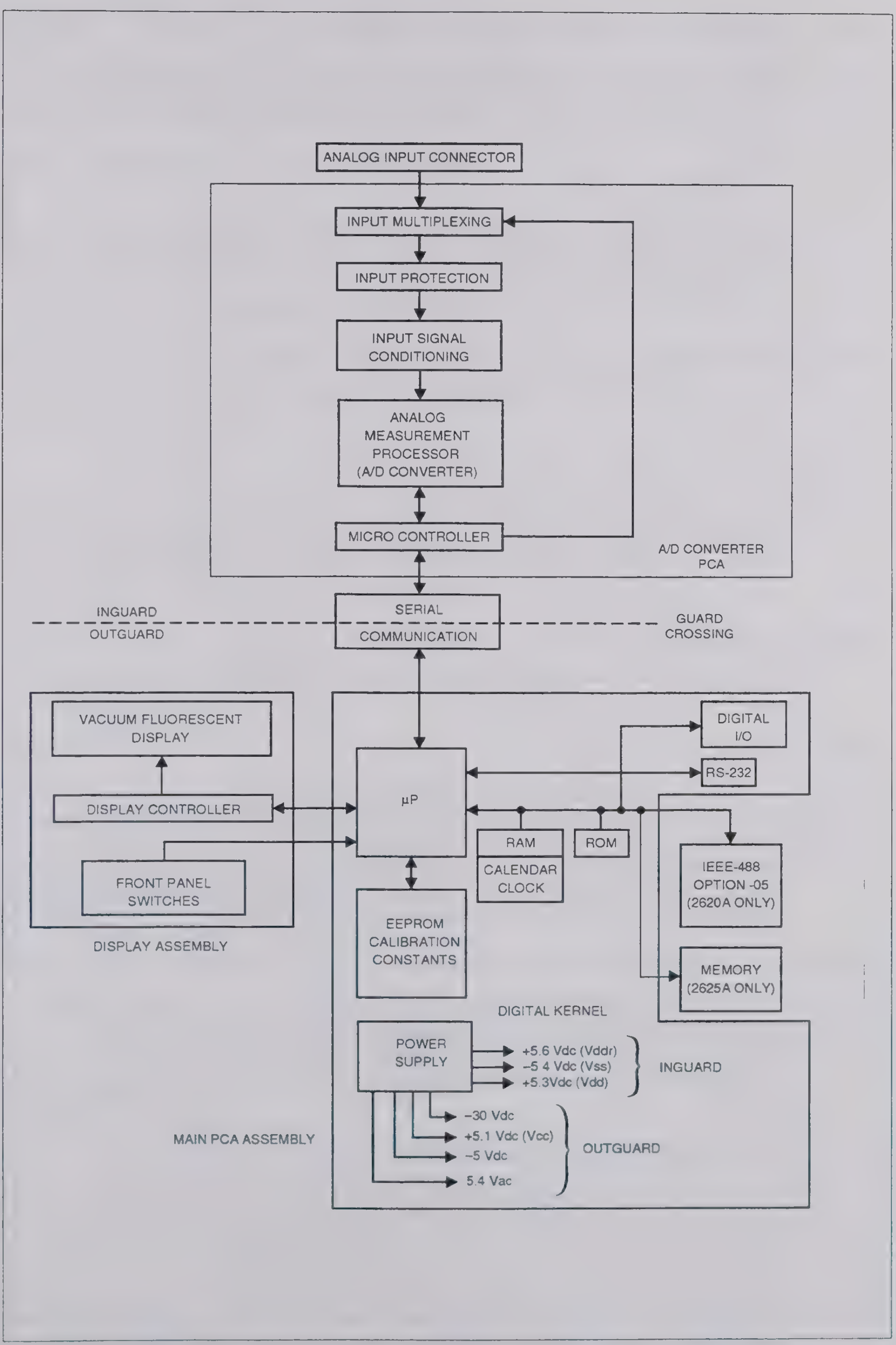

ANALOG INPUT CONNECTOR
INPUT MULTIPLEXING
INPUT PROTECTION
INPUT SIGNAL CONDITIONING
ANALOG MEASUREMENT PROCESSOR (A/D CONVERTER)
MICRO CONTROLLER
A/D CONVERTER PCA
INGUARD
OUTGUARD
SERIAL COMMUNICATION
GUARD CROSSING
VACUUM FLUORESCENT DISPLAY
DISPLAY CONTROLLER
FRONT PANEL SWITCHES
DISPLAY ASSEMBLY
μP
DIGITAL I/O
RS-232
RAM
CALENDAR CLOCK
ROM
IEEE-488 OPTION -05 (2620A ONLY)
EEPROM CALIBRATION CONSTANTS
MEMORY (2625A ONLY)
DIGITAL KERNEL
POWER SUPPLY
+5.6 Vdc (Vddr)
−5.4 Vdc (Vss)
+5.3Vdc (Vdd)
INGUARD
−30 Vdc
+5.1 Vdc (Vcc)
−5 Vdc
5.4 Vac
OUTGUARD
MAIN PCA ASSEMBLY

Figure 2-2. Overall Functional Block Diagram

SERIAL COMMUNICATION (GUARD CROSSING) 2-6.

This functional block provides a high isolation voltage communication path between the Digital Kernel of the Main PCA and the microcontroller on the A/D Converter PCA. This bidirectional communication circuit requires power supply voltages from the Power Supply block.

DIGITAL INPUTS AND OUTPUT 2-7.

This functional block contains the Totalizer, Totalizer Debouncer, eight bidirectional Digital I/O channels, four Alarm Outputs, and the Input Threshold control circuits. These circuits require power supply voltages from the Power Supply, a reset signal from the Display PCA, and signals from the Digital Kernel.

A/D Converter PCA 2-8.

The following paragraphs describe the major blocks of circuitry on the A/D Converter PCA.

ANALOG MEASUREMENT PROCESSOR 2-9.

The Analog Measurement Processor (A3U8) provides input signal conditioning, ranging, a/d conversion, and frequency measurement. This custom chip is controlled by the A/D Microcontroller (A3U9). The A/D Microcontroller communicates with the Main PCA processor (A1U4) over a custom serial interface.

INPUT PROTECTION CIRCUITRY 2-10.

This circuitry protects the instrument measurement circuits during overvoltage conditions.

INPUT SIGNAL CONDITIONING 2-11.

Here, each input is conditioned and/or scaled to a dc voltage for measurement by the a/d converter. DC voltage levels greater than 3V are attenuated. To measure resistance, a dc voltage is applied across a series connection of the input resistance and a reference resistance to develop dc voltages that can be ratioed. DC volts and ohms measurements are filtered by a passive filter. AC voltages are first scaled by an ac buffer, converted to a representative dc voltage by an rms converter, and then filtered by an active filter.

ANALOG-TO-DIGITAL (A/D) CONVERTER 2-12.

The dc voltage output from the signal conditioning circuits is applied to a buffer/integrator which charges a capacitor for an exact amount of time. The time required to discharge this capacitor, which is proportional to the level of the unknown input signal, is then measured by the digital counter circuits in the Analog Measurement Processor.

INGUARD MICROCONTROLLER CIRCUITRY 2-13.

This microcontroller (and associated circuitry) controls all functions on the A/D Converter PCA and communicates with the digital kernel on the Main PCA. Upon request by the Main PCA, the inguard microcontroller selects the input channel to be measured through the channel selection circuitry, sets up the input signal conditioning, commands the Analog Measurement Processor to begin a conversion, stops the measurement, and then fetches the measurement result. The inguard microcontroller manipulates the result mathematically and transmits the reading to the digital kernel.

CHANNEL SELECTION CIRCUITRY 2-14.

This circuitry consists of a set of relays and relay-control drivers. The relays form a tree that routes the input channels to the measurement circuitry. Two of the relays are also used to switch between 2-wire and 4-wire operation.

OPEN THERMOCOUPLE CHECK CIRCUITRY 2-15.

Under control of the Inguard Microcontroller, the open thermocouple check circuit applies a small ac signal to a thermocouple input before each measurement. If an excessive resistance is encountered, an open thermocouple input condition is reported.

Input Connector Assembly 2-16.

The following paragraphs briefly describe the major sections of the Input Connector PCA, which is used for connecting most of the analog inputs to the instrument.

20 CHANNEL TERMINALS 2-17.

Twenty HI and LO terminal blocks are provided in two rows, one for channels 1 through 10 and one for channels 11 through 20. The terminals can accommodate a wide range of wire sizes. The two rows of terminal blocks are maintained very close to the same temperature for accurate thermocouple measurements.

REFERENCE JUNCTION TEMPERATURE 2-18.

A semiconductor junction is used to sense the temperature of the thermocouple input terminals. The resulting dc output voltage is proportional to the block temperature and is sent to the A/D Converter PCA for measurement.

Display PCA 2-19.

The Display Assembly controller communicates with the main Microprocessor over a three-wire communication channel. Commands from the Microprocessor inform the Display Controller how to modify its internal display memory. The Display Controller then drives the grid and anode signals to illuminate the required segments on the Display. The A2 Display Assembly requires power supply voltages from the Power Supply and a clock signal from the A1U4 Microprocessor.

Memory PCA (2625A only) 2-20.

The Memory PCA is used by the Digital Kernel to store nonvolatile measurement data. This block requires power supply voltages from the Power Supply, a reset signal from the Display PCA, and signals from the Digital Kernel.

IEEE-488 Option (-05) 2-21.

Theory of operation for the IEEE-488 Option (-05) is presented in Section 7 of this manual. The related schematic diagram is found in Section 8.

DETAILED CIRCUIT DESCRIPTION 2-22.

Main PCA 2-23.

The following paragraphs describe the operation of the circuits on the Main PCA. The schematic for this pca is located in Section 8.

POWER SUPPLY CIRCUIT DESCRIPTION 2-24.

The Hydra power supply consists of three major sections:

- Raw DC Supply

  The raw dc supply converts line voltage (90V to 264V ac) to a dc output of 7.5V to 35V.

- 5V Switcher Supply

  The 5V switching supply regulates the 7.5 to 35V dc input to a nominal 5.1V ±0.25V dc (VCC).

- Inverter

  Using the 5V switching supply output, the inverter generates the -30V dc, -5V dc, and 5.4V ac supply levels needed for the vacuum-fluorescent display and the RS-232 Interface. The inverter also provides isolated +5.3V (VDD), +5.6V (VDDR), and -5.4V (VSS) outputs for the inguard circuitry.

Raw DC Supply 2-25.

The raw dc supply circuitry receives input from power transformer T401, which operates on an input ranging from 90V to 264V ac. The power transformer is energized whenever the power cord is plugged into the ac line; there is no on/off switch on the primary side of the transformer. The transformer has an internal 275V ac metal-oxide varistor (MOV) to clamp line transients. The MOV normally acts as an open circuit. When the peak voltage exceeds approximately 400V, the line impedance in series with the line fuse limits transients to approximately 450V. All line voltages use a slow blow 0.125 A, 250V fuse.

On the secondary side of the transformer, rectifiers A1CR2, A1CR3, and capacitor A1C7 rectify and filter the output. When it is ON, switch A1S1 (the front panel POWER switch) connects the output of the rectifiers to the filter capacitor and the rest of the instrument. Depending on line voltage, the output of the rectifiers is between 7.5 and 35V dc. Capacitor A1C2 helps to meet electromagnetic interference (EMI) and electromagnetic compatibility (EMC) requirements.

When external dc power is used, the power switch connects the external dc source to power the instrument. The external dc input uses thermistor A1RT1 (for overcurrent protection) and diode A1CR1 (for reverse input voltage protection.) Capacitor A1C59 helps meet EMI/EMC requirements. Resistor A1R48, capacitors A1C2 and A1C39 also ensure that the instrument meets EMI/EMC performance requirements.

Auxiliary 6V Supply 2-26.

Three-terminal regulator A1U19, voltage-setting resistors A1R44 and A1R46, and capacitor A1C34 make up the auxiliary 6-volt supply. This supply is used for the inverter oscillator, inverter driver, and the power fail detection circuits.

5V Switcher 2-27.

The 5V switcher supply uses a switcher supply controller/switch device A1U9 and related circuitry. The 7.5V dc to 35V dc input is regulated to 5.1V dc (VCC) through pulse-width modulation at a nominal switching frequency of 70 kHz.

The output voltage of the switcher supply is controlled by varying the duty cycle (ON time) of the switching transistor in the controller/switch device A1U9. A1U9 contains the supply reference, oscillator, switch transistor, pulse-width modulator comparator, switch drive circuit, current-limit comparator, current-limit reference, and thermal limit. Dual inductor A1T2 regulates the current that flows from the raw supply to the load as the switching transistor in A1U9 is turned on and off. Complementary switch A1CR10 conducts when the switching transistor is off.

The pulse-width modulator comparator in A1U9 compares the output to the reference and sets the ON-time/OFF-time ratio to regulate the output to 5.1V dc. A1C26 is the input filter capacitor, and A1C14 is the output filter capacitor. Proper inductor and capacitor values set the filter frequency response to ensure best overall system stability. Circuitry consisting of A1R27, A1C20, and A1C18 ensure that the switcher supply remains stable and operating in the continuous mode. Resistors A1R17, A1R23, A1R24, and A1R26 set the output voltage at 5.1V (either A1R17 or A1R23 may have been removed at the factory to adjust the output voltage of the supply to within 5% of 5.1V). A1R18 samples the raw supply voltage and injects a small correction to the output level and improves the line regulation over the very wide four-to-one dc input voltage range. Capacitor A1C21 sets the operating frequency of the switcher at approximately 70 kHz.

Resistors A1R29, A1R30, A1R31, A1R32, and A1R33 sense the output current of the switcher. The divided-down voltage produced from these sense resistors is connected to the current limit comparators (A1U9-9). When the peak current reaches approximately 3 amps, the switch transistor is turned off to limit the output current of the switcher supply.

Inverter 2-28.

The inverter supply uses a two transistor driven push-pull configuration. The center tap of transformer A1T1 primary is connected to the 5.1V dc VCC supply, and each side is alternately connected to common through transistors A1Q7 and A1Q8. A1R38 may be removed to disable the inverter supply for troubleshooting purposes. A1Q7 and A1Q8 are driven by the outputs of D flip-flop A1U22. Resistors A1R34 and A1R28, and diodes A1CR11 and A1CR12 shape the input drive signals to properly drive the gate of the transistors. D flip-flop A1U22 is wired as a divide-by-two counter driven by a 110-kHz square wave. The 110-kHz square wave is generated by hex inverter A1U23, which is connected as an oscillator with a frequency determined by the values of resistors A1R40 and A1R47 and capacitor A1C35. The resulting ac voltage produced across the secondary of A1T1 is rectified to provide the input to the inverter inguard and outguard supplies.

Inverter Outguard Supply 2-29.

The inverter outguard supply provides three outputs: 5.4V ac, -30V dc, and -5V dc. These voltages are required by the display and RS-232 drivers and receiver. The 5.4V ac supply comes off the secondary windings (pins 6 and 7) on transformer T1, and it is biased at -24V dc with zener diode A1VR3 and resistor A1R22. Dual diodes A1CR8 and A1CR9 and capacitor A1C17 are for the -30V dc supply. Capacitors A1C30 and A1C31, and dual diodes A1CR13 form a voltage doubler circuit that generates -12 volts. Three-terminal regulator A1U18 then regulates this voltage down to -5V for the RS-232 circuit. Capacitor A1C32 is needed for transient response performance of the three-terminal regulator.

Inverter Inguard Supply 2-30.

The inverter inguard supply provides three outputs: +5.3V dc (VDD) and -5.4V dc (VSS) for the inguard analog and digital circuitry, and +5.6V dc (VDDR) for the relays. Diodes A1CR5 and A1CR6, and capacitor A1C12 are for the +9.5 volt source, and diodes A1CR7 and capacitor A1C13 are for the -9.5V source.

Three-terminal regulator A1U6 regulates the 9.5V source to 5.6V for the relays. A1R5 and A1R6 set the output voltage at 5.6V. A1C6 is required for transient performance. The +5.3V regulator circuit uses A1Q2 for the series-pass element and A1Q4 as the error amplifier. A1VR2 is the reference for the positive supply. A1R14 provides the current to bias the reference zener. A1C4 is the output filter, and A1C9 provides frequency compensation of the regulator circuit. Transistor A1Q1 and resistor A1R13 make up the current-limit circuit.

When the voltage across A1R13 increases enough to turn on A1Q1, output current is limited by removing the base drive to A1Q2.

The -5.4 volt regulator operates like the +5.3 volt regulator, except that the NPN transistors in the positive supply are PNP transistors in the negative supply, and the PNP transistors in the positive supply are NPN transistors in the negative supply. If a VDD-to-VSS short circuit occurs, diode A1CR4 ensures that current limit occurs at the limit set for the -5.4V dc or +5.3V dc supply, whichever is lower.

Power Fail Detection 2-31.

The power fail detection circuit generates a signal to warn the Microprocessor that the power supply is going down. Comparator A1U24 compares the divided-down raw supply voltage and the band-gap generated reference voltage. When the raw supply voltage is greater than about 8V dc, the output of A1U24 is “high” and when the raw supply falls below 8V dc, the output goes “low”. Resistors A1R39 and A1R41 make up the divider, and resistor A1R43 provides bias for the band-gap reference. Resistor A1R42 is a pull up resistor for the comparator output, and resistor A1R45 provides positive feedback to provide the comparator with some hysteresis.

DIGITAL KERNEL 2-32.

The Digital Kernel is composed of the following eight functional circuit blocks: the Microprocessor, the ROM (Read-Only Memory), the NVRAM/Clock (Nonvolatile Random Access Memory and Real-Time Clock), the EEPROM (Electrically Erasable Programmable Read-Only Memory), the Counter/Timer, the RS-232 Interface, and the Option Interface.

Microprocessor 2-33.

The Microprocessor uses an eight-bit data bus and a sixteen-bit address bus to access memory locations in the ROM (A1U8), the NVRAM/Clock (A1U3), the Counter/Timer (A1U2), the Digital I/O Registers (A1U13, A1U16, A1U26), the Memory PCA (A6), and the IEEE-488 PCA (A5).

The Microprocessor oscillator operates at a 4.9152-MHz frequency determined by crystal A1Y1. The A1U4-68 system clock signal (the Microprocessor oscillator frequency divided by four) is a square wave with a frequency of 1.2288 MHz. This system clock also determines the memory cycle time of 0.813 microseconds. The system clock is also used by the Display Assembly and the IEEE-488 option assembly after being damped by series resistor A1R19 to minimize the EMI generated by this signal’s sharp edges.

When the address bus is stable, the Microprocessor enables either the reading of memory (by driving RD*, A1U4-67, low) or writing of memory (by driving WR*, A1U4-66, low.)

The Microprocessor uses a three-wire synchronous communication interface to store and retrieve instrument communication configuration and calibration information in the EEPROM (A1U1). See the EEPROM description for more detailed information.

The Microprocessor communicates to the Display Controller using another synchronous, three-wire communication interface described in detail in the Display Controller Theory of Operation in this section.

The Microprocessor communicates to the Microcontroller on the A/D Converter PCA (via the Serial Communication circuit) using an asynchronous communication protocol at 4800 baud. Communication to the Microcontroller (A3U9) originates at A1U4-11. Communication from the A/D's Microcontroller to the Microprocessor appears at A1U4-10. When there is no communication in progress between the Microprocessor and the Microcontroller, both of these signals are low.

Address Decoding 2-34.

The upper three bits of the address bus are decoded by A1U10-3,4,5 to generate the ROM* chip select signal for the ROM (A1U10-6).

The NVRAM/Clock chip select signal (A1U21-6 going low) is generated when the ROM* and RESET* signals are high and any one of address bits 9 through 12 is high. To avoid spurious write cycles during power cycling, the INT* output of the NVRAM (A1U3-1) is used to discharge the reset circuit on the Display PCA through resistor A1R63 when the power supply level at A1U3-28 is too low (less than approximately 4.65V dc) to allow memory operations to the NVRAM.

The miscellaneous I/O chip select (hexadecimal addresses 0000 through 01FF) is decoded using the ROM* signal and address bits 9 through 12 by A1U15 and A1U21. When ROM* is high and all four of the address bits are low, the I/O* signal (A1U21-8) is low. The I/O* signal and address bits 3 through 8 are then used by A1U10 and A1U11 to generate the CNTR*, DIO*, IEEE*, and MEM* chip select signals.

Table 2-1 shows a memory map for the Microprocessor.

Table 2-1. Microprocessor Memory Map

HEXADECIMAL ADDRESS	DEVICE SELECTED
2000 - FFFF	ROM (A1U8)
1FF8 - 1FFF	Real-Time Clock (A1U3)
0200 - 1FF7	NVRAM (A1U3)
0040 - 013F	Microprocessor Internal RAM
0038 - 003F	Counter/Timer (A1U2)
0032 (Read Only)	Digital Inputs (A1U13)
0032 (Write Only)	Digital Outputs (A1U26)
0035 (Write Only)	Alarm Outputs (A1U16)
0028 - 002F	IEEE-488 Option (2620A Only)
0005 - 0006 (Write Only)	Memory Page (2625A Only)
0004	Memory Data (2625A Only)

Serial Communication (Guard Crossing) 2-35.

The transmission of information from the Microprocessor (A1U4) to the Microcontroller (A3U9) is accomplished via the circuit made up of A1U15, A1U7, A1R8, A1R16, and A3R8. The transmit output from the Microprocessor (A1U4-11) is inverted by A1U15, which drives the optocoupler LED (A1U7-2). Resistor A1R8 limits the current through the LED.

The phototransistor in A1U7 responds to the light emitted by the LED when A1U7-2 is driven low (the collector of the phototransistor (A1U7-5) goes low.) The phototransistor collector is pulled up by A3R8 on the A/D Converter PCA. When turning off, the phototransistor base discharges through A1R16. With this arrangement, the rise and fall times of the phototransistor collector signal are nearly symmetrical.

The transmission of data from the Microcontroller (A3U9) to the Microprocessor (A1U4) is accomplished via the circuit made up of A3Q1, A3R7, A1U5, A1R7, and A1R3. The transmit output from the Microcontroller (A3U9-14) is inverted by A3Q1, which drives the optocoupler LED (A1U5-2) through resistor A3R7. The current through the LED is limited by resistor A3R7. The phototransistor in A1U5 responds to the light emitted by the LED when A1U5-2 is driven low; the emitter of the phototransistor (A1U5-4) goes high. The phototransistor collector (A1U5-5) is pulled up by VCC, and the emitter is pulled down by resistor A1R3. When turning off, the phototransistor base discharges through A1R7. With this arrangement, the rise and fall times of the phototransistor collector signal are nearly symmetrical.

Display/Keyboard Interface 2-36.

The Microcontroller sends information to the Display Processor via a three-wire synchronous communication interface. The detailed description of the DISTX, DISRX, and DSCLK signals may be found in the detailed description of the Display PCA. Note that the DISRX signal is pulled down by resistor A1R1 so that Microprocessor input A1U4-15 is not floating at any time. The Display PCA also provides the system reset circuitry and watchdog timer.

The Keyboard interface is made up of six bidirectional port lines from the Microcontroller. SWR1 through SWR6 (A1U4-21 through A1U4-26, respectively) are pulled up by A2Z1 on the Display PCA. The detailed description of the Display PCA describes how the Microprocessor interfaces to the Keyboard.

ROM 2-37.

The ROM provides the instruction storage for the Microprocessor. The chip select for this device (A1U8-20) goes low for any memory cycle between hexadecimal addresses 2000 and FFFF (accessing 56 kbytes). Whenever this device is chip selected for read, the instruction in the addressed location is output to the data bus and read by the Microprocessor.

NVRAM/Clock 2-38.

The NVRAM/Clock (A1U3) provides the data storage and real-time clock for the instrument. A lithium battery, a crystal, and an automatic power-fail control circuit are also integrated into this single package. When the RAM* chip select signal (A1U3-20) is low, the Microprocessor is accessing one of the 8192 bytes in the NVRAM/Clock. The RD* (A1U3-22) and WR* (A1U3-27) signals go low to indicate a read or write cycle, respectively.

The internal power-fail control circuit disables access to this device and drives the INT* output (A1U3-1) low when the VCC power supply is below approximately +4.5V dc. This action keeps locations in the NVRAM/Clock from being modified while the instrument is powering up and down. When the INT* output is low, the reset circuit on the Display PCA is discharged, and a system reset occurs. Therefore, the Microprocessor is reset on power failure as soon as it can no longer access the NVRAM/Clock.

The NVRAM contains 8184 bytes of nonvolatile data storage. The nonvolatile instrument configuration information, the nonvolatile measurement data, and the Microprocessor temporary data are stored in this area.

The Clock is composed of 8-byte wide registers that allow access to the real-time clock counters. The Microprocessor accesses these registers in the same way as the NVRAM.

EEPROM 2-39.

The EEPROM contains 64 registers, each of which is 16 bits long. These registers are used to provide nonvolatile storage of some of the instrument configuration information and all of the calibration information. When the Microprocessor is communicating to the EEPROM, Chip Select input (A1U1-1) is driven high to enable the EEPROM interface.

When the Microprocessor is reading data from the EEPROM, the data bits are serially shifted out on the Data Out signal (A1U1-4) with each one-to-zero transition of the Serial Clock (A1U1-2).

When the Microprocessor is writing commands and data to the EEPROM, the bits are serially shifted into the EEPROM on the Data In signal (A1U1-3) with each zero-to-one transition of the Serial Clock (A1U1-2). When the last data bit for an erase or write operation is shifted into the EEPROM, the Microprocessor pulses the Chip Select input (A1U1-1) low to start the operation. The EEPROM will then drive the Data Out signal (A1U1-4) low to indicate that it is busy writing the register. The Data Out signal goes high when the operation is complete. Since the Microprocessor waits for this signal to go high before doing anything else, an EEPROM failing to drive this signal high causes the Microprocessor to wait until the Watchdog Timer on the Display PCA resets the instrument.

The Chip Select input (A1U1-1) is always set low at the end of each EEPROM operation.

Counter/Timer 2-40.

The Counter/Timer IC (A1U2) has three 16-bit counters that are used both to implement the Totalizer function and to provide a periodic 50-millisecond interrupt used for interval time operation.

The output from the Totalizer Input circuit (A1U28-3) provides the clock input for Counter 2. Counter 2 operates as a 16-bit pre-loadable down counter for the Totalizer function. This counter causes the IRQ1* interrupt (A1U2-9) to go low, interrupting the Microprocessor when the counter value changes from hexadecimal 0000 to FFFF. The Counter 2 Gate input (A1U2-2) must be low for the Totalizer to operate correctly.

Counter 3 is used as a periodic 50.0-millisecond interrupt source. This counter divides the E clock input (A1U2-17) by 61440. The IRQ1* interrupt (A1U2-9) goes low (interrupting the Microprocessor) at the end of each 50.0-millisecond period. The Counter 3 Gate input (A1U2-5) and the Counter 3 Clock input (A1U2-7) should both be low for this counter to operate correctly. The 10-Hz square wave signal observed on the Counter 3 Output pin (A1U2-6) changes state every 50.0 milliseconds.

Counter 1 is not used in the instrument, but its Clock and Output pins have been connected to available pins on the Option Interface.

RS-232 Interface 2-41.

The RS-232 interface is composed of connector A1J4, RS-232 Driver/Receiver A1U25, and the hardware serial communication interface (SCI) in Microprocessor A1U4.

The SCI transmit signal (A1U4-14) goes to the RS-232 driver (A1U25-12), where it is inverted and level shifted so that the RS-232 transmit signal transitions between approximately +5.0 and -5.0V dc. When the instrument is not transmitting, the driver output A1U25-5 is approximately -5.0V dc. The RS-232 receive signal from A1J4 goes to the RS-232 receiver A1U25-4, which inverts and level shifts the signal so that the input to the SCI transitions between 0 and +5.0V dc. When nothing is being transmitted to the instrument, the receiver output (A1U25-13) is +5.0V dc.

Data Terminal Ready (DTR) is a modem control signal controlled by the Microprocessor. When the instrument is powered up, the Microprocessor port pin (A1U4-32) goes high, which results in the RS-232 driver output (A1U25-7) going to -5.0V dc. When the instrument has initialized the SCI and is ready to receive and transmit, A1U4-32 will go low, resulting in the RS-232 DTR signal (A1U25-7) going to +5.0V dc. The RS-232 DTR signal remains at +5.0V dc until the instrument is powered down.

Option Interface 2-42.

The interconnection to the option slot is implemented by J1 on the Main PCA. This connector (A1J1) routes the outguard logic power supply (VCC and GND), the eight-bit data bus, RD*, WR*, E, RESET*, IEEE*, MEM*, and the lower three bits of the address bus to the option installed in the option slot. This connector also routes an interrupt signal from the IEEE-488 option to the IRQ2* input of the Microprocessor.

An option sense signal from the installed option allows the Microprocessor to identify the type of option. When the instrument is powered up, the type of PCA installed in the option slot is determined by the Microprocessor by driving the IRQ2* signal (A1U4-20) and sensing the activity on the OPS* signal (A1U4-29). The Microprocessor first sets IRQ2* low and samples the OPS* input, then sets IRQ2* high and samples the OPS* input again. Table 2-2 describes how this information is used to determine what hardware is installed in the option slot.

DIGITAL I/O 2-43.

The following paragraphs describe the Digital Input Threshold, Digital Input Buffers, Digital and Alarm Output Drivers, Totalizer Input, and External Trigger Input circuits.

Table 2-2. Option Type Sensing

	STATE OF *OPS INPUT FOR PCA:		
IRQ2* OUTPUT	NONE INSTALLED	IEEE-488	MEMORY
0	1	0	0
1	1	0	1

DIGITAL INPUT THRESHOLD 2-44.

The Digital Input Threshold circuit sets the input threshold level for the Digital Input Buffers and the Totalizer Input. A software programmable voltage divider (A1U17, A1R35, A1R36, A1R37) and a unity gain buffer amplifier (A1AR1) are the main components in this circuit. The Microprocessor sets outputs A1U16-15 and A1U16-12 to select one of four input threshold levels. These outputs control the resistive divider (A1R35, A1R36, A1R37) via two drivers with open-collector outputs in A1U17. The voltage from the divider is then buffered by A1AR1 which sets the input threshold. Capacitor A1C29 filters the divider voltage at the input of A1AR1. Table 2-3 defines the programmable input threshold levels.

The instrument selects the +1.4V dc threshold level at power-up initialization.

DIGITAL INPUT BUFFERS 2-45.

Since the eight Digital Input Buffers are identical in design, only components used for Digital Input 0 are referenced in this description. If the Digital Output Driver (A1U27-16) is off, the input to the Digital Input Buffer is determined by the voltage level at A1J5-10. If the Digital Output Driver is on, the input of the Digital Input Buffer is the voltage at the output of the Digital Output Driver.

The Digital Input Threshold circuit and resistor network A1Z1 determine the input threshold voltage and hysteresis for inverting comparator A1AR2. The inverting input of the comparator (A1AR2-2) is protected by a series resistor (A1Z3) and diode A1CR14. A negative input clamp circuit (A1Q9, A1Z2, and A1CR17) sets a clamp voltage of approximately +0.7V dc for the protection diodes of all Digital Input Buffers. A negative input voltage at A1J5-10 causes A1CR14 to conduct current, clamping the comparator input A1AR2-2 at approximately 0V dc.

The input threshold of +1.4V dc and a hysteresis of +0.5V dc are used for all Digital Input Buffers. When the input of the Digital Input Buffer is greater than approximately +1.65V dc, the output of the inverting comparator is low. When the input then drops below about +1.15V dc, the output of the inverting comparator goes high.

DIGITAL AND ALARM OUTPUT DRIVERS 2-46.

Since the 12 Digital Output and Alarm Output Drivers are identical in design, the following example description references only the components that are used for Alarm Output Driver 0.

The Microprocessor controls the state of Alarm Output Driver 0 by writing to latch output A1U16-2. When A1U16-2 is set high, the output of the open-collector Darlington driver (A1U17-15) sinks current through current limiting resistor A1R62. When A1U16-2 is set low, the driver output turns off and is pulled up by A1Z2 and/or the voltage of the external device that the output is driving. If the driver output is driving an external inductive load, the internal flyback diode (A1U17-9) conducts the energy into MOV A1RV1 to keep the driver output from being damaged by excessive voltage. Capacitor A1C58 ensures that the instrument meets electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance requirements.

Table 2-3. Programmable Input Threshold Levels

A1U16-15	A1U16-12	INPUT THRESHOLD VOLTAGE
0	0	+2.5V dc
0	1	+0.7V dc
1	0	+1.4V dc
1	1	+0.7V dc

TOTALIZER INPUT 2-47.

The Totalizer Input circuit consists of Input Protection, a Digital Input Buffer circuit, and a Totalizer Debouncer circuit. The Digital Input Buffer for the totalizer is protected from electrostatic discharge (ESD) damage by A1R49 and A1C43. Refer to the detailed description of the Digital Input Buffer circuit for more information.

The Totalizer Debounce circuit allows the Microprocessor to select totalizing of either the input signal or the debounced input signal. Latch output A1U16-16 is set low by A1U4 to totalize the unmodified input signal or high to totalize the debounced input signal. This totalizer clock control is provided by A1U28; output A1U28-3 drives the totalizer counter clock input (A1U2-4).

The actual debouncing of the input signal is accomplished by A1U14, A1U20, and A1U29. An EXOR gate compares the input signal (A1U14-13) and the output of an eight-bit shift register (A1U29-9). If these signals differ, EXOR gate output A1U14-11 goes high, enabling counter A1U20 and shift register A1U29. The counter divides the system clock of 1.2288 MHz (A1U20-10) by 256 to yield a 4.8-kHz clock (A1U20-13). This signal clocks the eight-bit shift register. After approximately 1.5625 milliseconds, the input signal will have been shifted from the serial input (A1U29-10) through to the eighth output bit (A1U29-9). This forces the counter and shift register to stop. If the input signal changes state before 1.5625 milliseconds have elapsed, the counter is cleared and the shift register is preloaded again. Therefore, the input signal must remain stable for greater than 1.5625 milliseconds before that transition changes the state of the clock input of the totalizer counter (A1U2-4).

EXTERNAL TRIGGER INPUT CIRCUITS 2-48.

The External Trigger Input circuit can be configured by the Microprocessor to interrupt on a rising or falling edge of the XT* input (A1J6-2) or to not interrupt on any transitions of the XT* input.

The Microprocessor sets latch output A1U16-19 high for falling edge detection and low for rising edge detection of the XT* input. The Microprocessor can enable the external trigger interrupt by setting port pin A1U4-28 high or disable the interrupt by setting it low. Microprocessor port pin A1U4-28 should only be high if the instrument trigger mode of "ON" has been selected. Resistor A1R20 pulls NAND gate input A1U13 low during power-up to ensure that the external trigger interrupt input (A1U4-9) is high.

When the EXOR gate output (A1U14-3) goes high, and NAND gate input A1U12-13 is high, the output of the NAND gate (A1U12-11) goes low to interrupt the Microprocessor. The Microprocessor can also determine the state of the XT* input by reading the TRIG signal on port pin A1U4-27.

The XT* input is pulled up to +5V dc by A1Z2 and is protected from damage by ESD by A1R58, A1C54, A1Z3, and A1CR15. Capacitor A1C54 helps ensure that the instrument meets EMI/EMC performance requirements.

A/D Converter PCA 2-49.

The following paragraphs describe the operation of the circuits on the A/D Converter PCA. The schematic for this pca is located in Section 8.

ANALOG MEASUREMENT PROCESSOR 2-50.

Refer to Figure 2-3 for an overall picture of the Analog Measurement Processor chip and its peripheral circuits. Table 2-4 describes Analog Measurement Processor chip signal names.

The Analog Measurement Processor (A3U8) is a 68-pin CMOS device that, under control of the A/D Microcontroller (A3U9), performs the following functions:

- Input signal routing
- Input signal conditioning
- Range switching
- Passive filtering of dc voltage and resistance measurements
- Active filtering of ac voltage measurements
- A/D conversion
- Support for direct volts, true rms ac volts, temperature, resistance, and frequency measurements

Two separate signal paths are used, one for dc/ohms/temperature and one for ac. The volts dc (3V range and below) and temperature voltages are coupled directly to the a/d converter, while higher voltages are attenuated first. For ohms, the dc circuitry is augmented with an internal ohms source voltage regulator controlled through an extra set of switches. For volts ac, inputs are routed through the ac buffer, which uses the gain selected by the Measurement Processor (A3U8).

The a/d converter uses a modified dual-slope minor cycle method. The basic measurement unit, a minor cycle, consists of a fixed time integrate period for the unknown input, a variable time reference integrate period, a variable time hold period, and various short transition periods. A minor cycle period lasts for 25 ms or until a new minor cycle is begun, whichever comes first.

INPUT PROTECTION 2-51.

The instrument measurement circuits are protected when overvoltages are applied through the following comprehensive means:

- Any voltage transients on channel 0 HI or LO terminals are immediately clamped to a peak of about 1800V or less by MOVs A3RV1 and A3RV2. (This is much lower than the 2500V peaks that can be expected on 240 VAC, IEC 664 Installation Category II, ac mains.)
- Fusible resistors A3R10 and A3R11 protect the measurement circuitry in all measurement modes by limiting currents.
- A3Q11 clamps voltages exceeding 0.7V below and approximately 6.0V above analog common (LO) or LO SENSE, with A3R35 limiting the input current.

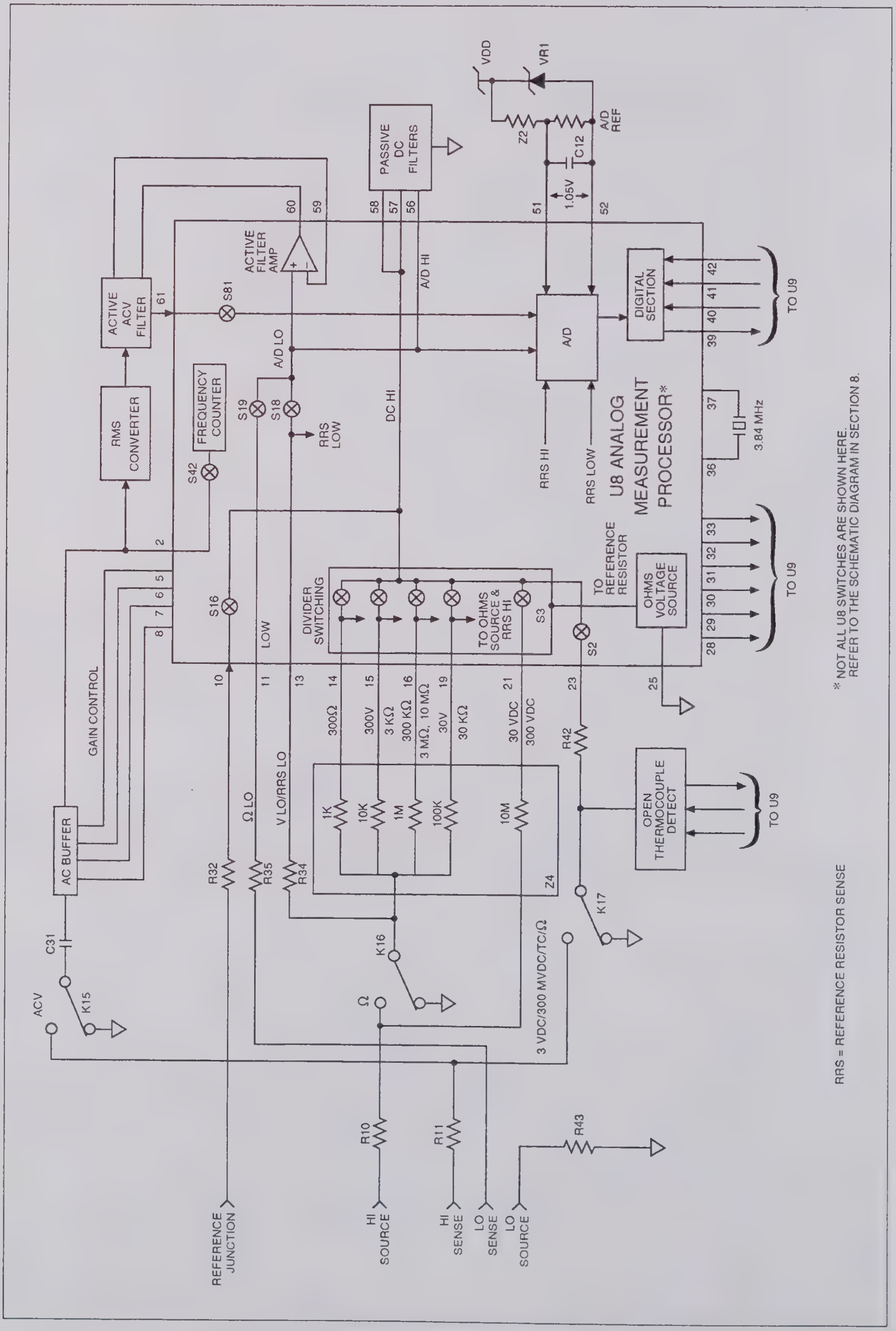

ACTIVE ACV FILTER
RMS CONVERTER
FREQUENCY COUNTER
ACTIVE FILTER AMP
PASSIVE DC FILTERS
VDD
VR1
Z2
C12
A/D REF
1.05V
A/D
DIGITAL SECTION
TO U9
U8 ANALOG MEASUREMENT PROCESSOR*
RRS HI
RRS LOW
3.84 MHz
OHMS VOLTAGE SOURCE
TO REFERENCE RESISTOR
OPEN THERMOCOUPLE DETECT
DIVIDER SWITCHING
TO OHMS SOURCE & RRS HI
S3
S2
S16
S18
S19
S42
S81
A/D LO
A/D HI
DC HI
LOW
RRS LOW
GAIN CONTROL
AC BUFFER
C31
ACV
K15
K16
K17
Ω
Ω LO
V LO/RRS LO
R32
R35
R34
R42
R43
R10
R11
Z4
1K
10K
1M
100K
10M
300Ω
300V
3 KΩ
300 KΩ
3 MΩ, 10 MΩ
30V
30 KΩ
30 VDC
300 VDC
3 VDC/300 MVDC/TC/Ω
2
5
6
7
8
10
11
13
14
15
16
19
21
23
25
28
29
30
31
32
33
36
37
39
40
41
42
51
52
56
57
58
59
60
61
REFERENCE JUNCTION
HI SOURCE
HI SENSE
LO SENSE
LO SOURCE
* NOT ALL U8 SWITCHES ARE SHOWN HERE. REFER TO THE SCHEMATIC DIAGRAM IN SECTION 8.
RRS = REFERENCE RESISTOR SENSE

Figure 2-3. Analog Simplified Schematic Diagram

Table 2-4. Analog Measurement Processor Pin Descriptions

PIN	NAME	DESCRIPTION
1	VDD	+5.4V supply
2	ACBO	AC buffer output
3	AIN	(not used)
4	AGND2	Analog ground
5	ACR4	AC buffer range 4 (300V)
6	ACR3	AC buffer range 3 (30V)
7	ACR2	AC buffer range 2 (3V)
8	ACR1	AC buffer range 1 (300 mV)
9	VSSA	-5.4V supply for AC ranging
10	REFJ	Reference junction input
11	DCV LOW	A/D converter low input
12	GRD	Driven guard
13	RRS	Reference resistor sense for ohms
14	V4	Tap #4 on the DCV input divider/ohms reference network
15	V3	Tap #3 on the DCV input divider/ohms reference network
16	V1	Tap #1 on the DCV input divider/ohms reference network
17	GRD	Driven guard
18	V2F	Tap #2 input on the DCV input divider/ohms reference network
19	V2	Tap #2 on the DCV input divider/ohms reference network
20	GRD	Driven guard
21	V0	Tap #0 on the DCV input divider/ohms reference network
22	GRD	Driven guard
23	OVS	Ohms and volts sense input
24	GRD	Guard
25	AGND1	Analog ground
26	-	(not used)
27	DGND	Analog ground
28	FC0	Function control #0
29	FC1	Function control #1
30	FC2	Function control #2
31	FC3	Function control #3
32	FC4	(not used)
33	FC5	(not used)
34	FC6	Function control #6
35	FC7	Function control #7
36	XIN	Crystal oscillator input
37	XOUT	Crystal oscillator output
38	MRST	Master reset
39	AS	Analog send
40	AR	Analog receive
41	SK	Serial clock
42	CS	Chip select
43	BRS	(not used)
44	VSS	-5.4V dc
45	INT	Integrator output

Table 2-4. Analog Measurement Processor Pin Descriptions (cont)

PIN	NAME	DESCRIPTION
46	SUM	Integrator summing node
47	B.1	Buffer output, 100 mV range
48	B.32	Buffer output, 300 mV range
49	B1	Buffer output, 1000 mV range
50	B3.2	Buffer output, 3V range
51	VREF+	A/D voltage reference plus
52	VREF-	A/D voltage reference minus
53	RAO	A/D reference amplifier output
54	RA+	A/D reference amplifier noninverting input
55	RA-	A/D reference amplifier inverting input
56	AFO	Passive filter 2
57	MOF	Passive filter 1 plus resistance
58	AFI	Passive filter 1
59	FAI	Filter amplifier inverting input
60	FAO	Filter amplifier output
61	RMSF	RMS output, filtered
62	AGND3	(not used, connected to filtered -5.4V dc)
63	RMSG2	(not used)
64	RMSO	RMS converter output
65	CAVG	(not used)
66	VSSR	-5.4V dc, filtered
67	RMSG1	(not used, pulled to filtered -5.4V dc)
68	RMSI	(not used)

- A3Q10 clamps voltages during ohms measurements with A3RT1, A3R34, A3R10, and A3Z4 limiting the input current. With large overloads, thermistor A3RT1 will heat up and increase in resistance.
- A3U8 also clamps voltages on its measurement input pins that exceed the VDD and VSS supply rails. Resistors A3R42, A3R11, A3R10, A3RT1, A3Z4, A3R35, and A3R34 limit any input currents.
- Any excessive voltages that are clamped through A3U8 to VDD or VSS, are then also clamped by zener diodes A3VR3 and A3VR2.
- The open thermocouple detect circuitry is protected against voltage transient damage by A3Q14 and A3Q15.
- When measuring ac volts, the ac buffer is protected by dual-diode clamp A3CR1 and resistor network A3Z3.
- Switching induced transients are also clamped by dual-diode A3CR4 and capacitor A3C33, and limited by resistor A3R33.

INPUT SIGNAL CONDITIONING 2-52.

Each input is conditioned and/or scaled to a dc voltage appropriate for measurement by the a/d converter. DC voltage applied to the a/d converter can be handled on internal ranges of 0.1V, 0.3V, 1V, or 3V. Therefore, high-voltage dc inputs are scaled, and ohms inputs are converted to a dc voltage. Line voltage level ac inputs are first scaled and then converted to a dc voltage. Noise rejection is provided by passive and active filters.

Function Relays 2-53.

Latching relays A3K15, A3K16, and A3K17 route the input signal to the proper circuit blocks to implement the desired measurement function. These relays are switched when a 6-millisecond pulse is applied to the appropriate reset or set coil by the NPN Darlington drivers in IC A3U10. The A/D Microcontroller A3U9 controls the relay drive pulses by setting the outputs of port 6. Since the other end of the relay coil is connected to the VDDR supply, a magnetic field is generated, causing the relay armature and contacts to move to (or remain in) the desired position. Function relay states are defined in Table 2-5.

DC Volts and Thermocouples 2-54.

For the 3V and lower ranges (including thermocouples), the HI input signal is applied directly to the A3U8 analog processor through A3R11, A3K17, and A3R42. Capacitor A3C27 filters this input, which the analog processor then routes through S2 and other internal switches, through the passive filter, and to the internal a/d converter. The LO SENSE signal is applied to A3U8 through A3R35 and routed through internal switch A3U8-S19 to LO of the a/d converter.

Guard signals MGRD and RGRD are driven by an amplifier internal to A3U8 to a voltage appropriate for preventing leakage from the input HI signal under high humidity conditions.

For the 30V range, the HI signal is scaled by resistor network A3Z4. Here, the input is applied to pin 1 of A3Z4 so that an approximate 100:1 divider is formed by the 10-MΩ and 100.5-kΩ resistors in A3Z4 when analog processor switches S3 and S13 are closed. The attenuated HI input is then sent through internal switch S12 to the passive filter and the a/d converter. Input LO is sensed through analog processor switch S18 and resistor A3R34.

For the 300V range (Figure 2-4), the HI signal is again scaled by A3Z4. The input is applied to pin 1 of A3Z4, and a 1000:1 divider is formed by the 10-MΩ and 10.01-kΩ resistors when switches S3 and S9 are closed in A3Z4. The attenuated HI input is then sent through internal switch S10 to the passive filter and the a/d converter. LO is sensed through analog processor switch S18 and resistor A3R34.

Ohms and RTDs 2-55.

Resistance measurements are made using a ratio ohms technique, as shown in Figure 2-5. A stable voltage source is connected in series with the reference resistor in A3Z4 and the unknown resistor. Since the same current flows through both resistors, the unknown resistance can be determined by multiplying the ratio of the voltage drops across the reference and the unknown resistors by the known reference resistor value.

Table 2-5. Function Relay States

RELAY POSITION			
FUNCTION	A3K17	A3K16	A3K15
DC mV, 3V, Thermocouples	Reset	Set	Set
DC 30V, 300V	Set	Set	Set
ACV	Set	Set	Reset
Ohms, RTDs	Reset	Reset	Set
Frequency	Set	Set	Reset

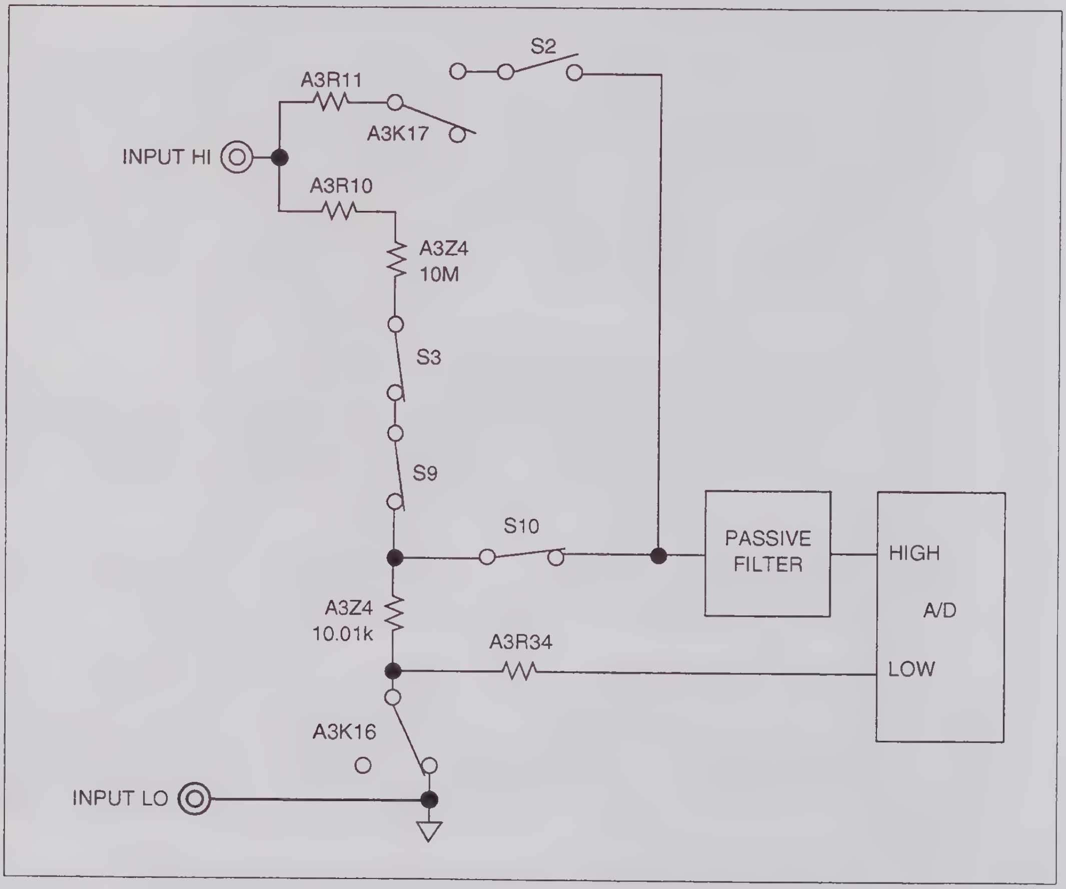
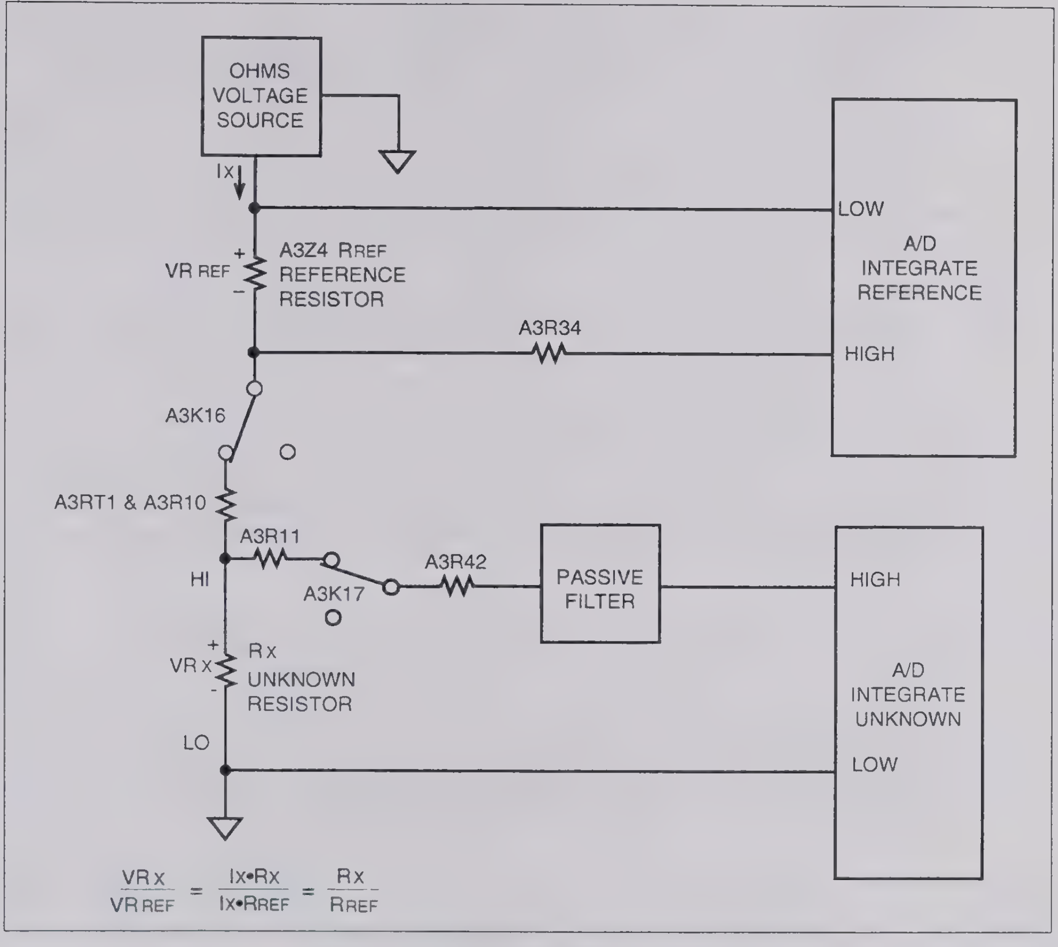


Figure 2-4. DC Volts 300V Range Simplified Schematic

For the RTD, 300Ω, 3-kΩ, and 30-kΩ ranges, the ratio technique is implemented by integrating the voltage across the unknown resistance for a fixed period of time and then integrating the negative of the voltage across the reference resistance for a variable time period. In this way, each minor cycle result gives the ratio directly.

For the 300-kΩ, 3-MΩ, and 10-MΩ ranges, the ratio is determined by performing two separate voltage measurements in order to improve noise rejection. One fixed-period integration is performed on the voltage across the unknown resistance, and the second integration is performed on the voltage across the reference resistance. The ratio of the two fixed-period voltge measurements is then computed by Microcontroller A3U9. The resistance measurement result is determined when A3U9 multiplies the ratio by the reference resistance value.

When an input is switched in for a measurement, the ohms source in Analog Processor A3U8 is set to the correct voltage for the range selected and is connected to the appropriate reference resistor in network A3Z4. A measurement current then flows through A3Z4, relay A3K16, thermistor A3RT1, resistor A3R10, the unknown resistance, A3R43, ground, and the ohms source.


OHMS VOLTAGE SOURCE
Ix
+
VR REF
−
A3Z4 RREF REFERENCE RESISTOR
A3R34
LOW
A/D INTEGRATE REFERENCE
HIGH
A3K16
A3RT1 & A3R10
A3R11
HI
A3K17
A3R42
PASSIVE FILTER
HIGH
+
VR X
-
Rx UNKNOWN RESISTOR
A/D INTEGRATE UNKNOWN
LO
LOW

$$\frac{VR_X}{VR_{REF}} = \frac{I_X \bullet R_X}{I_X \bullet R_{REF}} = \frac{R_X}{R_{REF}}$$

Figure 2-5. Ohms Simplified Schematic

The resulting voltage across the unknown resistance is integrated for a fixed period of time by the A/D Converter through the HI SENSE path of A3R11, A3K17, A3R42 and A3U8 switch S2, and the LO SENSE path of A3R35 and Analog Processor switch S19. Passive filtering is provided by A3C34, A3C27, and portions or all of the DC Filter block.

The voltage across the reference resistor for the 300Ω and RTD, 3-kΩ, and 30-kΩ ranges (the 1-kΩ, 10.01-kΩ, and 100.5-kΩ resistances in A3Z4, respectively) is integrated for a variable period of time until the voltage across the integrate capacitor reaches zero. For the 300Ω and RTD range, the reference resistor voltage is switched in through Analog Processor switch S6 and applied to the A/D Converter by switch S8. For the 3-kΩ range, switches S9 and S11 perform these functions, respectively. For the 30-kΩ range, switches S13 and S14 are used. For all ranges, the voltage is routed through A3R34 to the RRS input.

The reference resistor for the 300-kΩ, 3-MΩ, and 10-MΩ ranges is the 1-MΩ resistor in A3Z4, which is selected by S15. The voltage across this reference is integrated during its own minor cycle(s) and is switched to a passive filter and the A/D Converter by switches S1 and S18.

When 4-wire measurements are made on any of the six ranges, separate Source and Sense signal paths are maintained to the point of the unknown resistance. The 4-wire Source path measurement current is provided by the A3U8 ohms source through one of the A3U8 internal switches (S6, S9, S13, or S15) and the appropriate reference resistor in A3Z4. The current flows through relay A3K16, thermistor A3RT1, resistor A3R10, the HI Source instrument relay contacts (A3K1 - A3K3, A3K5 - A3K14), and the HI Source lead wire, to the unknown resistance to be measured. The current flows back through the LO Source lead wire, the LO Source path of the instrument relays (A3K1 - A3K3, A3K5 - A3K14), resistor A3R43, and analog ground, to the A3U8 ohms source.

The voltage that develops across the unknown resistance is sensed through the other 2 wires of the 4-wire set. HI is sensed through the HI Sense path made up of the users HI Sense lead wire, the HI Sense contacts in the instrument relays, resistor A3R11, relay A3K17, resistor A3R42, and Analog Processor A3U8 switch S2. LO is sensed through the users LO Sense lead wire, the LO Sense contacts in the instrument relays, protection resistor A3R35, and A3U8 switch S19.

Since virtually no current flows through the sense path, no error voltages are developed that would add to the voltage across the unknown resistance; this 4-wire measurement technique eliminates user lead-wire and instrument relay contact and circuit board trace resistance errors.

AC Volts 2-56.

AC-coupled ac voltage inputs are scaled by the ac buffer, converted to dc by a true rms ac-to-dc converter, filtered, and then sent to the a/d converter.

Refer to Figure 2-6. Input HI is switched to the ac buffer by dc-blocking capacitor A3C31, protection resistor A3R11, and latching relay A3K15. Resistor A3R44 and A3K15 act to discharge A3C31 between channel measurements. LO is switched to the A3U8 A/D Converter through A3R34 and S18.

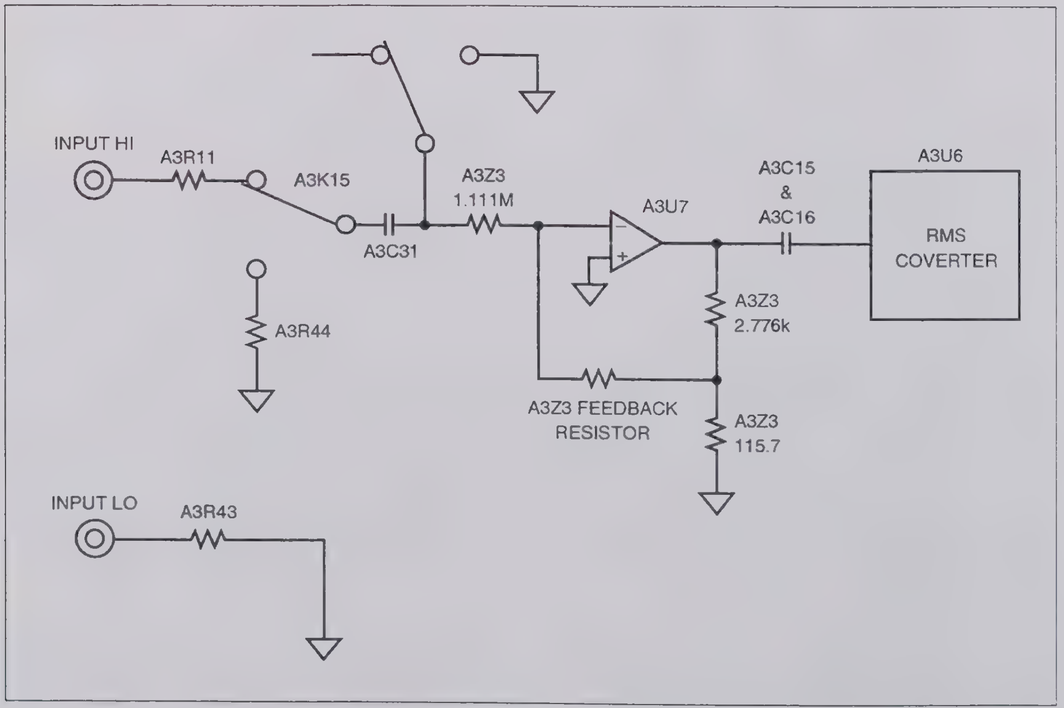


Figure 2-6. AC Buffer Simplified Schematic

JFETs A3Q3 through A3Q9 select one of the four gain (or attenuation) ranges of the buffer (wide-bandwidth op-amp A3U7.) The four JFET drive signals ACR1 through ACR4 turn the JFETs on at 0V and off at -VAC. Only one line at a time will be set at 0 volts to select a range.

The input signal to the buffer is first divided by 10, 100, or 1000 for the 300 mV, 3V, and 30V ranges, respectively. The resistance ratios used are summarized in Table 2-6. Note that the 111.1-kΩ resistor is left in parallel with the smaller (higher attenuation) resistors. The attenuated signal is then amplified by A3U7, which is set for a gain of 25 by the 2.776-kΩ and 115.7Ω resistors in A3Z3. Components A3R27 and A3C23 compensate high-frequency performance on the 300 mV range. For the 300V range, overall buffer gain is determined by the ratio of the 2.776-kΩ feedback resistor to the 1.111-MΩ input resistor.

The output of the buffer is ac-coupled by A3C15 and A3C16 to the true-rms ac-to-dc converter A3U6. Discharge JFET A3Q13 is switched on to remove any excess charge from the coupling capacitors A3C15 and A3C16 between channel measurements. A3C17 provides an averaging function for the converter, and resistor network A3Z1 divides the output by 2.5 before sending the signal to the active ac volts filter. Analog processor switch S81 connects the output of the active filter to HI of the A/D Converter.

Components A3R29, A3R30, A3C26, and A3C28 provide filtered power supplies (+VAC and -VAC) for the ac buffer, the ac switch JFETs, and the rms converter.

Frequency 2-57.

After any dc component is blocked by capacitors A3C15, A3C16, and A3C31, the output of the ac buffer is used to determine the input frequency. This signal is sent to the ACBO pin of analog processor A3U8 and switched to the internal frequency comparator and counter circuit by S42.

PASSIVE AND ACTIVE FILTERS 2-58.

The passive filters are used for the dc voltage and ohms measurements. For most ranges, capacitors A3C14 and A3C11 are switched into the measurement circuit in front of the A3U8 A/D Converter by switches S86, S87, and S88. These capacitors act with the 100-kΩ series resistance provided by A3R42 or A3Z4 to filter out high-frequency noise. For the 300-kΩ range, only A3C14 is switched in by switches S86 and S85. For the 3-MΩ and 10-MΩ ranges, A3C11 or A3C14 are not switched in to keep settling times reasonably short.

Between channel measurements, the passive filters are discharged by JFET A3Q2 under control of Microcontroller A3U9 through comparator A3U14. When the ZERO signal is asserted, A3R14 pulls the gate of A3Q2 to ground, turning the JFET on and discharging A3C11. At the same time, zeroing of filter capacitors A3C14 and A3C27 is accomplished by having the Analog Processor turn on internal switches S2, S86, and S87.

Table 2-6. AC Volts Input Signal Dividers

RANGE	DRIVE SIGNAL	A3Z3 DIVIDER RESISTOR(S)	OVERALL GAIN
300 mV	ACR1	111.1 kΩ	2.5
3V	ACR2	12.25 kΩ ll 111.1 kΩ	0.25
30V	ACR3	1.013 kΩ ll 111.1 kΩ	0.025
150/300V	ACR4	none	0.0025

The active filter is only used for ac voltage measurements. This three-pole active filter removes a significant portion of the ac ripple and noise present in the output of the rms converter without introducing any additional dc errors. The active filter op-amp within A3U8, resistors A3R20, A3R17, and A3R16, and capacitors A3C7, A3C10, and A3C6 form the filter circuit. This filter is referenced to the LO input to the a/d converter within A3U8 by the op-amp. The input to the filter is available at the RMSO pin, and the output is sent to the RMSF pin of A3U8. Switches S80 and S82, which are turned on prior to each new channel measurement, cause the filter to quickly settle (pre-charge) to near the proper dc output level.

A/D CONVERTER 2-59.

Figure 2-7 shows the dual slope a/d converter used in the instrument. The unknown input voltage is buffered and used to charge (integrate) a capacitor for an exact period of time. This integrator capacitor is then discharged by the buffered output of a stable and accurate reference voltage of opposite polarity. The capacitor discharge time, which is proportional to the level of the unknown input signal, is measured by the digital circuits in the Analog Measurement Processor. This time count becomes the conversion result.

In both the slow and fast measurement rates, the a/d converter uses its ±300 mV range for most measurement functions and ranges. The primary exceptions are that the 3V dc range is measured on the a/d converter 3V range, thermocouples are measured on the ±100 mV range, and the temperature reference is measured on the 1V a/d converter range. The typical overload point on a slow rate 30000 count range is 32000 display counts; the typical overload point on a fast rate 3000 count range is 3200 display counts.

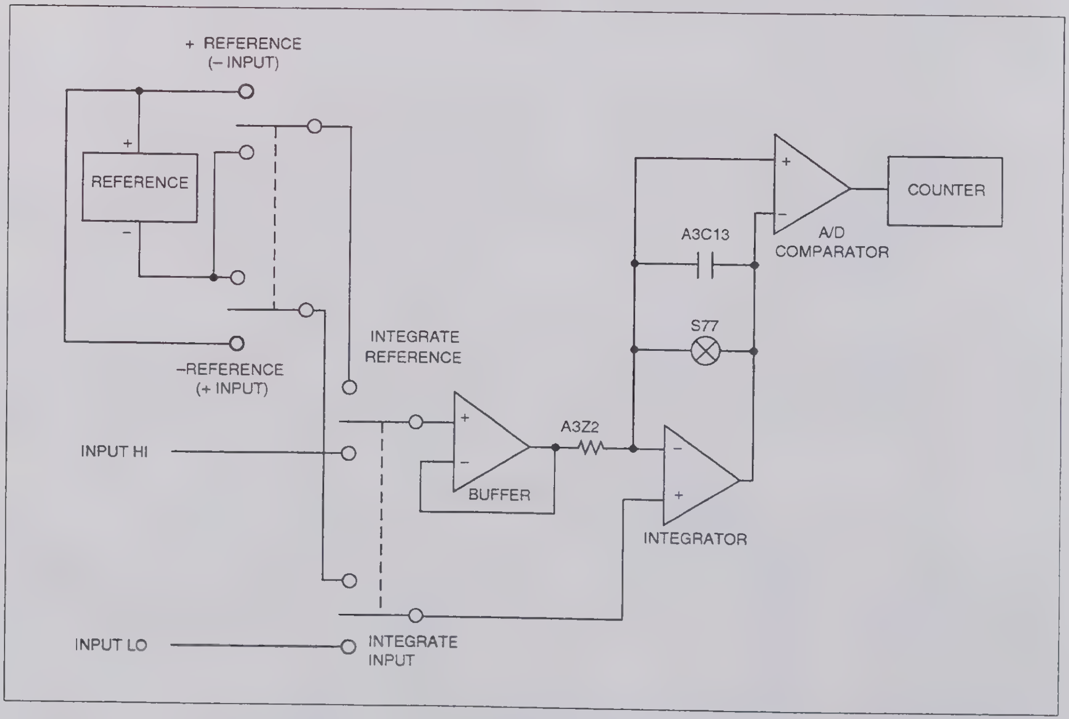


Figure 2-7. A/D Converter Simplified Schematic

During the integrate phase, the a/d buffer in the A3U8 Analog Measurement Processor applies the signal to be measured to one of the four integrator input resistors in network A3Z2. As shown on the A/D Converter schematic diagram in Section 8, the choice of resistor selects the a/d converter range. Switch S69 connects the buffer output through pin B.1 for the 100-mV range, S71 connects the output through B.32 for the 300 mV range, S73 connects to pin B1 for the 1V range, and S75 sets up the 3V range through pin B3.2.

The current through the selected integrator input resistor charges integrator capacitor A3C13, with the current dependent on the buffer output voltage. After the integrate phase, the buffer is connected to the opposite polarity reference voltage, and the integrator integrates back toward zero capacitor voltage until the comparator trips. An internal counter measures this variable integrate time. If the a/d converter input voltage is too high, the integrator overloads and does not return to its starting point by the end of the measurement phase. Switch S77 is then turned on to discharge integrate capacitor A3C13.

The reference voltage used during the variable integrate period for voltage (and high ohms) conversions is generated from zener reference diode A3VR1, which is time and temperature stable. The reference amplifier in the Analog Measurement Processor, along with resistors A3R15, A3R18, and A3R21, pulls approximately 2 mA of current through the zener. Resistors in network A3Z2 divide the zener voltage down to the reference 1.05V required by the A/D Converter.

INGUARD MICROCONTROLLER CIRCUITRY 2-60.

The Microcontroller, A3U9, with its internal program memory and RAM and associated circuitry, controls measurement functions on the A/D Converter PCA and communicates with the Main (outguard) processor.

The Microcontroller communicates directly with the A3U8 Analog Measurement Processor using the CLK, CS, AR, and AS lines and can monitor the state of the analog processor using the FC[0:7] lines. Filter zeroing is controlled by the ZERO signal. The open thermocouple detect circuitry is controlled by the OTCCLK and OTCEN lines and read by the OTC line. The Microcontroller also communicates with the Main (outguard) processor serially using the IGDR line to receive and the IGDS line (driven by A3Q1) to send.

The channel and function relays are driven to the desired measurement state by signals sent out through microcontroller ports 1, 3, 4, 6, and 7.

On power up, the reset/break detect circuit made up of quad comparator A3U1, capacitors A3C1 and A3C2, and resistors A3R1 through A3R6 and A3R8 resets the Microcontroller through the RESET* line. When a break signal is received from the outguard processor, the inguard A3U9 is again reset. Therefore, if Microcontroller operation is interrupted by line transients, the outguard can regain control of the inguard by resetting A3U9.

CHANNEL SELECTION CIRCUITRY 2-61.

Measurement input channel selection is accomplished by a set of latching 4-form-C relays organized in a tree structure. Relays A3K5, A3K6, and A3K8 through A3K14 select among channels 1 through 20. Relay A3K7 disconnects rear input channels 1 through 20 from the measurement circuitry between measurements. Relay A3K3 switches in the front panel channel 0 or the rear channels. Inductors A3L1 through A3L24 reduce EMI and current transients.

Selection between 2-wire and 4-wire operation for ohms measurements is performed by latching 2-form-C relays (A3K1 and A3K2.) These relays also serve to select a voltage or thermocouple rear input channel from either channels 1 through 10 or channels 11 through 20.

The coils for the relays are driven by the outputs of Darlington drivers A3U4, A3U5, A3U10, A3U11, and A3U12. The relays are switched when a 6-millisecond pulse is applied to the appropriate reset or set coil by the NPN Darlington drivers in these ICs. When the port pin of Microcontroller A3U9 connected to the input of a driver is set high, the output of the driver pulls one end of a relay set or reset coil low. Since the other end of the relay coil is connected to the VDDR supply, a magnetic field is generated, causing the relay armature and contacts to move to (or remain in) the desired position.

OPEN THERMOCOUPLE CHECK 2-62.

Immediately before a thermocouple measurement, the open thermocouple check circuit applies a small, ac-coupled signal to the thermocouple input. Microcontroller A3U9 initiates the test by asserting OTCEN, causing comparator A3U14/A3R40 to turn on JFET A3Q12. Next, the Microcontroller sends a 78-kHz square wave out the OTCCLK line through A3R41, A3Q12, and A3C32 to the thermocouple input. The resulting waveform is detected by A3U13 and A3CR2, and a proportional level is stored on capacitor A3C30. Op amp A3U13 compares this detected level with the VTH threshold voltage set up by A3R37 and A3R36 and stored on A3C29. If the resistance at the input is too large, the VTH level will be exceeded and the OTC (open thermocouple check) line will be asserted. After a short delay, the Microcontroller analyzes this OTC signal, determines whether the thermocouple should be reported as open, and deasserts OTCEN and sets OTCCLK high, ending the test.

Input Connector PCA 2-63.

The Input Connector assembly, which plugs into the A/D Converter PCA from the rear of the instrument, provides 20 pairs of channel terminals for connecting measurement sensors. This assembly also provides the reference junction temperature sensor circuitry used when making thermocouple measurements.

Circuit connections between the Input Connector and A/D Converter PCAs are made via connectors A4P1 and A4P2. Input channel and earth ground connections are made via A4P1, while temperature sensor connections are made through A4P2.

Input connections to channels 1 through 20 are made through terminal blocks TB1 and TB2. Channel 1 and 11 HI and LO terminals incorporate larger creepage and clearance distances and each have a metal oxide varistor (MOV) to earth ground in order to clamp voltage transients. MOVs A4RV1 through A4RV4 limit transient impulses to the more reasonable level of approximately 1800V peak instead of the 2500V peak that can be expected on 240 VAC, IEC 664 Installation Category II, ac mains. In this way, higher voltage ratings can be applied to channels 1 and 11 than can be applied to the other rear channels.

Strain relief for the user's sensor wiring is provided both by the Connector PCA housing and the two round pin headers. Each pin of the strain relief headers is electrically isolated from all other pins and circuitry.

Temperature sensor transistor A4Q1 outputs a voltage inversely proportional to the temperature of the input channel terminals. This voltage is 0.6V dc at 25 °C, increasing 2 mV with each degree decrease in temperature, or decreasing 2 mV with each degree increase in temperature. For high accuracy, A4Q1 is physically centered within and thermally linked to the 20 input terminals. Local voltage reference A4VR1 and resistors A4R1 through A4R3 set the calibrated operating current of the temperature sensor. Capacitor A4C1 shunts noise and EMI to ground.

Display PCA 2-64.

Display Assembly operation is classified into six functional circuit blocks: the Main PCA Connector, the Front Panel Switches, the Display, the Beeper Drive Circuit, the Watchdog Timer/Reset Circuit, and the Display Controller. These blocks are described in the following paragraphs.

MAIN PCA CONNECTOR 2-65.

The 20-pin Main PCA Connector (A2J1) provides the interface between the Main PCA and the other functional blocks on the Display PCA. Seven of the connector pins provide the necessary connections to the four power supply voltages (-30V dc, -5V dc, +5.1V dc, and 5.4V ac filament voltage). Six pins are used to provide the interface to the Front Panel Switches (A2SWR1 through A2SWR6). The other seven signals interface the Microprocessor (A1U4) to the Display Controller (A2U1) and pass the reset signals between the assemblies.

FRONT PANEL SWITCHES 2-66.

The Microprocessor scans the 19 Front Panel Switches (A2S1 through A2S18, and A2S21) using only six interface signals (plus the ground connection already available from the power supply). These six signals (SWR1 through SWR6) are connected to a bidirectional I/O port on the microprocessor. Each successive column has one less switch.

This arrangement allows the unused interface signals to function as strobe signals when their respective column is driven by the Microprocessor. The Microprocessor cycles through six steps to scan the complete Front Panel Switch matrix. Table 2-7 shows the interface signal state and, if the signal state is an output, the switches that may be detected as closed.

Table 2-7. Front Panel Switch Scanning

INTERFACE SIGNAL STATES OR KEY SENSED						
Step	SWR6	SWR5	SWR4	SWR3	SWR2	SWR1
1	A2S8	A2S17	A2S10	A2S12	A2S18	A2S13
2	A2S1	A2S2	A2S3	A2S4	A2S11	0
3	A2S7	A2S9	A2S5	A2S6	0	Z
4	A2S14	A2S15	A2S16	0	Z	Z
5	n/a	n/a	0	Z	Z	Z
6	A2S21	0	Z	Z	Z	Z

A2Sn indicates switch closure sensed.
0 indicates strobe driven to logic 0
Z indicates high impedance input; state ignored.

In step 1, six port bits are set to input, and the interface signal values are read. In steps 2 through 6, the bit listed as O is set to output zero, the other bits are read, and bits indicated by a Z are ignored.

Each of the interface signals is pulled up to the +5V dc supply by a 10-kΩ resistor in network A2Z1. Normally, the resistance between any two of the interface signals is approximately 20 kΩ. Checking resistances between any two signals (SWR1 through SWR6) verifies proper termination by resistor network A2Z1.

DISPLAY 2-67.

The custom vacuum-fluorescent display (A2DS1) comprises a filament, 11 grids (numbered 0 through 10 from right to left on the display), and up to 14 anodes under each grid. The anodes make up the digits and annunciators for their respective area of the display. The grids are positioned between the filament and the anodes.

A 5.4V ac signal, biased at a -24V dc level, drives the filament. When a grid is driven to +5V dc, the electrons from the filament are accelerated toward the anodes that are under that grid. Anodes under that grid that are also driven to +5V dc are illuminated, but the anodes that are driven to -30V dc are not. Grids are driven to +5V dc one at a time, sequencing from GRID(10) to GRID(0) (left to right, as the display is viewed.)

BEEPER DRIVE CIRCUIT 2-68.

The Beeper Drive circuit drives the speaker (A2LS1) to provide an audible response to a button press. A valid entry yields a short beep; an incorrect entry yields a longer beep.

The circuitry comprises a dual four-bit binary counter (A2U4) and a NAND gate (A2U6) used as an inverter. One four-bit free-running counter (A2U4) divides the 1.2288-MHz clock signal (E) from the microprocessor (A1U4) by 2 to generate the 614.4-kHz clock (CLK1) used by the Display Controller. This counter also divides the 1.2288-MHz clock by 16, generating the 76.8-kHz clock that drives the second four-bit binary counter (A2U4).

The second four-bit counter is controlled by an open-drain output on the Display Controller (A2U1-17) and pull-down resistor A2R1. When the beeper (A2LS1) is off, A2U1-17 is pulled to ground by A2R1. This signal is then inverted by A2U6, with A2U6-6 driving the CLR input high to hold the four-bit counter reset. Output A2U4-8 of the four-bit counter drives the parallel combination of the beeper (A2LS1) and A2R10 to ground to keep the beeper silent. When commanded by the Main Microprocessor, the Display Controller drives A2U1-17 high, enabling the beeper and driving the CLR input of the four-bit counter (A2U4-12) low. A 4.8-kHz square wave then appears at counter output A2U4-8 and across the parallel combination of A2LS1 and A2R10, causing the beeper to resonate.

WATCHDOG TIMER AND RESET CIRCUIT 2-69.

This circuit provides active high and active low reset signals to the rest of the system at a power-up or system reset if the Microprocessor does not communicate with the Display Processor for a 5-second period. The Watchdog Timer and Reset Circuit comprises dual retriggerable monostable multivibrator A2U5, NAND gates A2U6, diode A2CR3, and various resistive and capacitive timing components.

At power-up, capacitor A2C3 begins to charge up through resistor A2R3. The voltage level on A2C3 is detected by an input of Schmitt-Trigger NAND gate A2U6-12. The output of this gate (A2U6-11) then drives the active high reset signal (RESET) to the rest of the system. When the voltage on A2C3 is below the input threshold (typically +2.5V dc) of A2U6-12, A2U6-11 is high. As soon as A2C3 charges up to the threshold of A2U6-12, A2U6-11 goes low. The RESET signal drives NAND gate inputs A2U6-1 and A2U6-2 to generate the active low reset signal (RESET*) at A2U6-3.

When the RESET signal transitions from high to low (A2U5-1), the Watchdog Timer is triggered initially, causing A2U5-13 to go high. This half of the dual retriggerable monostable multivibrator uses timing components A2R2 and A2C2 to define a nominal 4.75-second watchdog timeout period. Each time a low-to-high transition of DISTX is detected on A2U5-2, capacitor A2C2 is discharged to restart the timeout period. If there are no low-to-high transitions on DISTX during the 4.75-second period, A2U5-13 transitions from high to low, triggers the other half of A2U5, and causes output A2U5-12 to go low. A2U5-12 is then inverted by A2U6 to drive the RESET signal high, causing a system reset. The low duration of A2U5-12 is determined by timing components A2Z1 and A2C4 and is nominally 460 µs. When A2U5-12 goes high again, RESET goes low to retrigger the Watchdog Timer.

DISPLAY CONTROLLER 2-70.

The Display Controller is a four-bit, single-chip microcomputer with high-voltage outputs that are capable of driving a vacuum-fluorescent display directly. The controller receives commands over a three-wire communication channel from the Microprocessor on the Main Assembly. Each command is transferred serially to the Display Controller on the display transmit (DISTX) signal, with bits being clocked into the Display Controller on the rising edges of the display clock signal (DSCLK). Responses from the Display Controller are sent to the Microprocessor on the display receive signal (DISRX) and are clocked out of the Display Controller on the falling edge of DSCLK.

Series resistor A2R11 isolates DSCLK from A2U1-40, preventing this output from trying to drive A1U4-16 directly. Figure 2-8 shows the waveforms during a single command byte transfer. Note that a high DISRX signal is used to hold off further transfers until the Display Controller has processed the previously received byte of the command.

Once reset, the Display Controller performs a series of self-tests, initializing display memory and holding the DISRX signal high. After DISRX goes low, the Display Controller is ready for communication; on the first command byte from the Microprocessor, the Display Controller responds with a self-test results response. If all self-tests pass, a response of 00000001 (binary) is returned. If any self-test fails, a response of 01010101 (binary) is returned. The Display Controller initializes its display memory to one of four display patterns depending on the states of the DTEST* (A2U1-41) and LTE* (A2U1-13) inputs. The DTEST* input is pulled up by A2Z1, but may be pulled down by jumpering A2TP4 to A2TP3 (GND). The LTE* input is pulled down by A2R12, but may be pulled up by jumpering A2TP5 to A2TP6 (VCC). The default conditions of DTEST* and LTE* cause the Display Controller to turn all segments on bright at power-up.

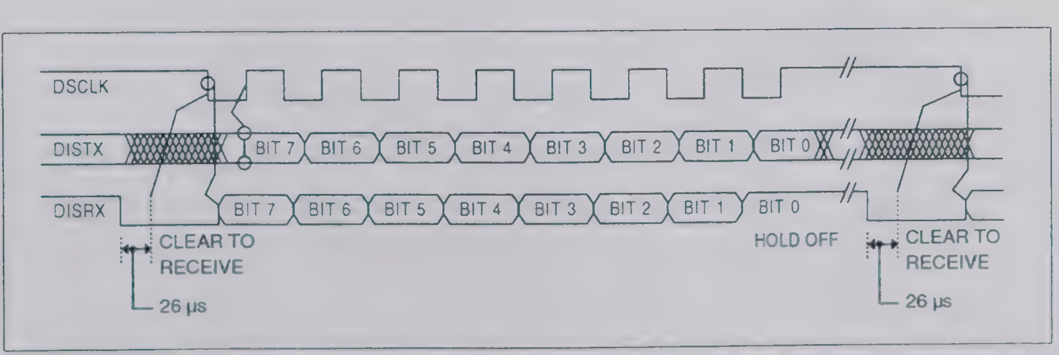


Figure 2-8. Command Byte Transfer Waveforms

Table 2-8 defines the logic and the selection process for the four display initialization modes.

The two display test patterns are a mixture of on and off segments forming a recognizable pattern that allows for simple testing of display operation. Test patterns #1 and #2 are shown in Section 5 of this manual.

The Display Controller provides 11 grid control outputs and 15 anode control outputs (only 14 anode control outputs are used). Each of these 26 high-voltage outputs provides an active driver to the +5V dc supply and a passive 220-kΩ (nominal) pull-down to the -30V dc supply. These pull-down resistances are internal to the Display Controller.

The Display Controller provides multiplexed drive to the vacuum-fluorescent display by strobing each grid while the segment data for that display area is present on the anode outputs. Each grid is strobed for approximately 1.14 milliseconds every 13.8 milliseconds, resulting in each grid on the display being strobed about 72 times per second. The grid strobing sequence is from GRID(10) to GRID(0), which results in left-to-right strobing of grid areas on the display. Figure 2-9 shows grid control signal timing.

Table 2-8. Display Initialization Modes

A2TP4 DTEST*	A2TP5 LTE*	Power-Up Display Initialization
1	1	All Segments OFF
1	0	All Segments ON (default)
0	1	Display Test Pattern #1
0	0	Display Test Pattern #2

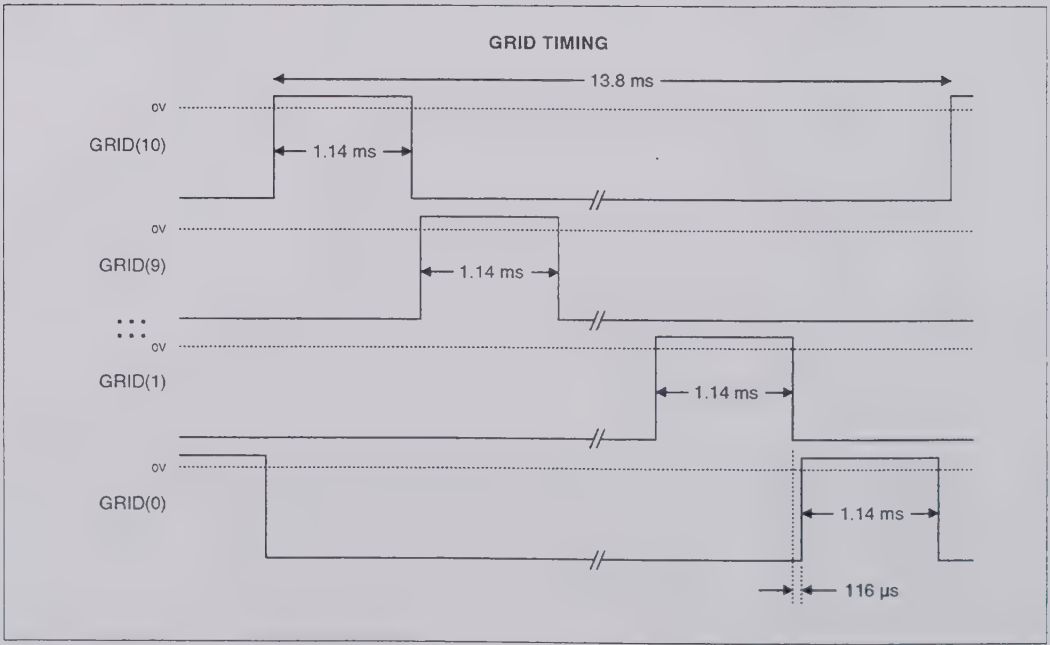


Figure 2-9. Grid Control Signal Timing

The single grid strobing process involves turning off the previously enabled grid, outputting the anode data for the next grid, and then enabling the next grid. This procedure ensures that there is some time between grid strobes so that no shadowing occurs on the display. A grid is enabled only if one or more anodes are also enabled. Thus, if all anodes under a grid are to be off, the grid is not turned on. Figure 2-10 describes the timing relationship between an individual grid control signal and the anode control signals.

Memory PCA (2625A only) 2-71.

The Memory PCA is a serially-accessed, byte-wide, nonvolatile 256K-byte memory that is capable of storing up to 2047 scans of data. The following paragraphs describe in detail the Main PCA Connector, Address Decoding, Page Register, Byte Counter, and Nonvolatile Memory blocks that make up this assembly.

MAIN PCA CONNECTOR 2-72.

The Memory PCA interfaces to the Main PCA through a 26-pin, right angle connector (A6J1). This connector routes the eight-bit data bus, the lower three bits of the address bus, memory control and address decode signals from the Main PCA to the Memory PCA. The Memory PCA is powered by the +5.1V dc power supply (VCC). The Memory PCA is sensed by the Microprocessor on the Main PCA through the connection of A6J1-11 to the option sense signal OPS* (A6J1-22).

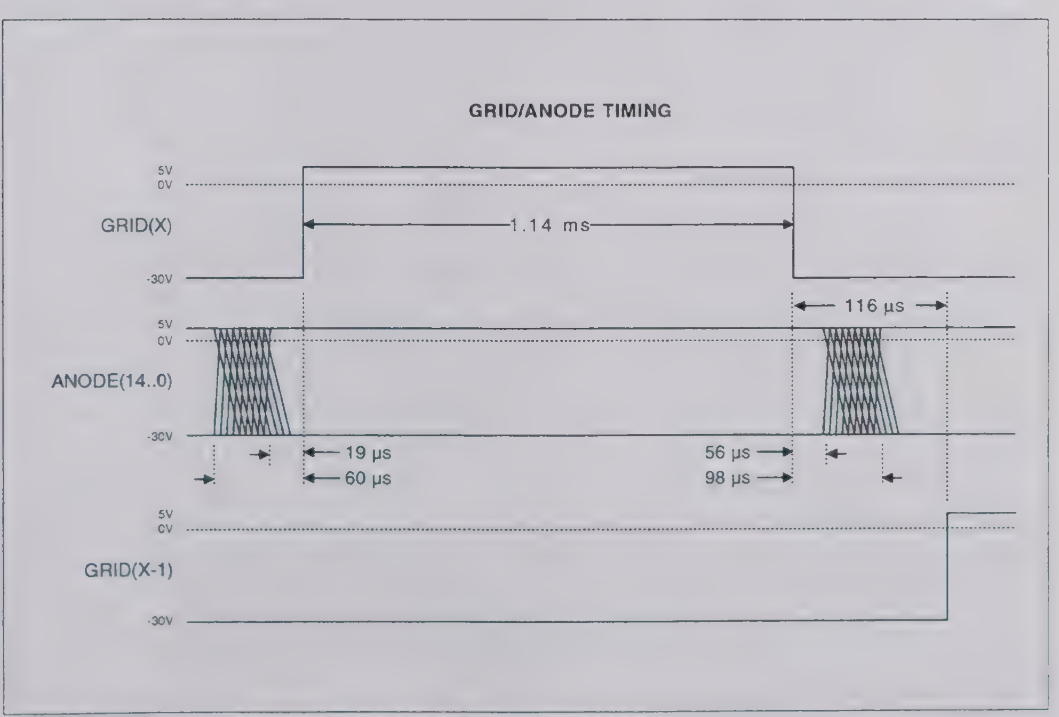


Figure 2-10. Grid-Anode Timing Relationships

ADDRESS DECODING 2-73.

Circuitry on the Main PCA decodes the Microprocessor address bus and provides the MEM* select signal to the Memory PCA. The 3-line to 8-line decoder (A6U8) is used to decode the three least significant address bits to get register select signals for hexadecimal addresses 4, 5, and 6. When the MEM* signal drives A6U8-4 low and the RESET* signal (A6U8-6) is high, the A0 through A2 address bits are decoded to get the MEMORY, PAGEL, and PAGEH register select signals. Address decoding is disabled when RESET* is low so that the Nonvolatile Memory cannot be accidentally modified during power-up or power-down.

PAGE REGISTER 2-74.

The Page Register is an 11-bit register that is writable by the Microprocessor on the Main PCA. The outputs of this register control the most significant address bits of the nonvolatile memories (A6U6 and A6U7.) When register select PAGEL goes high and the WE* signal is low, NAND gate output A6U2-3 goes high to latch the data bus into the lower part of the page register (A6U1). When register select PAGEH goes high and the WE* signal is low, NAND gate output A6U2-8 goes high to latch the lower three bits of the data bus into the high part of the page register (A6U4).

BYTE COUNTER 2-75.

The Byte Counter is a seven-bit ripple counter that controls the lower address bits of the nonvolatile RAMs. This counter is cleared when a new value is written to the lower page register. It automatically increments at the end of each read or write access to the memory data register.

NAND gate output A6U2-3 goes high to write the lower page register and clear the Byte Counter. When data is read from or written to the Non-Volatile Memory, NAND gate output A6U2-6 goes high during the memory cycle, and then low at the end of the memory cycle. The transition from high to low increments the Byte Counter so that the next access to the memory data register will be for the next sequential byte in the Non-Volatile Memory.

NONVOLATILE MEMORY 2-76.

The Non-Volatile Memory is made up of two 128K-byte static CMOS memories with integrated lithium battery, power-fail detection, and battery switching circuitry. When the VCC (+5.1V dc) power supply is above +4.5V dc, memories A6U6 and A6U7 are fully operational. When VCC drops below approximately +4.25V dc, all accesses to the memory are disabled by the internal power-fail detection circuit. When VCC drops below about +3.0V dc, the battery switching circuitry disconnects VCC and connects the lithium battery to the memory so that data is retained while the instrument power is off.

The most significant bit of the Page Register (A6U4-1,16) is gated with the MEMORY register select signal by A6U5 to get the memory chip select signals (A6U5-6 and A6U5-8). Memory pages 0 through 1023 are stored in memory device A6U7, and memory pages 1024 through 2047 are stored in memory device A6U6. The WR* and RD* control signals from the Microprocessor on the Main PCA are used to enable writing of data to and reading data from the memory devices, respectively.

IEEE-488 Interface (Option -05) 2-77.

Refer to Section 7 for detailed circuit descriptions of this option.

Section 2A

Theory of Operation (2635A)

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INTRODUCTION 2A-1.

The theory of operation begins with a general overview of the instrument and progresses to a detailed description of the circuits of each pca.

The instrument is first described in general terms with a Functional Block Description. Then, each block is detailed further (often to the component level) with Detailed Circuit Descriptions. Refer to Section 8 of this manual for full schematic diagrams. The Interconnect Diagram in this section (Figure 2A-1) illustrates physical connections among pca's.

Signal names followed by a '*' are active (asserted) low. All other signals are active high.

FUNCTIONAL BLOCK DESCRIPTION 2A-2.

Refer to Figure 2A-2, Overall Functional Block Diagram, during the following functional block descriptions.

Main PCA Circuitry 2A-3.

The following paragraphs describe the major circuit blocks on the Main PCA.

POWER SUPPLY 2A-4.

The Power Supply functional block provides voltages required by the vacuum-fluorescent display (-30V dc, -5.0V dc, and filament voltage of 5.4V ac), the inguard circuitry (-5.4V dc VSS, +5.3V dc VDD, and +5.6V dc VDDR), and outguard digital circuitry of +5.0V dc (VCC).

Within the Power Supply, the Raw DC Supply converts ac line voltage to dc levels. The 5V Switching Supply converts this raw dc to 5.0V ±0.25V dc, which is used by the Inverter in generating the above-mentioned outputs. The Power Fail Detector monitors the Raw DC Supply and provides a power supply status signal to the Microprocessor in the Digital Kernel.

DIGITAL KERNEL 2A-5.

The Digital Kernel functional block is responsible for the coordination of all activities within the instrument. This block requires voltages from the Power Supply and signals from the Power-on Reset circuit.

Specifically, the Digital Kernel Microprocessor performs the following functions:

- Executes the instructions stored in FLASH EPROM.
- Stores temporary data and nonvolatile instrument configuration data in NVRAM.
- Stores instrument calibration data in FLASH EPROM.
- Communicates with the microcontroller on the A/D Converter PCA via the Serial Communication (Guard Crossing) block.
- Communicates with the Display Controller to display readings and user interface information.
- Communicates with the Field Programmable Gate Array, which scans the user interface keyboard found on the Display Assembly and interfaces with the Digital I/O hardware.
- Communicates with a host computer via the RS-232 interface.
- Stores instrument setup and measurement data on a Static RAM memory card installed in the Memory Card Interface Assembly.
- Reads the digital inputs and changes digital and alarm outputs.

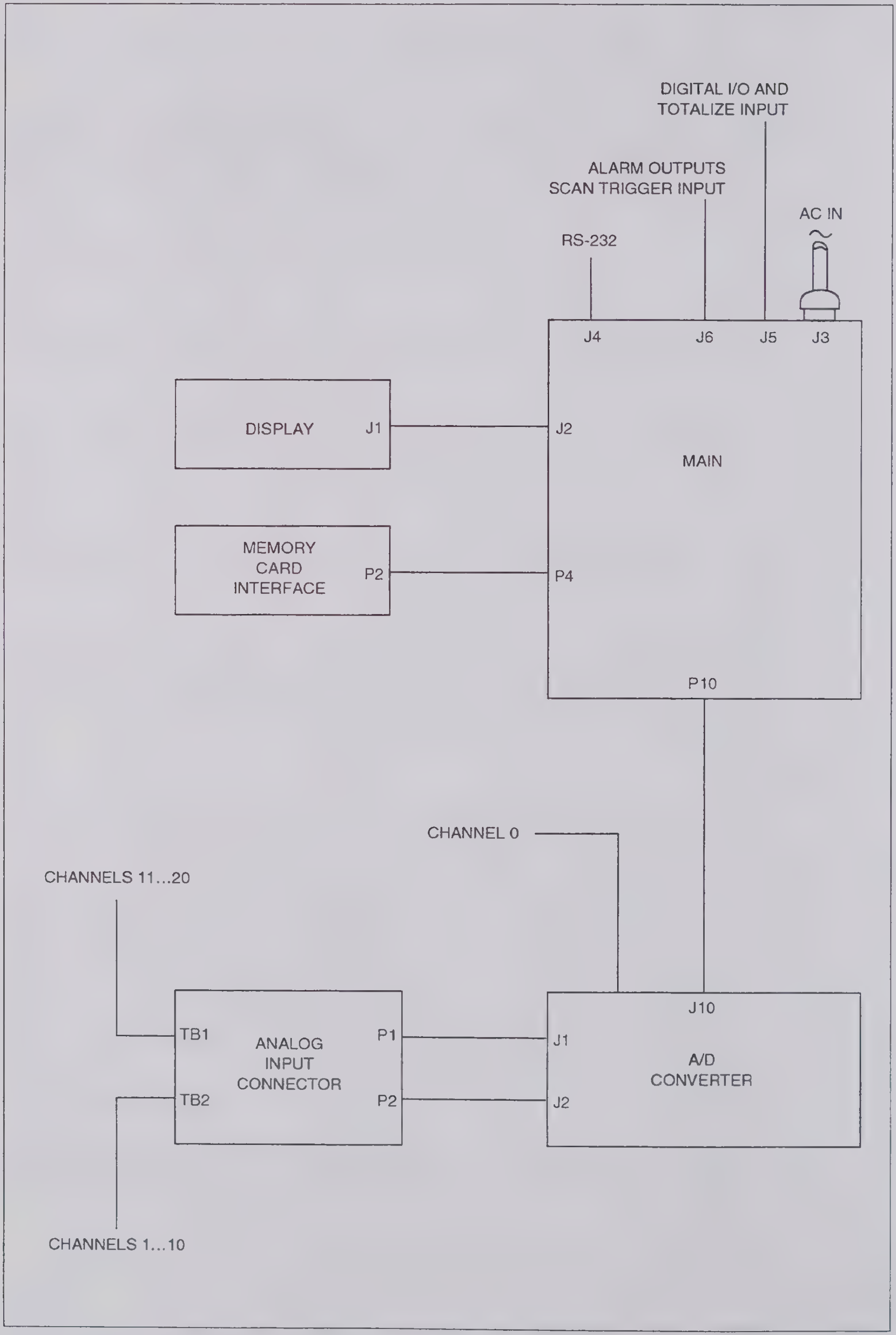

DIGITAL I/O AND TOTALIZE INPUT
ALARM OUTPUTS SCAN TRIGGER INPUT
AC IN
RS-232
J4
J6
J5
J3
DISPLAY
J1
J2
MAIN
MEMORY CARD INTERFACE
P2
P4
P10
CHANNEL 0
CHANNELS 11...20
J10
TB1
ANALOG INPUT CONNECTOR
P1
J1
A/D CONVERTER
TB2
P2
J2
CHANNELS 1...10

Figure 2A-1. Interconnect Diagram

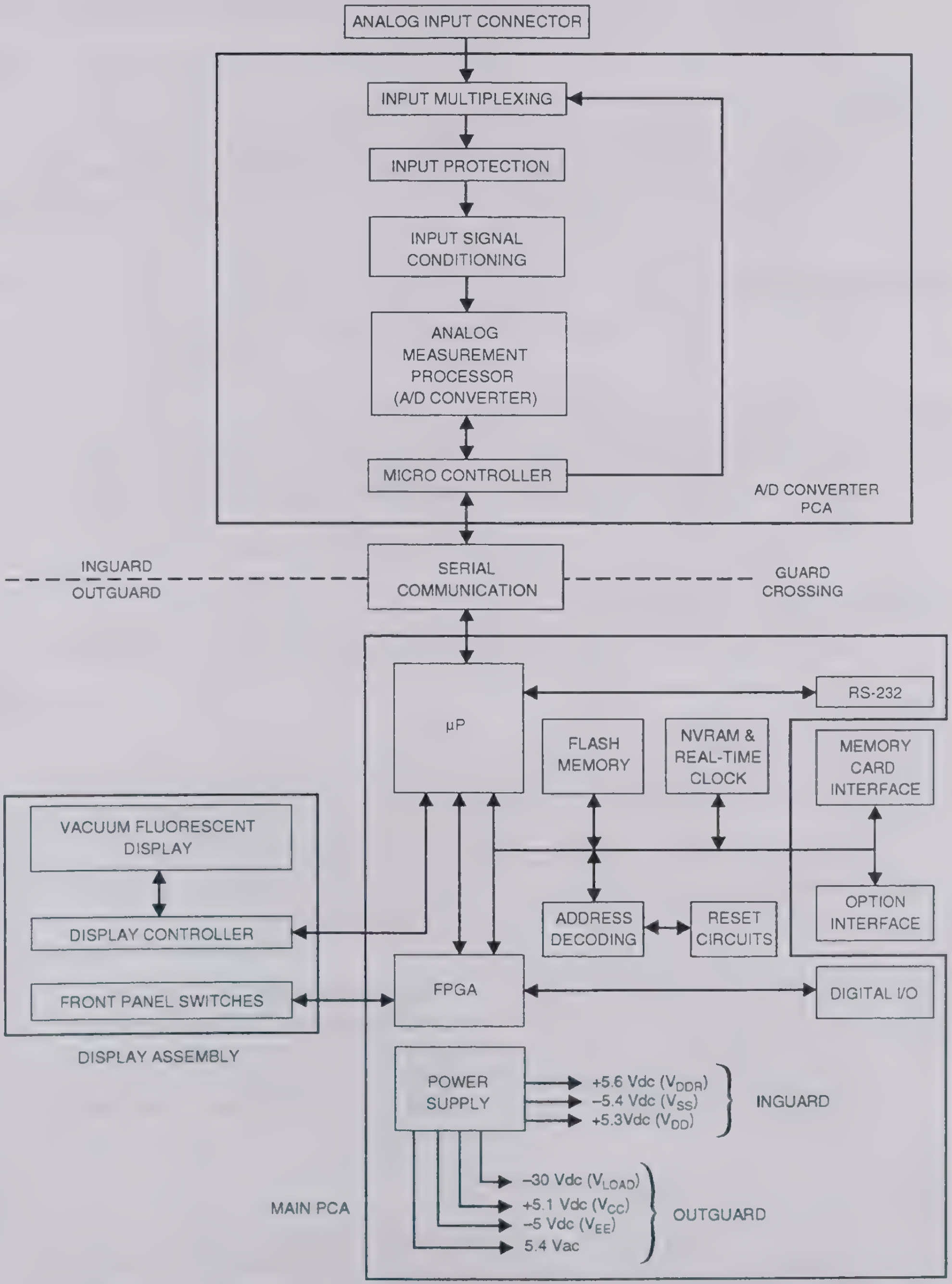

ANALOG INPUT CONNECTOR
INPUT MULTIPLEXING
INPUT PROTECTION
INPUT SIGNAL CONDITIONING
ANALOG MEASUREMENT PROCESSOR (A/D CONVERTER)
MICRO CONTROLLER
A/D CONVERTER PCA
INGUARD
OUTGUARD
SERIAL COMMUNICATION
GUARD CROSSING
µP
RS-232
FLASH MEMORY
NVRAM & REAL-TIME CLOCK
MEMORY CARD INTERFACE
VACUUM FLUORESCENT DISPLAY
DISPLAY CONTROLLER
FRONT PANEL SWITCHES
DISPLAY ASSEMBLY
ADDRESS DECODING
RESET CIRCUITS
OPTION INTERFACE
FPGA
DIGITAL I/O
POWER SUPPLY
+5.6 Vdc (V_{DDR})
–5.4 Vdc (V_{SS})
+5.3Vdc (V_{DD})
INGUARD
–30 Vdc (V_{LOAD})
+5.1 Vdc (V_{CC})
–5 Vdc (V_{EE})
5.4 Vac
OUTGUARD
MAIN PCA

Figure 2A-2. Overall Functional Block Diagram

SERIAL COMMUNICATION (GUARD CROSSING) 2A-6.

This functional block provides a high isolation voltage communication path between the Digital Kernel of the Main PCA and the microcontroller on the A/D Converter PCA. This bidirectional communication circuit requires power supply voltages from the Power Supply block.

DIGITAL INPUTS AND OUTPUTS 2A-7.

This functional block contains the Totalizer and External Trigger Input Buffers, eight bidirectional Digital I/O channels, four Alarm Outputs, and the Input Threshold control circuits. These circuits require power supply voltages from the Power Supply and signals from the Digital Kernel.

A/D Converter PCA 2A-8.

The following paragraphs describe the major blocks of circuitry on the A/D Converter PCA.

ANALOG MEASUREMENT PROCESSOR 2A-9.

The Analog Measurement Processor (A3U8) provides input signal conditioning, ranging, a/d conversion, and frequency measurement. This custom chip is controlled by the A/D Microcontroller (A3U9). The A/D Microcontroller communicates with the Main PCA Microprocessor (A1U1) over a custom serial interface.

INPUT PROTECTION CIRCUITRY 2A-10.

This circuitry protects the instrument measurement circuits during overvoltage conditions.

INPUT SIGNAL CONDITIONING 2A-11.

Here, each input is conditioned and/or scaled to a dc voltage for measurement by the a/d converter. DC voltage levels greater than 3V are attenuated. To measure resistance, a dc voltage is applied across a series connection of the input resistance and a reference resistance to develop dc voltages that can be ratioed. DC volts and ohms measurements are filtered by a passive filter. AC voltages are first scaled by an ac buffer, converted to a representative dc voltage by an rms converter, and then filtered by an active filter.

ANALOG-TO-DIGITAL (A/D) CONVERTER 2A-12.

The dc voltage output from the signal conditioning circuits is applied to a buffer/integrator which charges a capacitor for an exact amount of time. The time required to discharge this capacitor, which is proportional to the level of the unknown input signal, is then measured by the digital counter circuits in the Analog Measurement Processor.

INGUARD MICROCONTROLLER CIRCUITRY 2A-13.

This microcontroller (and associated circuitry) controls all functions on the A/D Converter PCA and communicates with the digital kernel on the Main PCA. Upon request by the Main PCA, the inguard microcontroller selects the input channel to be measured through the channel selection circuitry, sets up the input signal conditioning, commands the Analog Measurement Processor to begin a conversion, stops the measurement, and then fetches the measurement result. The inguard microcontroller manipulates the result mathematically and transmits the reading to the digital kernel.

CHANNEL SELECTION CIRCUITRY 2A-14.

This circuitry consists of a set of relays and relay-control drivers. The relays form a tree that routes the input channels to the measurement circuitry. Two of the relays are also used to switch between 2-wire and 4-wire operation.

OPEN THERMOCOUPLE CHECK CIRCUITRY 2A-15.

Under control of the Inguard Microcontroller, the open thermocouple check circuit applies a small ac signal to a thermocouple input before each measurement. If an excessive resistance is encountered, an open thermocouple input condition is reported.

Input Connector Assembly 2A-16.

The following paragraphs briefly describe the major sections of the Input Connector PCA, which is used for connecting most of the analog inputs to the instrument.

20 CHANNEL TERMINALS 2A-17.

Twenty HI and LO terminal blocks are provided in two rows, one for channels 1 through 10 and one for channels 11 through 20. The terminals can accommodate a wide range of wire sizes. The two rows of terminal blocks are maintained very close to the same temperature for accurate thermocouple measurements.

REFERENCE JUNCTION TEMPERATURE 2A-18.

A semiconductor junction is used to sense the temperature of the thermocouple input terminals. The resulting dc output voltage is proportional to the block temperature and is sent to the A/D Converter PCA for measurement.

Display PCA 2A-19.

The Display Assembly controller communicates with the main Microprocessor over a three-wire communication channel. Commands from the Microprocessor inform the Display Controller how to modify its internal display memory. The Display Controller then drives the grid and anode signals to illuminate the required segments on the Display. The A2 Display Assembly requires power supply voltages from the Power Supply, a reset signal from the Reset Circuit, and a clock signal from the Digital Kernel.

Memory Card Interface PCA 2A-20.

The Memory Card Interface PCA is used to access the memory on an industry standard memory card installed through the slot in the front panel of the instrument. This assembly allows management of the memory card power, adapts timing of accesses by the Digital Kernel to the memory card, and provides visible indicators for low battery voltage and memory card busy status.

DETAILED CIRCUIT DESCRIPTION 2A-21.

Main PCA 2A-22.

The following paragraphs describe the operation of the circuits on the Main PCA. The schematic for this pca is located in Section 8.

POWER SUPPLY CIRCUIT DESCRIPTION 2A-23.

The Hydra power supply consists of three major sections:

- Raw DC Supply

  The raw dc supply converts line voltage (90V to 264V ac) to a dc output of 7.5V to 35V.

- 5V Switcher Supply

  The 5V switching supply regulates the 7.5 to 35V dc input to a nominal 5.0V ±0.25V dc (VCC).

- Inverter

  Using the 5V switching supply output, the inverter generates the -30V dc, -5V dc, and 5.4V ac supply levels needed for the vacuum-fluorescent display and the RS-232 Interface. The inverter also provides isolated +5.3V (VDD), +5.6V (VDDR), and -5.4V (VSS) outputs for the inguard circuitry.

Raw DC Supply 2A-24.

The raw dc supply circuitry receives input from power transformer T401, which operates on an input ranging from 90V to 264V ac. The power transformer is energized whenever the power cord is plugged into the ac line; there is no on/off switch on the primary side of the transformer. The transformer has an internal 275V ac metal-oxide varistor (MOV) to clamp line transients. The MOV normally acts as an open circuit. When the peak voltage exceeds approximately 400V, the line impedance in series with the line fuse limits transients to approximately 450V. All line voltages use a slow blow 0.125 A, 250V fuse.

On the secondary side of the transformer, rectifiers A1CR2, A1CR3, and capacitor A1C7 rectify and filter the output. When it is ON, switch A1S1 (the front panel POWER switch) connects the output of the rectifiers to the filter capacitor and the rest of the instrument. Depending on line voltage, the output of the rectifiers is between 7.5 and 35V dc. Capacitor A1C2 helps to meet electromagnetic interference (EMI) and electromagnetic compatibility (EMC) requirements.

When external dc power is used, the power switch connects the external dc source to power the instrument. The external dc input uses thermistor A1RT1 (for overcurrent protection) and diode A1CR1 (for reverse input voltage protection.) Capacitor A1C59 helps meet EMI/EMC requirements. Resistor A1R48, capacitors A1C2 and A1C39 also ensure that the instrument meets EMI/EMC performance requirements.

Auxiliary 6V Supply 2A-25.

Three-terminal regulator A1U19, voltage-setting resistors A1R44 and A1R46, and capacitor A1C34 make up the auxiliary 6-volt supply. This supply is used for the inverter oscillator, inverter driver, and the power fail detection circuits.

5V Switcher 2A-26.

The 5V switcher supply uses a switcher supply controller/switch device A1U9 and related circuitry. The 7.5V dc to 35V dc input is regulated to 5.0V dc (VCC) through pulse-width modulation at a nominal switching frequency of 70 kHz.

The output voltage of the switcher supply is controlled by varying the duty cycle (ON time) of the switching transistor in the controller/switch device A1U9. A1U9 contains the supply reference, oscillator, switch transistor, pulse-width modulator comparator, switch drive circuit, current-limit comparator, current-limit reference, and thermal limit. Dual inductor A1T2 regulates the current that flows from the raw supply to the load as the switching transistor in A1U9 is turned on and off. Complementary switch A1CR10 conducts when the switching transistor is off.

The pulse-width modulator comparator in A1U9 compares the output to the reference and sets the ON-time/OFF-time ratio to regulate the output to 5.0V dc. A1C26 is the input filter capacitor, and A1C14 is the output filter capacitor. Proper inductor and capacitor values set the filter frequency response to ensure best overall system stability. Circuitry consisting of A1R27, A1C20, and A1C18 ensure that the switcher supply remains stable and operating in the continuous mode. Resistors A1R17, A1R23, A1R24, and A1R26 set the output voltage at 5.0V (either A1R17 or A1R23 may have been removed at the factory to adjust the output voltage of the supply to within 5% of 5.0V). A1R18 samples the raw supply voltage and injects a small correction to the output level and improves the line regulation over the very wide four-to-one dc input voltage range. Capacitor A1C21 sets the operating frequency of the switcher at approximately 70 kHz.

Resistors A1R29, A1R30, A1R31, A1R32, and A1R33 sense the output current of the switcher. The divided-down voltage produced from these sense resistors is connected to the current limit comparators (A1U9-9). When the peak current reaches approximately 3 amps, the switch transistor is turned off to limit the output current of the switcher supply.

Inverter 2A-27.

The inverter supply uses a two transistor driven push-pull configuration. The center tap of transformer A1T1 primary is connected to the 5.0V dc VCC supply, and each side is alternately connected to common through transistors A1Q7 and A1Q8. A1R38 may be removed to disable the inverter supply for troubleshooting purposes. A1Q7 and A1Q8 are driven by the outputs of D flip-flop A1U22. Resistors A1R34 and A1R28, and diodes A1CR11 and A1CR12 shape the input drive signals to properly drive the gate of the transistors. D flip-flop A1U22 is wired as a divide-by-two counter driven by a 110-kHz square wave. The 110-kHz square wave is generated by hex inverter A1U23, which is connected as an oscillator with a frequency determined by the values of resistors A1R40 and A1R47 and capacitor A1C35. The resulting ac voltage produced across the secondary of A1T1 is rectified to provide the input to the inverter inguard and outguard supplies.

Inverter Outguard Supply 2A-28.

The inverter outguard supply provides three outputs: 5.4V ac, -30V dc, and -5V dc. These voltages are required by the display and RS-232 drivers and receiver. The 5.4V ac supply comes off the secondary windings (pins 6 and 7) on transformer T1, and it is biased at -24V dc with zener diode A1VR3 and resistor A1R22. Dual diodes A1CR8 and A1CR9 and capacitor A1C17 are for the -30V dc supply. Capacitors A1C30 and A1C31, and dual diodes A1CR13 form a voltage doubler circuit that generates -12 volts. Three-terminal regulator A1U18 then regulates this voltage down to -5V for the RS-232 circuit. Capacitor A1C32 is needed for transient response performance of the three-terminal regulator.

Inverter Inguard Supply 2A-29.

The inverter inguard supply provides three outputs: +5.3V dc (VDD) and -5.4V dc (VSS) for the inguard analog and digital circuitry, and +5.6V dc (VDDR) for the relays. Diodes A1CR5 and A1CR6, and capacitor A1C12 are for the +9.5 volt source, and diodes A1CR7 and capacitor A1C13 are for the -9.5V source.

Three-terminal regulator A1U6 regulates the 9.5V source to 5.6V for the relays. A1R5 and A1R6 set the output voltage at 5.6V. A1C6 is required for transient performance. The +5.3V regulator circuit uses A1Q2 for the series-pass element and A1Q4 as the error amplifier. A1VR2 is the reference for the positive supply. A1R14 provides the current to bias the reference zener. A1C4 is the output filter, and A1C9 provides frequency compensation of the regulator circuit. Transistor A1Q1 and resistor A1R13 make up the current-limit circuit.

When the voltage across A1R13 increases enough to turn on A1Q1, output current is limited by removing the base drive to A1Q2.

The -5.4 volt regulator operates like the +5.3 volt regulator, except that the NPN transistors in the positive supply are PNP transistors in the negative supply, and the PNP transistors in the positive supply are NPN transistors in the negative supply. If a VDD-to-VSS short circuit occurs, diode A1CR4 ensures that current limit occurs at the limit set for the -5.4V dc or +5.3V dc supply, whichever is lower.

Power Fail Detection 2A-30.

The power fail detection circuit generates a signal to warn the Microprocessor that the power supply is going down. A comparator in A1U10 compares the divided-down raw supply voltage to a voltage reference internal to A1U10. When the raw supply voltage is greater than about 8V dc, the output of A1U10 is "high" and when the raw supply falls below 8V dc, the output goes "low". Resistors A1R19 and A1R20 make up the divider, and capacitor A1C74 provides filtering of high frequency noise at the comparator input. The reference voltage internal to A1U10 is nominally 1.3 volts dc.

DIGITAL KERNEL 2A-31.

The Digital Kernel is composed of the following nine functional circuit blocks: the Reset Circuits, the Microprocessor, the Address Decoding, the Flash Memory, the Nonvolatile Static RAM and Real-Time Clock, the FPGA (Field Programmable Gate Array), the Serial Communication (Guard Crossing), the RS-232 Interface, and the Option Interface.

Reset Circuits 2A-32.

The Power-On Reset signal (POR*, A1U10-7) is generated by the Microprocessor Supervisor, which monitors the voltage of VCC at A1U10-2. If VCC is less than +4.65 volts, then A1U10-7 will be driven low. POR* drives the enable inputs of the four tri-state buffers in A1U2, causing the HALT*, RESET*, ORST*, and DRST* signals to be driven low when POR* is low. When POR* goes high, the tri-state buffer outputs (A1U2) go to their high-impedance state and the pull-up resistors pull the outputs to a high level.

When HALT* and RESET* are both driven low, the Microprocessor (A1U1) is reset and will begin execution when they both go high. The Microprocessor may execute a "reset" instruction during normal operation to drive A1U1-92 low for approximately 10 microseconds to reset all system hardware connected to the RESET* signal.

The Display Reset signal (DRST*) is driven low by A1U2-6 when POR* is low, or it may be driven low by the Microprocessor (A1U1-56) if the instrument firmware needs to reset only the display hardware. For example, the firmware resets the display hardware after the FPGA is loaded at power-up and the Display Clock (DCLK) signal from the FPGA begins normal operation. This ensures that the Display Processor is properly reset while DCLK is active.

The Option Reset signal (ORST*) is driven low by A1U2-3 when POR* is low, or it may be driven low by the Microprocessor (A1U1-58) if the instrument firmware needs to reset only the Option Interface hardware. For example, the firmware resets any option interface hardware after the FPGA is loaded at power-up and the Option Clock (OCLK) signal from the FPGA begins normal operation. This ensures that any Option Interface hardware is properly reset while OCLK is active.

Microprocessor 2A-33.

The Microprocessor uses a 16-bit data bus and a 19-bit address bus to access locations in the Flash Memory (A1U14 and A1U16), the Nonvolatile Static RAM (A1U20 and A1U24), the Real-Time Clock (A1U12), the FPGA (A1U25), the Memory Card Interface PCA (A6), and the Option Interface (A1J1). All of the data bus lines and the lowest 12 address lines have series termination resistors located near the Microprocessor (A1U1) to ensure that the instrument meets EMI/EMC performance requirements. When a memory access is done to the upper half of the data bus (D15 through D8), the upper data strobe (UDS*) goes low. When a memory access is done to the lower half of the data bus (D7 through D0), the lower data strobe (LDS*) goes low. When a memory access is a read cycle, R/W* must be high. Conversely for any write cycle, R/W* must be low.

The Microprocessor is a variant of the popular Motorola 68000 processor and is enhanced by including hardware support for clock generation, address decoding, timers, parallel ports, synchronous and asynchronous serial communications, interrupt controller, DMA (Direct Memory Access) controllers, and a watchdog timer.

The 12.288-MHz system clock signal (A1TP11) is generated by the oscillator circuit composed of A1U1, A1Y1, A1R2, A1C3, and A1C8. This clock goes through a series termination resistor (A1R107) to the FPGA (A1U25) and also through another series termination resistor (A1R86) to the Memory Card Interface (A1P4). These resistors are necessary to ensure that the instrument meets EMI/EMC performance requirements.

The Microprocessor has four software programmed address decoders that include wait state control logic. These four outputs are used to enable external memory and I/O components during read and write bus cycles. See "Address Decoding" for a complete description.

One sixteen-bit timer in the Microprocessor is used to generate a regular interrupt every 53.333 milliseconds. This timer uses the 12.288-MHz system clock (A1TP11) as a clock source. The timer changes the state of parallel port pin A1U1-113 each time that it interrupts the Microprocessor. The signal at A1U1-113 should be a 9.375-Hz square wave (period of 106.67 milliseconds).

Another 16-bit timer is used as the totalizer counter. The totalizer signal originating at J5-2 goes through the totalizer input buffer, the FPGA, and then to the external clock input for this timer in the Microprocessor (U1-114 and TP20). See the Totalizer part of "Digital I/O" for a complete description.

The Microprocessor has two parallel ports. Many of the parallel port pins are either used as software controlled signals or as inputs or outputs of timers and serial communication channels. Port A has 16 bits and Port B has 12 bits.

The Microprocessor communicates to the Display Controller using a synchronous, three-wire communication interface controlled by hardware in the Microprocessor. Information is communicated to the Display Controller to display user interface menus and measurement data. Details of this communication are described in the Display Controller Theory of Operation in this section.

The Microprocessor communicates to the Microcontroller on the A/D Converter PCA (via the Serial Communication circuit) using an asynchronous communication channel at 4800 baud. Communication to the Microcontroller (A3U9) originates at A1U1-54. Communication from the A/D's Microcontroller to the Microprocessor appears at A1U1-53. When there is no communication in progress between the Microprocessor and the Microcontroller, both of these signals are high.

The Microprocessor uses another asynchronous communication channel to communicate to external computing or modem equipment through the RS-232 interface. This interface is described in detail in the RS-232 Interface Theory of Operation in this section.

The third asynchronous communication channel in the Microprocessor is connected to the Option Interface (J1) but is not used in the instrument at this time.

The interrupt controller in the Microprocessor prioritizes interrupts received from hardware devices both internal and external to the Microprocessor. Table 2A-1 lists interrupt sources from highest to lowest priority.

The Microprocessor also has several internal DMA (Direct Memory Access) controllers that are used by the serial communication channels. Each serial communication channel has a DMA channel that handles character reception and another that handles character transmission. The use of these DMA controllers is transparent to the external operation of the Microprocessor, but it is important to understand that communication is handled at hardware speeds without the need for an interrupt for each character being transferred.

A watchdog timer internal to the Microprocessor is programmed to have a 10-second timeout interval. If the code executed by the Microprocessor fails to reinitialize the watchdog timer every 10 seconds or less, then A1U1-117 (POR*) is driven low for 16 cycles of SCLK (approximately 1.3 microseconds). This results in a complete hardware reset of the instrument, which restarts operation.

Address Decoding 2A-34.

The four chip-select outputs on the Microprocessor are individual software programmed elements that allow the Microprocessor to select the base address, the size, and the number of wait states for the memory accessed by each output.

Table 2A-1. Microprocessor Interrupt Sources

Pin	Signal Name	Description
A1U1-95	XTINT*	External Trigger Interrupt (Highest Priority)
A1U1-96	CINT*	Real-Time Clock Interrupt; once per second
A1U1-121	KINT*	Keyboard Interrupt; interrupts on each debounced change of keyboard conditions.
		RS-232 Interface Interrupt; internal to the Microprocessor.
		A/D Communication Interrupt; internal to the Microprocessor.
		Timer Interrupt every 53.333 milliseconds; internal to the Microprocessor.
A1U1-119	MCINT*	Memory Card Interface Interrupt; interrupts when a memory card is inserted, removed, powered up or powered down.
		Totalizer Interrupt; internal to the Microprocessor. Interrupts on totalizer overflow from a count of 65535 to 0.
A1U1-97	OINT*	Option Interface Interrupt; not currently used in this product.

The FLASH* signal (A1U1-128) enables accesses to 128 kilobytes of Flash Memory (A1U14 and A1U16). The FLASH* signal goes through jumper W3, which must always be installed during normal instrument operation. W3 is removed only during the initial programming of the Flash Memory during production at the factory. The SRAM* signal enables the Nonvolatile Static RAM (A1U20 and A1U24), and the MCARD* signal goes to the Memory Card Interface PCA (A6). The I/O* signal goes to the I/O Decoder (A1U11), which decodes small areas of address space for I/O devices like the FPGA, the Real-Time Clock, and the Option Interface. There are no wait states for accesses to FLASH* and SRAM*, but two wait states are used for any access to I/O*. Each wait state adds approximately 83 nanoseconds to the length of a memory read or write cycle. The Memory Card Interface handles wait state timing for any accesses to MCARD*.

When the Microprocessor is starting up (also referred to as "booting"), the address decoding maps the address space as shown in Table 2A-2.

Just before beginning execution of the instrument code, the address decoding is changed to map the address space as shown in Table 2A-3. This change switches the positions of Flash Memory and Nonvolatile Static RAM within the address space of the Microprocessor.

Flash EPROM 2A-35.

The Flash EPROM is an electrically erasable and programmable memory that provides storage of instructions for the Microprocessor and measurement calibration data.

Table 2A-2. Booting Microprocessor Memory Map

HEXADECIMAL ADDRESS	DEVICE SELECTED
000000 - 03FFFF	Flash (A1U14 and A1U16)
100000 - 13FFFF	NVRAM (A1U20 and A1U24)
300000 - 30007F	FPGA Configuration (A1U25)
300080 - 3000FF	Real-Time Clock (A1U12)
300100 - 30017F	Option Interface (A1J1)
310000 - 311FFF	Memory Card Interface (A1P4)
400000 - 401000	Microprocessor Internal

Table 2A-3. Instrument Microprocessor Memory Map

HEXADECIMAL ADDRESS	DEVICE SELECTED
000000 - 03FFFF	NVRAM (A1U20 and A1U24)
100000 - 13FFFF	Flash (A1U14 and A1U16)
300000 - 300007	FPGA Control / Status (A1U25)
300008 - 30000F	Alarm Outputs (A1U25)
300010 - 300017	Digital Outputs (A1U25)
300018 - 30001F (Read Only)	Digital Inputs (A1U25)
300020 - 300027 (Read Only)	Keyboard Input (A1U25)
300080 - 3000FF	Real-Time Clock (A1U12)
300100 - 30017F	Option Interface (A1J1)
310000 - 311FFF	Memory Card Interface (A1P4)
400000 - 401000	Microprocessor Internal

A switching power supply composed of A1U15, A1T3, A1CR21, and A1C66 through A1C69 generates a nominal +12 volt programming power supply (VPP) when the Microprocessor drives VPPEN high (A1U15-2). Resistor A1R35 pulls A1U15-2 to near ground during power-up to ensure that A1U15 is not enabled while the Microprocessor is being reset. When the power supply is not enabled, the output voltage (VPP) should be about 0.1 volt less than the input voltage of the power supply (VCC).

The only time that the programming power supply is active is when new firmware is being loaded or new calibration constants are being stored into the Flash EPROM. The code executed immediately after power-up is stored in an area of the Flash EPROM (known as the Boot Block) that is only eraseable and reprogrammable if BBVPP (A1U14-30 and A1U16-30) is at a nominal +12 volts. This may be accomplished by installing jumper A1W1, but this should only be done by a trained technican, and A1W1 should never be installed unless it is necessary to update the Boot firmware. In normal operation, resistor A1R73 and diode A1CR20 pull BBVPP up to about 0.25 volts less than VCC.

The FLASH* chip select (A1U1-128) for these devices goes low for any memory access to A1U14 or A1U16. The FLASH* signal goes through jumper W3, which must always be installed during normal instrument operation. W3 is removed only during the initial programming of the Flash Memory during production at the factory. A1U14 is connected to the high 8 bits of the data bus, so read accesses are enabled by the Read Upper (RDU*) signal going low, and write accesses are enabled by the Write Upper (WRU*) signal going low. A1U16 is connected to the low 8 bits of the data bus, so read accesses are enabled by the Read Lower (RDL*) signal going low, and write accesses are enabled by the Write Lower (WRL*) signal going low.

NVRAM / Real-Time Clock 2A-36.

The Nonvolatile Static RAM (NVRAM) provides the storage of data and configuration information for the instrument. The Real-Time Clock maintains time and calendar date information for use by the instrument.

A nonvolatile power supply (VBB) biases A1U12, A1U20, A1U24, and A1U26. The Microprocessor Supervisor (A1U10) monitors the voltage on VCC (A1U10-2). If VCC is greater than the voltage of the lithium battery (A1U10-8), A1U10 switches VCC from A1U10-2 to A1U10-1 (VBB). If VCC drops below the voltage of the lithium battery (A1U10-8), A1U10 will switch voltage from lithium battery A1BT1 through current-limiting resistor A1R98 to A1U10-1 (VBB). The nominal current required from the lithium battery (A1BT1) at room temperature with the instrument powered down is approximately 2 microamperes. This can be easily measured by checking the voltage across A1R98.

The SRAM* address decode output (A1U1-127) for the 128 kilobytes of NVRAM goes low for any memory access to A1U20 or A1U24. This signal must go through two NAND gates in A1U26 to the NVRAM chip select inputs (A1U20-22 and A1U24-22). This ensures that when the instrument is powered down and A1U10-7 is driven low, A1U20-22 and A1U24-22 will be driven high so that the contents of the NVRAM cannot be changed and the power dissipated by the NVRAM is minimized. Jumper A1W4 in A<18> is not used in the current instrument; it should be installed only if more NVRAM is needed in a future instrument that needs 512 kilobytes of NVRAM using the same circuit board. A1U24 is connected to the high 8 bits of the data bus, so read accesses are enabled by the Read Upper (RDU*;A1U24-24) signal going low, and write accesses are enabled by the Write Upper (WRU*;A1U24-29) signal going low. A1U20 is connected to the low 8 bits of the data bus, so read accesses are enabled by the Read Lower (RDL*;A1U20-24) signal going low, and write accesses are enabled by the Write Lower (WRL*;A1U20-29) signal going low.

Memory accesses to the Real-Time Clock (A1U12) are enabled by the RTC* address decode output (A1U11-16). This signal must go through two NAND gates in A1U26 to the Real-Time Clock chip select input (A1U12-18). This ensures that when the instrument is powered down and A1U10-7 is driven low, A1U12-18 will be driven high so that the contents of the Real-Time Clock cannot be changed, and the power dissipated by the Real-Time Clock is minimized. A1U12 is connected to the low 8 bits of the data bus, so read accesses are enabled by the Read Lower (RDL*;A1U12-19) signal going low, and write accesses are enabled by the Write Lower (WRL*;A1U12-20) signal going low. When the instrument is powered up, the accuracy of the timebase generated by the internal crystal may be tested by measuring the frequency of the 1-Hz square wave output (A1U12-4). The Real-Time Clock also has an interrupt output (A1U12-3) that is used by the Microprocessor to time the interval between scans when a scan interval is set in the instrument. There should be one interrupt per second from the Real-Time Clock.

Serial Communication (Guard Crossing) 2A-37.

The transmission of information from the Microprocessor (A1U1) to the Microcontroller (A3U9) is accomplished via the circuit made up of A1Q10, A1U7, A1R8, A1R16, and A3R8. The transmit output from the Microprocessor (A1U1-54) is buffered by A1Q10, which then switches current through optocoupler LED (A1U7-2). Resistor A1R8 limits the current through the LED.

The phototransistor in A1U7 responds to the light emitted by the LED when A1U1-54 is driven low. (The collector of the phototransistor, A1U7-5, goes low.) The phototransistor collector is pulled up by A3R8 on the A/D Converter PCA. When turning off, the phototransistor base discharges through A1R16. With this arrangement, the rise and fall times of the phototransistor collector signal are nearly symmetrical.

The transmission of data from the Microcontroller (A3U9) to the Microprocessor (A1U1) is accomplished via the circuit made up of A3Q1, A3R7, A1U5, A1R7, and A1R3. The transmit output from the Microcontroller (A3U9-14) is inverted by A3Q1, which drives the optocoupler LED (A1U5-2) through resistor A3R7. The current through the LED is limited by resistor A3R7. The phototransistor in A1U5 responds to the light emitted by the LED when A1U5-2 is driven low. (The collector of the phototransistor, A1U5-4, goes low.) The phototransistor collector (A1U5-5) is pulled up by resistor A1R3. When turning off, the phototransistor base discharges through A1R7. With this arrangement, the rise and fall times of the phototransistor collector signal are nearly symmetrical.

Display/Keyboard Interface 2A-38.

The Microprocessor sends information to the Display Processor via a three-wire synchronous communication interface. The detailed description of the DISTX, DISRX, and DSCLK signals may be found in the detailed description of the Display PCA. Note that the DISRX signal is pulled down by resistor A1R1 so that Microprocessor inputs A1U1-49 and A1U1-118 are not floating at any time.

The Display Clock (DCLK) is a 1.024-MHz clock that is generated by the FPGA. Series resistor A1R85 is necessary to ensure that the instrument meets EMI/EMC performance requirements. The Display Assembly is reset when the Display Reset (DRST*) signal is driven low. The reset circuit on the Display Assembly is discharged through resistor A1R21, which limits the peak current from A2C3. DRST* is driven low at power-up, or it may be driven low by the Microprocessor (A1U1-56).

The Keyboard interface is made up of six bidirectional I/O lines from the Field Programmable Gate Array (FPGA). SWR1 through SWR6 (A1U25-67, A1U25-68, A1U25-71, A1U25-73, A1U25-70, A1U25-69, respectively) are pulled up by A2Z1 on the Display PCA. Hardware in the FPGA scans the keyboard switch array, detects and debounces switch changes, and interrupts the Microprocessor to indicate that a debounced keypress is available. A detailed description of this may be found under the following heading "Field Programmable Gate Array (FPGA)".

Field Programmable Gate Array (FPGA) 2A-39.

The FPGA is a complex programmable logic device that contains the following six functional elements after the Microprocessor has loaded the configuration into the FPGA: Clock Dividers, Internal Register Address Decoding, Keyboard Scanner, Digital I/O Buffers and Latches, Totalizer Debouncing and Mode Selection, and the External Trigger Logic.

When the instrument is powered up, the FPGA clears its configuration memory and waits until RESET* (A1U25-78) goes high. The FPGA then tests its mode pins and should determine that it is in "peripheral" configuration mode (A1U25-54 high; A1U25-52 low; A1U25-56 high). In this mode the Microprocessor must load the configuration information into the FPGA before the FGPA logic can begin operation.

The Microprocessor first makes sure that the FPGA is ready to be configured by driving XD/P* (A1U25-80) low and then pulsing the RESET* (A1U25-78) input low for about 10 microseconds. The Microprocessor then waits until the XINIT* (A1U25-65) output goes high, indicating that the FPGA has been initialized and is ready for configuration. The Microprocessor then writes a byte of configuration data to the FPGA by driving PGA* (A1U25-88) low and latching the data on the data inputs (D<8> through D<15>) by pulsing WRU* (A1U25-5) low and then back high. The XRDY (A1U25-99) output then goes low to indicate that the FPGA is busy loading that configuration byte. The Microprocessor will then wait until XRDY goes high again before loading the next configuration byte, and the sequence is repeated until the last byte is loaded. While the configuration data is being loaded, the FPGA drives the XD/P* signal (A1U25-80) low. When the FPGA has been completely configured, the XD/P* signal is released and pulled high by resistor A1R70. The Microprocessor will repeat the configuration sequence if XD/P* (A1U25-80) does not go high when it is expected to.

CLOCK DIVIDERS

The 12.288-MHz system clock (A1U25-30) is divided down by the Clock Dividers to create the 3.072-MHz Option Clock (OCLK; A1U25-22) and 1.024-MHz Display Clock (DCLK; A1U25-19). The Display Clock is not a square wave; it is low for 2/3 of a cycle and high for the other 1/3. The Display Clock is also used internal to the FPGA to create the 128-kHz Totalizer Debouncer Clock and the 4-kHz Keyboard Scanner Clock.

INTERNAL REGISTER ADDRESS DECODING

The FPGA logic decodes four bits of the address bus (A<3> through A<6>), the PGA* chip select signal (A1U25-88), RDU* (A1U25-95), and WRU* (A1U25-5) to allow the Microprocessor to read five registers and write to three registers implemented in the FPGA logic. The absolute addresses are listed in Table 2-1B.

KEYBOARD SCANNER

The Keyboard Scanner sequences through the array of switches on the Display Assembly to detect and debounce switch closures. After a switch closure is detected, it must remain closed for at least 16 milliseconds before the Microprocessor will be interrupted and the Keyboard Input register will be read from the FPGA. When the keyboard interrupt (KINT*, A1U25-62) goes low, the Keyboard Scanner stops scanning until the Microprocessor reads the Keyboard Input register which automatically clears the interrupt by driving KINT* high again. The FPGA will interrupt the Microprocessor again when the switch on the Display Assembly is detected as open again. Actually the Microprocessor will be interrupted once for each debounced change in the contents of the Keyboard Input register. See also the information on “Front Panel Switches” in the “Display PCA” section for this instrument.

The Microprocessor can enable or disable the Keyboard Scanner by changing the state of a bit in the Control/Status register that is in the FPGA. The Keyboard Scanner is disabled if the instrument is in either the RWLS or LWLS state (see User Manual; RWLS and LWLS Computer Interface Commands).

DIGITAL I/O BUFFERS AND LATCHES

The FPGA logic implements internal registers for the eight Digital Outputs (DO<0> through DO<7>) and the four Alarm Outputs (AO<0> through AO<3>). These registers are both written and read by the Microprocessor. The FPGA logic also implements an eight-bit input buffer so that the Microprocessor can read the eight Digital Input lines (DI<0> through DI<7>). See also “Digital Input Buffers” and “Digital and Alarm Output Drivers”.

TOTALIZER DEBOUNCING AND MODE SELECTION

Logic internal to the FPGA lets the Microprocessor enable a debouncer in the Totalizer input signal path. The detailed description of the Totalizer Debouncer and Mode Selection may be found under the heading “Totalizer Input”.

EXTERNAL TRIGGER LOGIC

Logic internal to the FPGA allows the Microprocessor to set up the External Trigger Logic to interrupt on rising or falling edges of the XTI input to the FPGA. The detailed description of the External Trigger operation may be found in the “External Trigger Input Circuits” section.

RS-232 Interface 2A-40.

The RS-232 interface is composed of connector A1J4, RS-232 Driver/Receiver A1U13, and the serial communication hardware in Microprocessor A1U1.

The serial communication transmit signal (A1U1-80) goes to the RS-232 driver (A1U13-14), where it is inverted and level shifted so that the RS-232 transmit signal transitions between approximately +5.0 and -5.0V dc. When the instrument is not transmitting, the driver output (TP13;A1U13-3) is approximately -5.0V dc. The RS-232 receive signal from A1J4 goes to the RS-232 receiver A1U13-4, which inverts and level shifts the signal so that the input to the serial communication hardware transitions between 0 and +5.0V dc. When nothing is being transmitted to the instrument, the receiver output (TP12;A1U13-13) is +5.0V dc.

Data Terminal Ready (DTR) and Request To Send (RTS) are modem control signals controlled by the Microprocessor. When the instrument is powered up, the Microprocessor initially sets DTR and RTS false by setting A1U1-61 and A1U1-79 high, which results in the RS-232 driver outputs (A1U13-7 and A1U13-5 respectively) going to -5.0V dc. When the instrument has initialized the RS-232 interface and is ready to receive and transmit, A1U1-61 and A1U1-79 will go low, resulting in the RS-232 DTR and RTS signals going to +5.0V dc. The RS-232 DTR and RTS signals will remain at +5.0V dc until the instrument is powered down except for a short period of time when the user changes RS-232 communication parameters from the front panel of the instrument.

Clear To Send (CTS) and Data Set Ready (DSR) are modem control inputs from the attached RS-232 equipment. Of these signals, only CTS is used when CTS flow control is enabled when CTS is turned on via the RS-232 communication setup menu. The CTS modem control signal from A1J4 goes to the RS-232 receiver A1U13-6, which inverts and level shifts the signal so that the input to the Microprocessor (A1U1-51) transitions between 0 and +5.0V dc. When the instrument is cleared to send characters to the RS-232 interface, the receiver output (A1U13-11) is +5.0V dc. If the RS-232 CTS signal is not driven by the attached RS-232 equipment, the receiver output (A1U13-11) is near 0V dc.

Option Interface 2A-41.

The interconnection to the option slot is implemented by J1 on the Main PCA. This connector (A1J1) routes the outguard logic power supply (VCC and GND), eight bits of the data bus (D<8> through D<15>), RDU*, WRU*, OCLK, RESET*, OPTE*, and the lower three bits of the address bus to the hardware installed in the option slot. This connector also routes an interrupt signal (OINT*) from the option hardware to the IRQ1* input of the Microprocessor (A1U1-97). The OPTE*, RDU*, and WRU* signals pass through series resistors that are necessary to ensure that the instrument meets EMI/EMC performance requirements.

An option sense signal from the installed option allows the Microprocessor to detect whether or not option hardware is installed. Currently there is no optional hardware available for this instrument.

DIGITAL I/O 2A-42.

The following paragraphs describe the Digital Input Threshold, Digital Input Buffers, Digital and Alarm Output Drivers, Totalizer Input, and External Trigger Input circuits.

DIGITAL INPUT THRESHOLD 2A-43.

The Digital Input Threshold circuit sets the input threshold level for the Digital Input Buffers and the Totalizer Input. A fixed value voltage divider (A1R36, A1R37) and a unity gain buffer amplifier (A1U8) are the main components in this circuit. The voltage from the divider (approximately +1.4V dc) is then buffered by A1U8, which sets the input threshold. Capacitor A1C29 filters the divider voltage at the input of A1U8.

DIGITAL INPUT BUFFERS 2A-44.

Since the eight Digital Input Buffers are identical in design, only components used for Digital Input 0 are referenced in this description. If the Digital Output Driver (A1U17-12) is off, the input to the Digital Input Buffer is determined by the voltage level at A1J5-10. If the Digital Output Driver is on, the input of the Digital Input Buffer is the voltage at the output of the Digital Output Driver.

The Digital Input Threshold circuit and resistor network A1Z1 determine the input threshold voltage and hysteresis for inverting comparator A1U3. The inverting input of the comparator (A1U3-13) is protected by a series resistor (A1Z3) and diode A1CR14. A negative input clamp circuit (A1Q9, A1Z2, and A1CR17) sets a clamp voltage of approximately +0.7V dc for the protection diodes of all Digital Input Buffers. A negative input voltage at A1J5-10 causes A1CR14 to conduct current, clamping the comparator input A1U3-13 at approximately 0V dc.

The input threshold of +1.4V dc and a hysteresis of +0.5V dc are used for all Digital Input Buffers. When the input of the Digital Input Buffer is greater than approximately +1.25V dc, the output of the inverting comparator is low. When the input then drops below about +0.75V dc, the output of the inverting comparator goes high.

DIGITAL AND ALARM OUTPUT DRIVERS 2A-45.

Since the 12 Digital Output and Alarm Output Drivers are identical in design, the following example description references only the components that are used for Alarm Output Driver 0.

The Microprocessor controls the state of Alarm Output Driver 0 by writing to the Alarm Output register in the FPGA (A1U25) to set the level of output A1U25-63. When A1U25-63 is set high, the output of the open-collector Darlington driver (A1U17-16) sinks current through current-limiting resistor A1R62. When A1U25-63 is set low, the driver output turns off and is pulled up by A1Z2 and/or the voltage of the external device that the output is driving. If the driver output is driving an external inductive load, the internal flyback diode (A1U17-9) conducts the energy into MOV A1RV1 to keep the driver output from being damaged by excessive voltage. Capacitor A1C58 ensures that the instrument meets electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance requirements.

TOTALIZER INPUT 2A-46.

The Totalizer Input circuit consists of Input Protection, a Digital Input Buffer circuit, and a Totalizer Debouncing circuit. The Digital Input Buffer for the totalizer is protected from electrostatic discharge (ESD) damage by A1R49 and A1C43. Refer to the detailed description of the Digital Input Buffer circuit for more information.

The Totalizer Debounce circuit in the FPGA (A1U25) allows the Microprocessor to select totalizing of either the input signal or the debounced input signal. The buffered Totalizer Input signal (TOTI*) goes into the FPGA at A1U25-12. Inside the FPGA, the totalizer signal is routed to the Totalizer Output (TOTO, A1U25-8) which then goes to a 16-bit counter in the Microprocessor (A1U1-114; TP20).

The actual debouncing of the input signal is accomplished by A1U25. Counters divide the 12.288-MHz system clock down to 128 kHz for the debouncing circuit. An EXOR gate compares the input signal (TOTI*) and the latched output of the debouncer. If these signals differ, the EXOR gate output goes high, enabling the debouncer. If the input remains stable for 1.75 milliseconds, the totalizer output (TOTO, A1U25-8) changes state. If the input does not remain stable for 1.75 milliseconds, the totalizer output does not change state. For a stable totalizer input of +5V dc, the totalizer output (TOTO, A1U25-8) will be 0.0V dc. For a stable totalizer input of +0.0V dc, the totalizer output (TOTO, A1U25-8) will be +5V dc.

EXTERNAL TRIGGER INPUT CIRCUITS 2A-47.

The External Trigger Input circuit can be configured by the Microprocessor to interrupt on a rising or falling edge of the XT* input (A1J6-2) or to not interrupt on any transitions of the XT* input. The falling edge of the XT* input is used by the instrument firmware as an indication to start scanning, and the rising edge is used as an indication to stop scanning.

The External Trigger Input is pulled up to +5V dc by A1Z2 and is protected from electrostatic discharge (ESD) damage by A1R58, A1C54, A1Z3, and A1CR15. Capacitor A1C54 helps ensure that the instrument meets EMI/EMC performance requirements.

The input (XTI) is then routed to the FPGA (A1U25), which contains the External Trigger control circuitry. The Microprocessor sets control register bits in the FPGA (A1U25) to control the external trigger circuit. The External Trigger control circuit output (A1U25-9) drives the non-maskable interrupt on the Microprocessor (A1U1-95).

If External Triggering is enabled (see User Manual), the Microprocessor sets FPGA control register bits to allow a low level on the XT* input to cause the External Trigger Interrupt (XTINT*; A1U25-9) to go low. The Microprocessor then changes the FPGA control register bits to allow a high level on the XT* input to cause XTINT* (A1U25-9) to go low. Thus the Microprocessor can detect both rising and falling edges on the XT* input. Normally, the XTINT* output of the FPGA (A1U25-9) should be low only for a few microseconds at any time. If it is held low constantly, the instrument will not be able to operate. Resistor A1R64 pulls the XTINT* output high to ensure that it is high during power-up.

A/D Converter PCA 2A-48.

The following paragraphs describe the operation of the circuits on the A/D Converter PCA. The schematic for this pca is located in Section 8.

ANALOG MEASUREMENT PROCESSOR 2A-49.

Refer to Figure 2A-3 for an overall picture of the Analog Measurement Processor chip and its peripheral circuits. Table 2A-4 describes Analog Measurement Processor chip signal names.

The Analog Measurement Processor (A3U8) is a 68-pin CMOS device that, under control of the A/D Microcontroller (A3U9), performs the following functions:

- Input signal routing
- Input signal conditioning
- Range switching
- Passive filtering of dc voltage and resistance measurements
- Active filtering of ac voltage measurements
- A/D conversion
- Support for direct volts, true rms ac volts, temperature, resistance, and frequency measurements

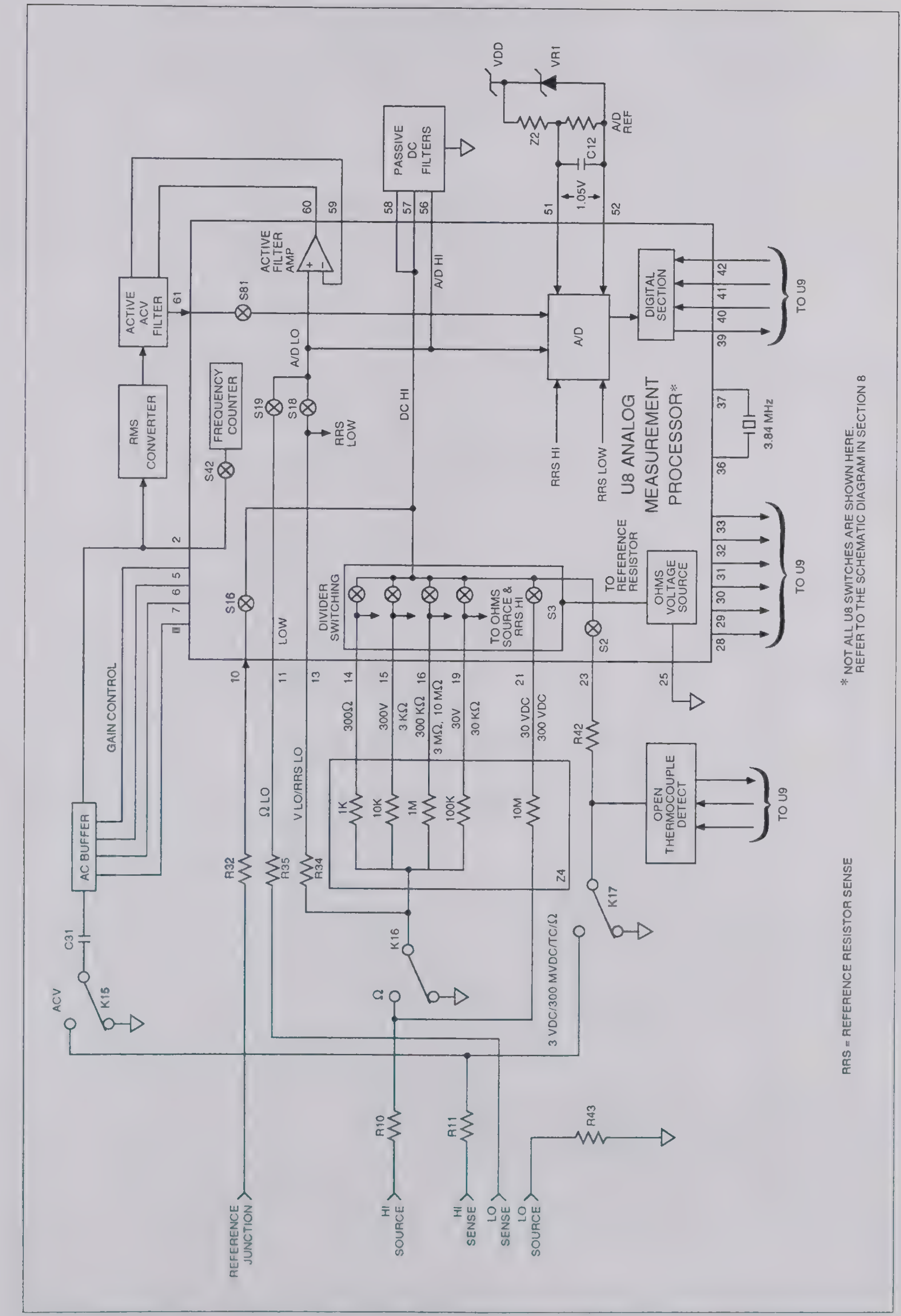

ACTIVE ACV FILTER
RMS CONVERTER
FREQUENCY COUNTER
ACTIVE FILTER AMP
PASSIVE DC FILTERS
VDD
VR1
Z2
C12
A/D REF
1.05V
A/D
DIGITAL SECTION
TO U9
U8 ANALOG MEASUREMENT PROCESSOR*
3.84 MHz
RRS HI
RRS LOW
A/D HI
A/D LO
DC HI
S81
S42
S19
S18
S16
S3
S2
RRS LOW
LOW
DIVIDER SWITCHING
TO OHMS SOURCE & RRS HI
TO REFERENCE RESISTOR
OHMS VOLTAGE SOURCE
OPEN THERMOCOUPLE DETECT
GAIN CONTROL
AC BUFFER
C31
ACV
K15
K16
K17
Ω
Ω LO
V LO/RRS LO
R32
R35
R34
R42
R10
R11
R43
Z4
1K
10K
1M
100K
10M
300Ω
300V
3 KΩ
300 KΩ
3 MΩ, 10 MΩ
30V
30 KΩ
30 VDC
300 VDC
3 VDC/300 MVDC/TC/Ω
2
5
6
7
8
10
11
13
14
15
16
19
21
23
25
28
29
30
31
32
33
36
37
39
40
41
42
51
52
56
57
58
59
60
61
REFERENCE JUNCTION
HI SOURCE
HI SENSE
LO SENSE
LO SOURCE
* NOT ALL U8 SWITCHES ARE SHOWN HERE. REFER TO THE SCHEMATIC DIAGRAM IN SECTION 8
RRS = REFERENCE RESISTOR SENSE

Figure 2A-3. Analog Simplified Schematic Diagram

Table 2A-4. Analog Measurement Processor Pin Descriptions

PIN	NAME	DESCRIPTION
1	VDD	+5.4V supply
2	ACBO	AC buffer output
3	AIN	(not used)
4	AGND2	Analog ground
5	ACR4	AC buffer range 4 (300V)
6	ACR3	AC buffer range 3 (30V)
7	ACR2	AC buffer range 2 (3V)
8	ACR1	AC buffer range 1 (300 mV)
9	VSSA	-5.4V supply for AC ranging
10	REFJ	Reference junction input
11	D C V LOW	A/D converter low input
12	GRD	Driven guard
13	RRS	Reference resistor sense for ohms
14	V4	Tap #4 on the DCV input divider/ohms reference network
15	V3	Tap #3 on the DCV input divider/ohms reference network
16	V1	Tap #1 on the DCV input divider/ohms reference network
17	GRD	Driven guard
18	V2F	Tap #2 input on the DCV input divider/ohms reference network
19	V2	Tap #2 on the DCV input divider/ohms reference network
20	GRD	Driven guard
21	V0	Tap #0 on the DCV input divider/ohms reference network
22	GRD	Driven guard
23	OVS	Ohms and volts sense input
24	GRD	Guard
25	AGND1	Analog ground
26	-	(not used)
27	DGND	Analog ground
28	FC0	Function control #0
29	FC1	Function control #1
30	FC2	Function control #2
31	FC3	Function control #3
32	FC4	(not used)
33	FC5	(not used)
34	FC6	Function control #6
35	FC7	Function control #7
36	XIN	Crystal oscillator input
37	XOUT	Crystal oscillator output
38	MRST	Master reset
39	AS	Analog send
40	AR	Analog receive

Table 2A-4. Analog Measurement Processor Pin Descriptions (cont)

PIN	NAME	DESCRIPTION
41	SK	Serial clock
42	CS	Chip select
43	BRS	(not used)
44	VSS	-5.4V dc
45	INT	Integrator output
46	SUM	Integrator summing node
47	B.1	Buffer output, 100 mV range
48	B.32	Buffer output, 300 mV range
49	B1	Buffer output, 1000 mV range
50	B3.2	Buffer output, 3V range
51	VREF+	A/D voltage reference plus
52	VREF-	A/D voltage reference minus
53	RAO	A/D reference amplifier output
54	RA+	A/D reference amplifier noninverting input
55	RA-	A/D reference amplifier inverting input
56	AFO	Passive filter 2
57	MOF	Passive filter 1 plus resistance
58	AFI	Passive filter 1
59	FAI	Filter amplifier inverting input
60	FAO	Filter amplifier output
61	RMSF	RMS output, filtered
62	AGND3	(not used, connected to filtered -5.4V dc)
63	RMSG2	(not used)
64	RMSO	RMS converter output
65	CAVG	(not used)
66	VSSR	-5.4V dc, filtered
67	RMSG1	(not used, pulled to filtered -5.4V dc)
68	RMSI	(not used)

Two separate signal paths are used, one for dc/ohms/temperature and one for ac. The volts dc (3V range and below) and temperature voltages are coupled directly to the a/d converter, while higher voltages are attenuated first. For ohms, the dc circuitry is augmented with an internal ohms source voltage regulator controlled through an extra set of switches. For volts ac, inputs are routed through the ac buffer, which uses the gain selected by the Measurement Processor (A3U8).

The a/d converter uses a modified dual-slope minor cycle method. The basic measurement unit, a minor cycle, consists of a fixed time integrate period for the unknown input, a variable time reference integrate period, a variable time hold period, and various short transition periods. A minor cycle period lasts for 25 ms or until a new minor cycle is begun, whichever comes first.

INPUT PROTECTION 2A-50.

The instrument measurement circuits are protected when overvoltages are applied through the following comprehensive means:

- Any voltage transients on channel 0 HI or LO terminals are immediately clamped to a peak of about 1800V or less by MOVs A3RV1 and A3RV2. (This is much lower than the 2500V peaks that can be expected on 240 VAC, IEC 664 Installation Category II, ac mains.)
- Fusible resistors A3R10 and A3R11 protect the measurement circuitry in all measurement modes by limiting currents.
- A3Q11 clamps voltages exceeding 0.7V below and approximately 6.0V above analog common (LO) or LO SENSE, with A3R35 limiting the input current.
- A3Q10 clamps voltages during ohms measurements with A3RT1, A3R34, A3R10, and A3Z4 limiting the input current. With large overloads, thermistor A3RT1 will heat up and increase in resistance.
- A3U8 also clamps voltages on its measurement input pins that exceed the VDD and VSS supply rails. Resistors A3R42, A3R11, A3R10, A3RT1, A3Z4, A3R35, and A3R34 limit any input currents.
- Any excessive voltages that are clamped through A3U8 to VDD or VSS, are then also clamped by zener diodes A3VR3 and A3VR2.
- The open thermocouple detect circuitry is protected against voltage transient damage by A3Q14 and A3Q15.
- When measuring ac volts, the ac buffer is protected by dual-diode clamp A3CR1 and resistor network A3Z3.
- Switching induced transients are also clamped by dual-diode A3CR4 and capacitor A3C33, and limited by resistor A3R33.

INPUT SIGNAL CONDITIONING 2A-51.

Each input is conditioned and/or scaled to a dc voltage appropriate for measurement by the a/d converter. DC voltage applied to the a/d converter can be handled on internal ranges of 0.1V, 0.3V, 1V, or 3V. Therefore, high-voltage dc inputs are scaled, and ohms inputs are converted to a dc voltage. Line voltage level ac inputs are first scaled and then converted to a dc voltage. Noise rejection is provided by passive and active filters.

Function Relays 2A-52.

Latching relays A3K15, A3K16, and A3K17 route the input signal to the proper circuit blocks to implement the desired measurement function. These relays are switched when a 6-millisecond pulse is applied to the appropriate reset or set coil by the NPN Darlington drivers in IC A3U10. The A/D Microcontroller A3U9 controls the relay drive pulses by setting the outputs of port 6. Since the other end of the relay coil is connected to the VDDR supply, a magnetic field is generated, causing the relay armature and contacts to move to (or remain in) the desired position. Function relay states are defined in Table 2A-5.

Table 2A-5. Function Relay States

RELAY POSITION			
FUNCTION	A3K17	A3K16	A3K15
DC mV, 3V, Thermocouples	Reset	Set	Set
DC 30V, 300V	Set	Set	Set
ACV	Set	Set	Reset
Ohms, RTDs	Reset	Reset	Set
Frequency	Set	Set	Reset

DC Volts and Thermocouples 2A-53.

For the 3V and lower ranges (including thermocouples), the HI input signal is applied directly to the A3U8 analog processor through A3R11, A3K17, and A3R42. Capacitor A3C27 filters this input, which the analog processor then routes through S2 and other internal switches, through the passive filter, and to the internal a/d converter. The LO SENSE signal is applied to A3U8 through A3R35 and routed through internal switch A3U8-S19 to LO of the a/d converter.

Guard signals MGRD and RGRD are driven by an amplifier internal to A3U8 to a voltage appropriate for preventing leakage from the input HI signal under high humidity conditions.

For the 30V range, the HI signal is scaled by resistor network A3Z4. Here, the input is applied to pin 1 of A3Z4 so that an approximate 100:1 divider is formed by the 10-MΩ and 100.5-kΩ resistors in A3Z4 when analog processor switches S3 and S13 are closed. The attenuated HI input is then sent through internal switch S12 to the passive filter and the a/d converter. Input LO is sensed through analog processor switch S18 and resistor A3R34.

For the 300V range (Figure 2A-4), the HI signal is again scaled by A3Z4. The input is applied to pin 1 of A3Z4, and a 1000:1 divider is formed by the 10-MΩ and 10.01-kΩ resistors when switches S3 and S9 are closed in A3Z4. The attenuated HI input is then sent through internal switch S10 to the passive filter and the a/d converter. LO is sensed through analog processor switch S18 and resistor A3R34.

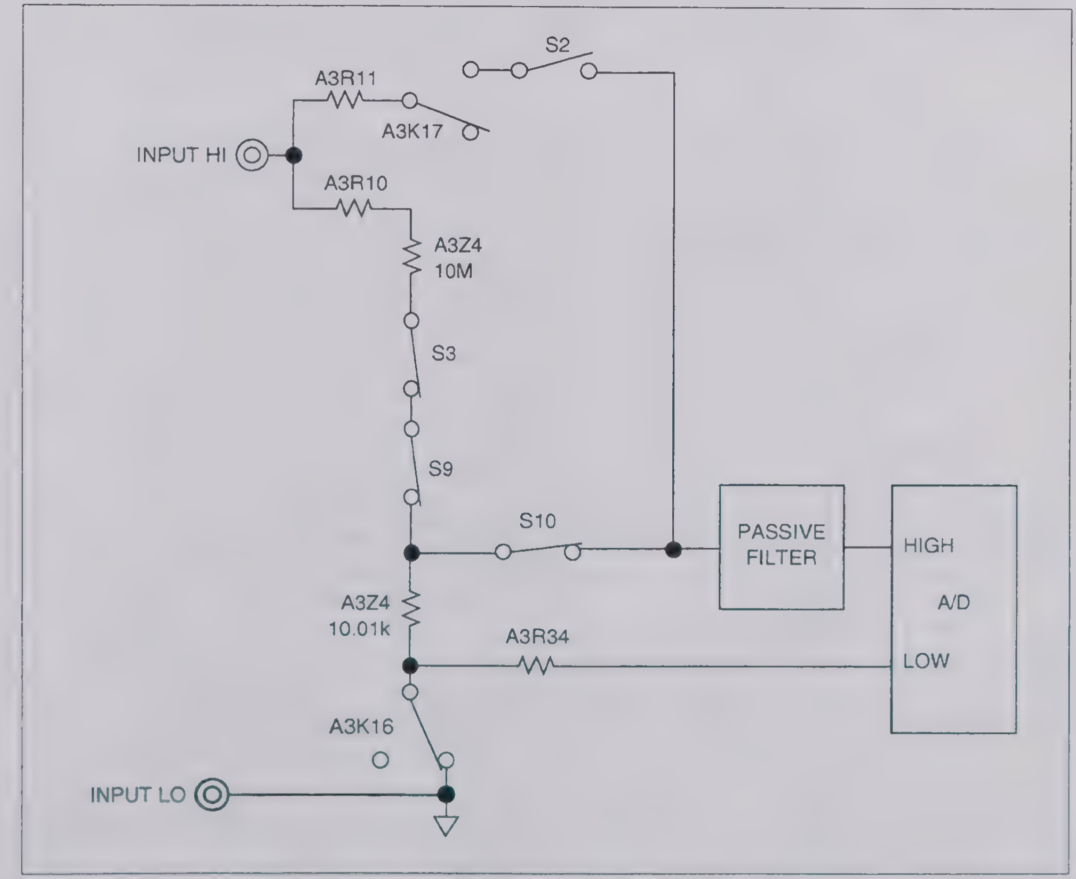


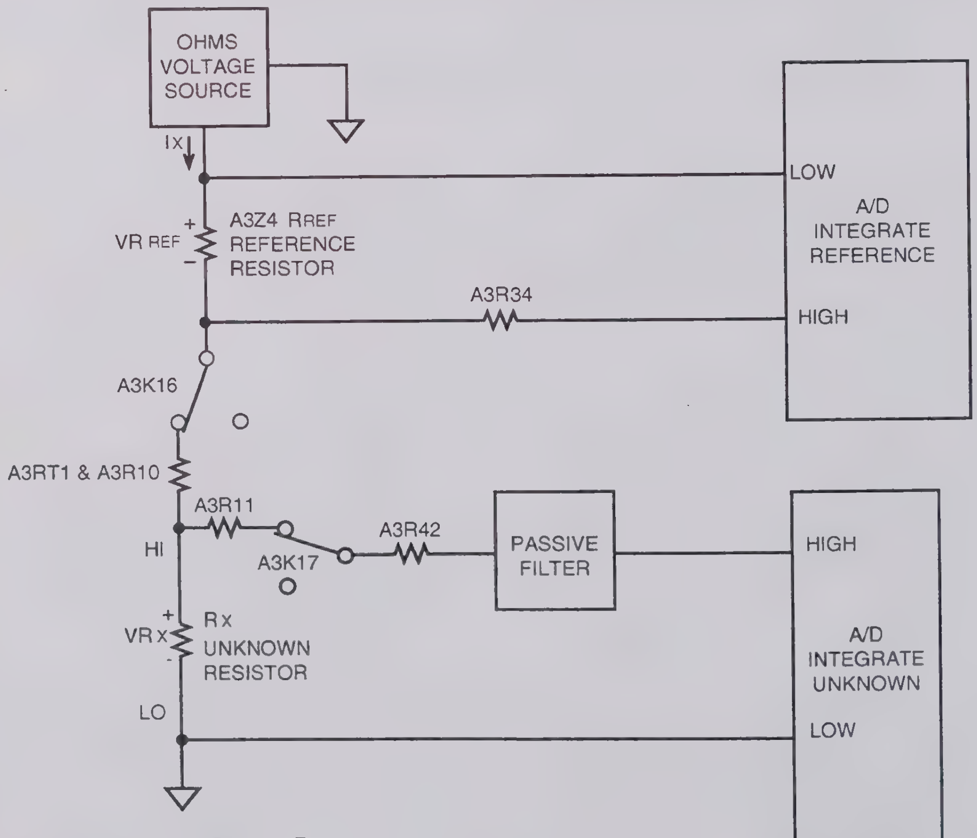
Figure 2A-4. DC Volts 300V Range Simplified Schematic

Ohms and RTDs 2A-54.

Resistance measurements are made using a ratio ohms technique, as shown in Figure 2A-5. A stable voltage source is connected in series with the reference resistor in A3Z4 and the unknown resistor. Since the same current flows through both resistors, the unknown resistance can be determined by multiplying the ratio of the voltage drops across the reference and the unknown resistors by the known reference resistor value.

For the RTD, 300Ω, 3-kΩ, and 30-kΩ ranges, the ratio technique is implemented by integrating the voltage across the unknown resistance for a fixed period of time and then integrating the negative of the voltage across the reference resistance for a variable time period. In this way, each minor cycle result gives the ratio directly.

For the 300-kΩ, 3-MΩ, and 10-MΩ ranges, the ratio is determined by performing two separate voltage measurements in order to improve noise rejection. One fixed-period integration is performed on the voltage across the unknown resistance, and the second integration is performed on the voltage across the reference resistance. The ratio of the two fixed-period voltge measurements is then computed by Microcontroller A3U9. The resistance measurement result is determined when A3U9 multiplies the ratio by the reference resistance value.


OHMS VOLTAGE SOURCE
Ix
+
VR REF
−
A3Z4 RREF REFERENCE RESISTOR
LOW
A/D INTEGRATE REFERENCE
A3R34
HIGH
A3K16
A3RT1 & A3R10
A3R11
HI
A3K17
A3R42
PASSIVE FILTER
HIGH
+
VR X
-
Rx UNKNOWN RESISTOR
A/D INTEGRATE UNKNOWN
LO
LOW

$$\frac{VR_X}{VR_{REF}} = \frac{I_X \bullet R_X}{I_X \bullet R_{REF}} = \frac{R_X}{R_{REF}}$$

Figure 2A-5. Ohms Simplified Schematic

When an input is switched in for a measurement, the ohms source in Analog Processor A3U8 is set to the correct voltage for the range selected and is connected to the appropriate reference resistor in network A3Z4. A measurement current then flows through A3Z4, relay A3K16, thermistor A3RT1, resistor A3R10, the unknown resistance, A3R43, ground, and the ohms source.

The resulting voltage across the unknown resistance is integrated for a fixed period of time by the A/D Converter through the HI SENSE path of A3R11, A3K17, A3R42 and A3U8 switch S2, and the LO SENSE path of A3R35 and Analog Processor switch S19. Passive filtering is provided by A3C34, A3C27, and portions or all of the DC Filter block.

The voltage across the reference resistor for the 300Ω and RTD, 3-kΩ, and 30-kΩ ranges (the 1-kΩ, 10.01-kΩ, and 100.5-kΩ resistances in A3Z4, respectively) is integrated for a variable period of time until the voltage across the integrate capacitor reaches zero. For the 300Ω and RTD range, the reference resistor voltage is switched in through Analog Processor switch S6 and applied to the A/D Converter by switch S8. For the 3-kΩ range, switches S9 and S11 perform these functions, respectively. For the 30-kΩ range, switches S13 and S14 are used. For all ranges, the voltage is routed through A3R34 to the RRS input.

The reference resistor for the 300-kΩ, 3-MΩ, and 10-MΩ ranges is the 1-MΩ resistor in A3Z4, which is selected by S15. The voltage across this reference is integrated during its own minor cycle(s) and is switched to a passive filter and the A/D Converter by switches S1 and S18.

When 4-wire measurements are made on any of the six ranges, separate Source and Sense signal paths are maintained to the point of the unknown resistance. The 4-wire Source path measurement current is provided by the A3U8 ohms source through one of the A3U8 internal switches (S6, S9, S13, or S15) and the appropriate reference resistor in A3Z4. The current flows through relay A3K16, thermistor A3RT1, resistor A3R10, the HI Source instrument relay contacts (A3K1 - A3K3, A3K5 - A3K14), and the HI Source lead wire, to the unknown resistance to be measured. The current flows back through the LO Source lead wire, the LO Source path of the instrument relays (A3K1 - A3K3, A3K5 - A3K14), resistor A3R43, and analog ground, to the A3U8 ohms source.

The voltage that develops across the unknown resistance is sensed through the other 2 wires of the 4-wire set. HI is sensed through the HI Sense path made up of the users HI Sense lead wire, the HI Sense contacts in the instrument relays, resistor A3R11, relay A3K17, resistor A3R42, and Analog Processor A3U8 switch S2. LO is sensed through the users LO Sense lead wire, the LO Sense contacts in the instrument relays, protection resistor A3R35, and A3U8 switch S19.

Since virtually no current flows through the sense path, no error voltages are developed that would add to the voltage across the unknown resistance; this 4-wire measurement technique eliminates user lead-wire and instrument relay contact and circuit board trace resistance errors.

AC Volts 2A-55.

AC-coupled ac voltage inputs are scaled by the ac buffer, converted to dc by a true rms ac-to-dc converter, filtered, and then sent to the a/d converter.

Refer to Figure 2A-6. Input HI is switched to the ac buffer by dc-blocking capacitor A3C31, protection resistor A3R11, and latching relay A3K15. Resistor A3R44 and A3K15 act to discharge A3C31 between channel measurements. LO is switched to the A3U8 A/D Converter through A3R34 and S18.

JFETs A3Q3 through A3Q9 select one of the four gain (or attenuation) ranges of the buffer (wide-bandwidth op-amp A3U7.) The four JFET drive signals ACR1 through ACR4 turn the JFETs on at 0V and off at -VAC. Only one line at a time will be set at 0 volts to select a range.

The input signal to the buffer is first divided by 10, 100, or 1000 for the 300 mV, 3V, and 30V ranges, respectively. The resistance ratios used are summarized in Table 2A-6. Note that the 111.1-kΩ resistor is left in parallel with the smaller (higher attenuation) resistors. The attenuated signal is then amplified by A3U7, which is set for a gain of 25 by the 2.776-kΩ and 115.7Ω resistors in A3Z3. Components A3R27 and A3C23 compensate high-frequency performance on the 300 mV range. For the 300V range, overall buffer gain is determined by the ratio of the 2.776-kΩ feedback resistor to the 1.111-MΩ input resistor.

The output of the buffer is ac-coupled by A3C15 and A3C16 to the true-rms ac-to-dc converter A3U6. Discharge JFET A3Q13 is switched on to remove any excess charge from the coupling capacitors A3C15 and A3C16 between channel measurements. A3C17 provides an averaging function for the converter, and resistor network A3Z1 divides the output by 2.5 before sending the signal to the active ac volts filter. Analog processor switch S81 connects the output of the active filter to HI of the A/D Converter.

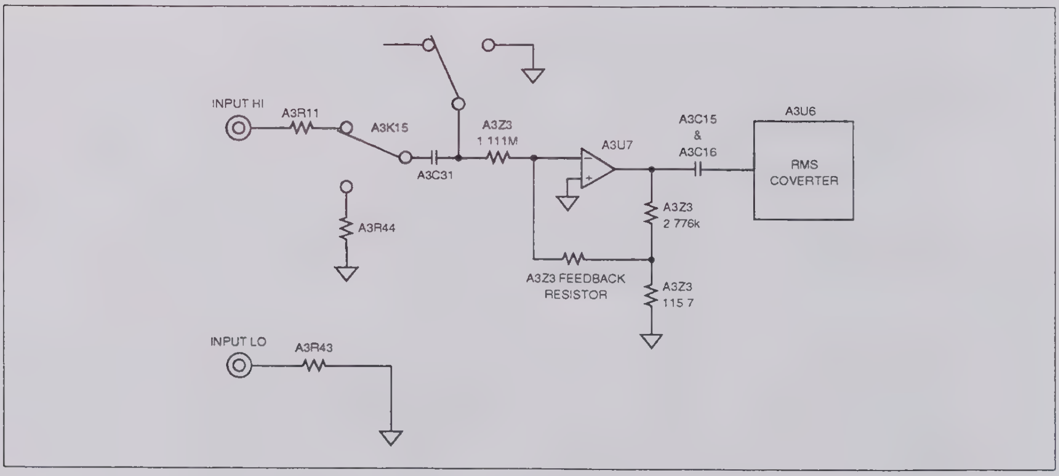


Figure 2A-6. AC Buffer Simplified Schematic

Table 2A-6. AC Volts Input Signal Dividers

RANGE	DRIVE SIGNAL	A3Z3 DIVIDER RESISTOR(S)	OVERALL GAIN
300 mV	ACR1	111.1 kΩ	2.5
3V	ACR2	12.25 kΩ ‖ 111.1 kΩ	0.25
30V	ACR3	1.013 kΩ ‖ 111.1 kΩ	0.025
150/300V	ACR4	none	0.0025

Components A3R29, A3R30, A3C26, and A3C28 provide filtered power supplies (+VAC and -VAC) for the ac buffer, the ac switch JFETs, and the rms converter.

Frequency 2A-56.

After any dc component is blocked by capacitors A3C15, A3C16, and A3C31, the output of the ac buffer is used to determine the input frequency. This signal is sent to the ACBO pin of analog processor A3U8 and switched to the internal frequency comparator and counter circuit by S42.

PASSIVE AND ACTIVE FILTERS 2A-57.

The passive filters are used for the dc voltage and ohms measurements. For most ranges, capacitors A3C14 and A3C11 are switched into the measurement circuit in front of the A3U8 A/D Converter by switches S86, S87, and S88. These capacitors act with the 100-kΩ series resistance provided by A3R42 or A3Z4 to filter out high-frequency noise. For the 300-kΩ range, only A3C14 is switched in by switches S86 and S85. For the 3-MΩ and 10-MΩ ranges, A3C11 or A3C14 are not switched in to keep settling times reasonably short.

Between channel measurements, the passive filters are discharged by JFET A3Q2 under control of Microcontroller A3U9 through comparator A3U14. When the ZERO signal is asserted, A3R14 pulls the gate of A3Q2 to ground, turning the JFET on and discharging A3C11. At the same time, zeroing of filter capacitors A3C14 and A3C27 is accomplished by having the Analog Processor turn on internal switches S2, S86, and S87.

The active filter is only used for ac voltage measurements. This three-pole active filter removes a significant portion of the ac ripple and noise present in the output of the rms converter without introducing any additional dc errors. The active filter op-amp within A3U8, resistors A3R20, A3R17, and A3R16, and capacitors A3C7, A3C10, and A3C6 form the filter circuit. This filter is referenced to the LO input to the a/d converter within A3U8 by the op-amp. The input to the filter is available at the RMSO pin, and the output is sent to the RMSF pin of A3U8. Switches S80 and S82, which are turned on prior to each new channel measurement, cause the filter to quickly settle (pre-charge) to near the proper dc output level.

A/D CONVERTER 2A-58.

Figure 2A-7 shows the dual slope a/d converter used in the instrument. The unknown input voltage is buffered and used to charge (integrate) a capacitor for an exact period of time. This integrator capacitor is then discharged by the buffered output of a stable and accurate reference voltage of opposite polarity. The capacitor discharge time, which is proportional to the level of the unknown input signal, is measured by the digital circuits in the Analog Measurement Processor. This time count becomes the conversion result.

In both the slow and fast measurement rates, the a/d converter uses its ±300 mV range for most measurement functions and ranges. The primary exceptions are that the 3V dc range is measured on the a/d converter 3V range, thermocouples are measured on the ±100 mV range, and the temperature reference is measured on the 1V a/d converter range. The typical overload point on a slow rate 30000 count range is 32000 display counts; the typical overload point on a fast rate 3000 count range is 3200 display counts.

During the integrate phase, the a/d buffer in the A3U8 Analog Measurement Processor applies the signal to be measured to one of the four integrator input resistors in network A3Z2. As shown on the A/D Converter schematic diagram in Section 8, the choice of resistor selects the a/d converter range. Switch S69 connects the buffer output through pin B.1 for the 100-mV range, S71 connects the output through B.32 for the 300 mV range, S73 connects to pin B1 for the 1V range, and S75 sets up the 3V range through pin B3.2.

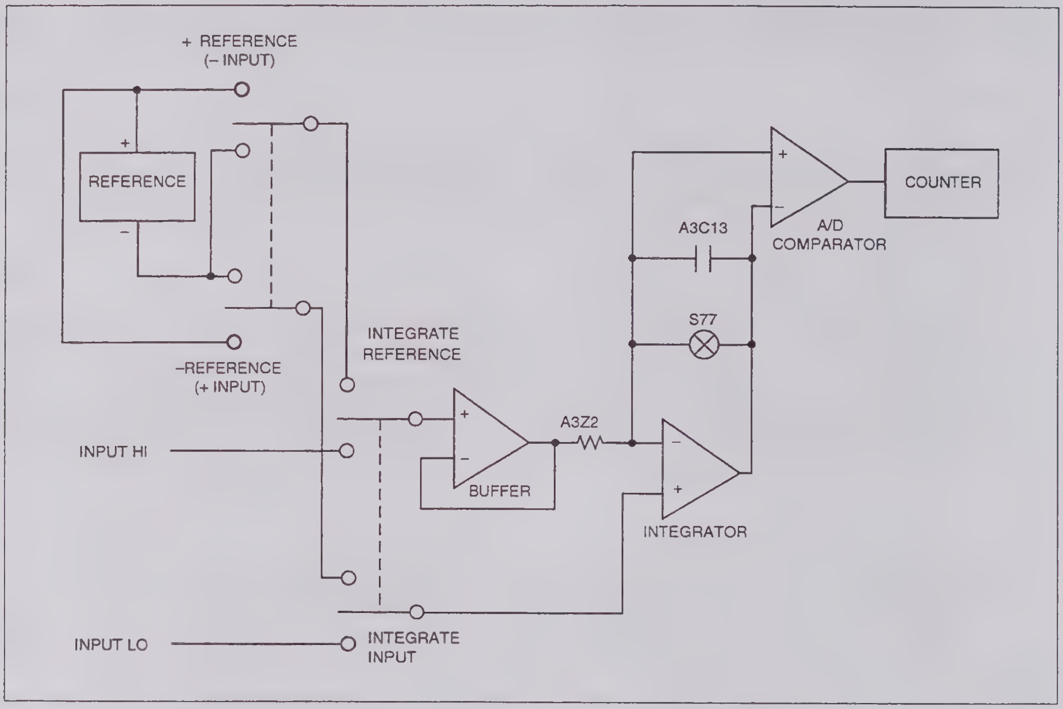


Figure 2A-7. A/D Converter Simplified Schematic

The current through the selected integrator input resistor charges integrator capacitor A3C13, with the current dependent on the buffer output voltage. After the integrate phase, the buffer is connected to the opposite polarity reference voltage, and the integrator integrates back toward zero capacitor voltage until the comparator trips. An internal counter measures this variable integrate time. If the a/d converter input voltage is too high, the integrator overloads and does not return to its starting point by the end of the measurement phase. Switch S77 is then turned on to discharge integrate capacitor A3C13.

The reference voltage used during the variable integrate period for voltage (and high ohms) conversions is generated from zener reference diode A3VR1, which is time and temperature stable. The reference amplifier in the Analog Measurement Processor, along with resistors A3R15, A3R18, and A3R21, pulls approximately 2 mA of current through the zener. Resistors in network A3Z2 divide the zener voltage down to the reference 1.05V required by the A/D Converter.

INGUARD MICROCONTROLLER CIRCUITRY 2A-59.

The Microcontroller, A3U9, with its internal program memory and RAM and associated circuitry, controls measurement functions on the A/D Converter PCA and communicates with the Main (outguard) processor.

The Microcontroller communicates directly with the A3U8 Analog Measurement Processor using the CLK, CS, AR, and AS lines and can monitor the state of the analog processor using the FC[0:7] lines. Filter zeroing is controlled by the ZERO signal. The open thermocouple detect circuitry is controlled by the OTCCLK and OTCEN lines and read by the OTC line. The Microcontroller also communicates with the Main (outguard) processor serially using the IGDR line to receive and the IGDS line (driven by A3Q1) to send.

The channel and function relays are driven to the desired measurement state by signals sent out through microcontroller ports 1, 3, 4, 6, and 7.

On power up, the reset/break detect circuit made up of quad comparator A3U1, capacitors A3C1 and A3C2, and resistors A3R1 through A3R6 and A3R8 resets the Microcontroller through the RESET* line. When a break signal is received from the outguard processor, the inguard A3U9 is again reset. Therefore, if Microcontroller operation is interrupted by line transients, the outguard can regain control of the inguard by resetting A3U9.

CHANNEL SELECTION CIRCUITRY 2A-60.

Measurement input channel selection is accomplished by a set of latching 4-form-C relays organized in a tree structure. Relays A3K5, A3K6, and A3K8 through A3K14 select among channels 1 through 20. Relay A3K7 disconnects rear input channels 1 through 20 from the measurement circuitry between measurements. Relay A3K3 switches in the front panel channel 0 or the rear channels. Inductors A3L1 through A3L24 reduce EMI and current transients.

Selection between 2-wire and 4-wire operation for ohms measurements is performed by latching 2-form-C relays (A3K1 and A3K2.) These relays also serve to select a voltage or thermocouple rear input channel from either channels 1 through 10 or channels 11 through 20.

The coils for the relays are driven by the outputs of Darlington drivers A3U4, A3U5, A3U10, A3U11, and A3U12. The relays are switched when a 6-millisecond pulse is applied to the appropriate reset or set coil by the NPN Darlington drivers in these ICs. When the port pin of Microcontroller A3U9 connected to the input of a driver is set high, the output of the driver pulls one end of a relay set or reset coil low. Since the other end of the relay coil is connected to the VDDR supply, a magnetic field is generated, causing the relay armature and contacts to move to (or remain in) the desired position.

OPEN THERMOCOUPLE CHECK 2A-61.

Immediately before a thermocouple measurement, the open thermocouple check circuit applies a small, ac-coupled signal to the thermocouple input. Microcontroller A3U9 initiates the test by asserting OTCEN, causing comparator A3U14/A3R40 to turn on JFET A3Q12. Next, the Microcontroller sends a 78-kHz square wave out the OTCCLK line through A3R41, A3Q12, and A3C32 to the thermocouple input. The resulting waveform is detected by A3U13 and A3CR2, and a proportional level is stored on capacitor A3C30. Op amp A3U13 compares this detected level with the VTH threshold voltage set up by A3R37 and A3R36 and stored on A3C29. If the resistance at the input is too large, the VTH level will be exceeded and the OTC (open thermocouple check) line will be asserted. After a short delay, the Microcontroller analyzes this OTC signal, determines whether the thermocouple should be reported as open, and deasserts OTCEN and sets OTCCLK high, ending the test.

Input Connector PCA 2A-62.

The Input Connector assembly, which plugs into the A/D Converter PCA from the rear of the instrument, provides 20 pairs of channel terminals for connecting measurement sensors. This assembly also provides the reference junction temperature sensor circuitry used when making thermocouple measurements.

Circuit connections between the Input Connector and A/D Converter PCAs are made via connectors A4P1 and A4P2. Input channel and earth ground connections are made via A4P1, while temperature sensor connections are made through A4P2.

Input connections to channels 1 through 20 are made through terminal blocks TB1 and TB2. Channel 1 and 11 HI and LO terminals incorporate larger creepage and clearance distances and each have a metal oxide varistor (MOV) to earth ground in order to clamp voltage transients. MOVs A4RV1 through A4RV4 limit transient impulses to the more reasonable level of approximately 1800V peak instead of the 2500V peak that can be expected on 240 VAC, IEC 664 Installation Category II, ac mains. In this way, higher voltage ratings can be applied to channels 1 and 11 than can be applied to the other rear channels.

Strain relief for the user's sensor wiring is provided both by the Connector PCA housing and the two round pin headers. Each pin of the strain relief headers is electrically isolated from all other pins and circuitry.

Temperature sensor transistor A4Q1 outputs a voltage inversely proportional to the temperature of the input channel terminals. This voltage is 0.6V dc at 25 °C, increasing 2 mV with each degree decrease in temperature, or decreasing 2 mV with each degree increase in temperature. For high accuracy, A4Q1 is physically centered within and thermally linked to the 20 input terminals. Local voltage reference A4VR1 and resistors A4R1 through A4R3 set the calibrated operating current of the temperature sensor. Capacitor A4C1 shunts noise and EMI to ground.

Display PCA

2A-63.

Display Assembly operation is classified into six functional circuit blocks: the Main PCA Connector, the Front Panel Switches, the Display, the Beeper Drive Circuit, the Watchdog Timer/Reset Circuit, and the Display Controller. These blocks are described in the following paragraphs.

MAIN PCA CONNECTOR

2A-64.

The 20-pin Main PCA Connector (A2J1) provides the interface between the Main PCA and the other functional blocks on the Display PCA. Seven of the connector pins provide the necessary connections to the four power supply voltages. (See the following table.)

POWER SUPPLY	A2J1 PINS	NOMINAL VOLTAGE
VCC	8	+5.0V dc
VEE	6	-5.0V dc
VLOAD	7	-30V dc
FIL1 to FIL2	2 to 3	5.4V ac

Six pins are used to provide the interface to the Front Panel Switches (A2SWR1 through A2SWR6). The other seven signals interface the Microprocessor (A1U1) to the Display Controller (A2U1) and pass the reset signals between the assemblies.

FRONT PANEL SWITCHES

2A-65.

The FPGA scans the 19 Front Panel Switches (A2S1 through A2S18, and A2S21) using only six interface signals (plus the ground connection already available from the power supply). These six signals (SWR1 through SWR6) are connected to bidirectional I/O pins on the FPGA. Each successive column has one less switch.

This arrangement allows the unused interface signals to function as strobe signals when their respective column is driven by the FPGA. The FPGA cycles through six steps to scan the complete Front Panel Switch matrix. Table 2A-7 shows the interface signal state and, if the signal state is an output, the switches that may be detected as closed.

In step 1, six I/O pins are set to input, and the interface signal values are read. In steps 2 through 6, the pin listed as O is set to output zero, the other pins are read, and pins indicated by a Z are ignored.

Each of the interface signals is pulled up to the +5V dc supply by a 10-kΩ resistor in network A2Z1. Normally, the resistance between any two of the interface signals is approximately 20 kΩ. Checking resistances between any two signals (SWR1 through SWR6) verifies proper termination by resistor network A2Z1.

DISPLAY 2A-66.

The custom vacuum-fluorescent display (A2DS1) comprises a filament, 11 grids (numbered 0 through 10 from right to left on the display), and up to 14 anodes under each grid. The anodes make up the digits and annunciators for their respective area of the display. The grids are positioned between the filament and the anodes.

A 5.4V ac signal, biased at a -24V dc level, drives the filament. When a grid is driven to +5V dc, the electrons from the filament are accelerated toward the anodes that are under that grid. Anodes under that grid that are also driven to +5V dc are illuminated, but the anodes that are driven to -30V dc are not. Grids are driven to +5V dc one at a time, sequencing from GRID(10) to GRID(0) (left to right, as the display is viewed.)

BEEPER DRIVE CIRCUIT 2A-67.

The Beeper Drive circuit drives the speaker (A2LS1) to provide an audible response to a button press. A valid entry yields a short beep; an incorrect entry yields a longer beep.

The circuitry comprises a dual four-bit binary counter (A2U4) and a NAND gate (A2U6) used as an inverter. One four-bit free-running counter (A2U4) divides the 1.024-MHz clock signal (E) from the FPGA (DSCLK) by 2 to generate the 512-kHz clock (CLK1) used by the Display Controller. This counter also divides the 1.024-MHz clock by 16, generating the 64-kHz clock that drives the second four-bit binary counter (A2U4).

Table 2A-7. Front Panel Switch Scanning

INTERFACE SIGNAL STATES OR KEY SENSED						
Step	SWR6	SWR5	SWR4	SWR3	SWR2	SWR1
1	A2S8	A2S17	A2S10	A2S12	A2S18	A2S13
2	A2S1	A2S2	A2S3	A2S4	A2S11	0
3	A2S7	A2S9	A2S5	A2S6	0	Z
4	A2S14	A2S15	A2S16	0	Z	Z
5	n/a	n/a	0	Z	Z	Z
6	A2S21	0	Z	Z	Z	Z

A2Sn indicates switch closure sensed.
0 indicates strobe driven to logic 0
Z indicates high impedance input; state ignored.

The second four-bit counter is controlled by an open-drain output on the Display Controller (A2U1-17) and pull-down resistor A2R1. When the beeper (A2LS1) is off, A2U1-17 is pulled to ground by A2R1. This signal is then inverted by A2U6, with A2U6-6 driving the CLR input high to hold the four-bit counter reset. Output A2U4-8 of the four-bit counter drives the parallel combination of the beeper (A2LS1) and A2R10 to ground to keep the beeper silent. When commanded by the Microprocessor, the Display Controller drives A2U1-17 high, enabling the beeper and driving the CLR input of the four-bit counter (A2U4-12) low. A 4-kHz square wave then appears at counter output A2U4-8 and across the parallel combination of A2LS1 and A2R10, causing the beeper to resonate.

WATCHDOG TIMER AND RESET CIRCUIT 2A-68.

The Watchdog Timer and Reset circuit has been defeated by the insertion of the jumper between TP1 and TP3 on the Display Assembly. In this instrument, the reset circuitry is on the Main Assembly and the Watchdog Timer is part of the Microprocessor (A1U1).

The Display Reset signal (DRST*) drives the RESET2* signal on the Display Assembly low when the instrument is being reset. This discharges capacitor A2C3, and NAND gate output A2U6-11 provides an active high reset signal to the Display Processor. The Watchdog Timer on the Display Assembly (A2U5, A2U6 and various resistive and capacitive timing components) is held "cleared" by TP1 being held at 0V dc by a jumper, and output A2U5-12 will always be high.

DISPLAY CONTROLLER 2A-69.

The Display Controller is a four-bit, single-chip microcomputer with high-voltage outputs that are capable of driving a vacuum-fluorescent display directly. The controller receives commands over a three-wire communication channel from the Microprocessor on the Main Assembly. Each command is transferred serially to the Display Controller on the display transmit (DISTX) signal, with bits being clocked into the Display Controller on the rising edges of the display clock signal (DSCLK). Responses from the Display Controller are sent to the Microprocessor on the display receive signal (DISRX) and are clocked out of the Display Controller on the falling edge of DSCLK.

Series resistor A2R11 isolates DSCLK from A2U1-40, preventing this output from trying to drive A1U1-77 directly. Figure 2A-8 shows the waveforms during a single command byte transfer. Note that a high DISRX signal is used to hold off further transfers until the Display Controller has processed the previously received byte of the command.

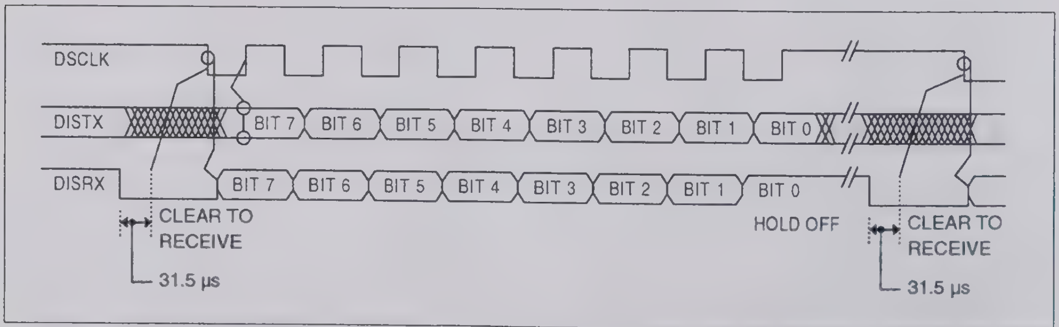


Figure 2A-8. Command Byte Transfer Waveforms

Once reset, the Display Controller performs a series of self-tests, initializing display memory and holding the DISRX signal high. After DISRX goes low, the Display Controller is ready for communication. On the first command byte from the Microprocessor, the Display Controller responds with a self-test results response. If all self-tests pass, a response of 00000001 (binary) is returned. If any self-test fails, a response of 01010101 (binary) is returned. The Display Controller initializes its display memory to one of four display patterns depending on the states of the DTEST* (A2U1-41) and LTE* (A2U1-13) inputs. The DTEST* input is pulled up by A2Z1, but may be pulled down by jumpering A2TP4 to A2TP3 (GND). The LTE* input is pulled down by A2R12, but may be pulled up by jumpering A2TP5 to A2TP6 (VCC). The default conditions of DTEST* and LTE* cause the Display Controller to turn all segments on bright at power-up.

Table 2A-8 defines the logic and the selection process for the four display initialization modes.

The two display test patterns are a mixture of on and off segments forming a recognizable pattern that allows for simple testing of display operation. Test patterns #1 and #2 are shown in Section 5 of this manual.

The Display Controller provides 11 grid control outputs and 15 anode control outputs. (Only 14 anode control outputs are used.) Each of these 26 high-voltage outputs provides an active driver to the +5V dc supply and a passive 220-kΩ (nominal) pull-down to the -30V dc supply. These pull-down resistances are internal to the Display Controller.

The Display Controller provides multiplexed drive to the vacuum-fluorescent display by strobing each grid while the segment data for that display area is present on the anode outputs. Each grid is strobed for approximately 1.37 milliseconds every 16.56 milliseconds, resulting in each grid on the display being strobed about 60.4 times per second. The grid strobing sequence is from GRID(10) to GRID(0), which results in left-to-right strobing of grid areas on the display. Figure 2A-9 shows grid control signal timing.

The single grid strobing process involves turning off the previously enabled grid, outputting the anode data for the next grid, and then enabling the next grid. This procedure ensures that there is some time between grid strobes so that no shadowing occurs on the display. A grid is enabled only if one or more anodes are also enabled. Thus, if all anodes under a grid are to be off, the grid is not turned on. Figure 2A-10 describes the timing relationship between an individual grid control signal and the anode control signals.

Table 2A-8. Display Initialization Modes

A2TP4 DTEST*	A2TP5 LTE*	Power-Up Display Initialization
1	1	All Segments OFF
1	0	All Segments ON (default)
0	1	Display Test Pattern #1
0	0	Display Test Pattern #2

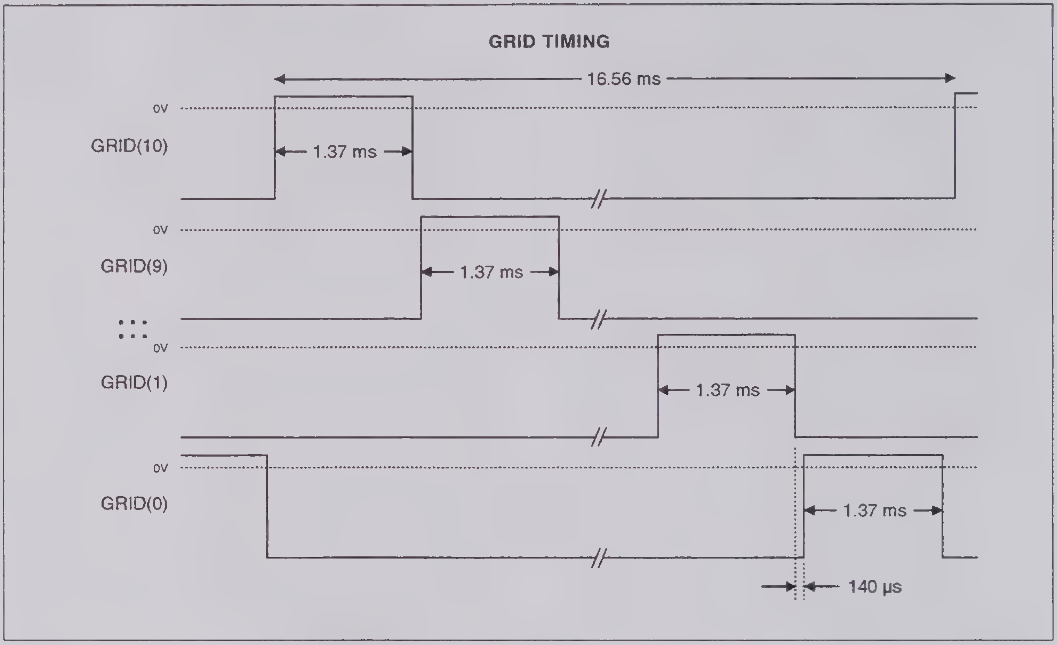

GRID TIMING
16.56 ms
0V
GRID(10)
1.37 ms
0V
GRID(9)
1.37 ms
0V
GRID(1)
1.37 ms
0V
GRID(0)
1.37 ms
140 µs

Figure 2A-9. Grid Control Signal Timing

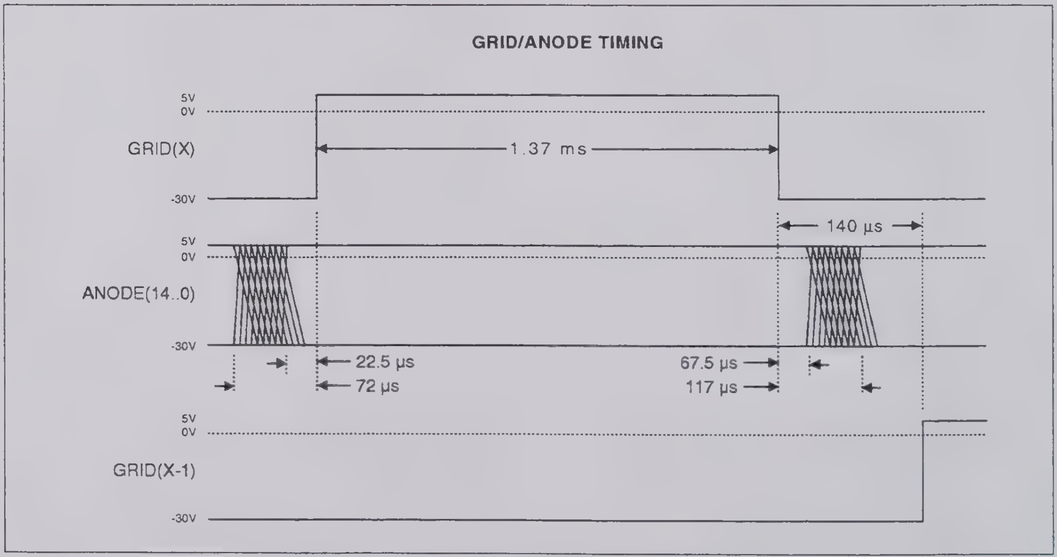

GRID/ANODE TIMING
5V
0V
GRID(X)
1.37 ms
-30V
140 µs
5V
0V
ANODE(14..0)
-30V
22.5 µs
72 µs
67.5 µs
117 µs
5V
0V
GRID(X-1)
-30V

Figure 2A-10. Grid-Anode Timing Relationships

Memory Card Interface PCA 2A-70.

The Memory Card Interface Assembly operation is composed of four functional circuit blocks: the Main PCA Connector, the Microprocessor Interface, the Memory Card Controller, and the PCMCIA Memory Card Connector. These blocks are described in the following paragraphs.

MAIN PCA CONNECTOR 2A-71.

The Memory Card Interface PCA interfaces to the Main PCA through a 40-pin, right angle connector (A6P2). This connector routes eight bits of the Microprocessor data bus, the lower four bits of the address bus, memory control, and interrupt and address decode signals from the Main PCA to the Memory Card Interface PCA. The Memory Card Interface PCA is powered by the +5.0V dc power supply (VCC). The pinout of the high density ribbon cable that connects the Main PCA to the Memory Card Interface PCA is carefully selected to prevent cross-talk between signals and to provide low impedance connections to the VCC power supply.

MICROPROCESSOR INTERFACE 2A-72.

The timing of Microprocessor read and write accesses to the Memory Card Controller (A6U1) are controlled by the Wait State Timing Controller (A6U3). The Memory Card Controller (A6U1) determines whether wait states are required when the Microprocessor accesses one of its internal registers.

When a register in the Memory Card Controller (A6U1) is read, the four address bits select one of the 16 registers to read, and the XMCARD* signal (A6U1-34) is driven to a low level by the Microprocessor. The XRDU* signal (A6U1-36) is then driven low by A1U11-14 to enable the data outputs from the Memory Card Controller (XD8 through XD15). At the end of the read access, both XMCARD* and XRDU* are driven high again.

When a register in the Memory Card Controller (A6U1) is written, the four address bits select one of the 16 registers to write, and the XMCARD* signal (A6U1-34) is driven to a low level by the Microprocessor. The XWRU* signal (A6U1-37) is then driven low by A1U11-13 to initiate the transfer of the data bus inputs on the Memory Card Controller (XD8 through XD15) to the internal register. At the end of the write access, both XMCARD* and XRDU* are driven high again, and the data is latched into the internal register.

If no wait states are required, the WAIT* signal (A6U1-39) will remain high through the entire read or write access to the Memory Card Controller. The Wait State Timing Controller will drive the DTACK* signal (A6U3-19) low after the next low to high transition of the system clock (A6U3-1) to indicate to the Microprocessor that the data transfer has been acknowledged, and the read or write access may be completed. The DTACK* signal is a tri-state bus that is pulled up to VCC by resistor A1R83 and pulled low by devices being accessed by the Microprocessor.

If wait states are required, the WAIT* signal (A6U1-39) will go low shortly after XMCARD* (A6U1-34) goes low during a read or write access to the Memory Card Controller. The Memory Card Controller then counts cycles of the system clock (A6U1-32 and A6U1-35) and when the correct number of wait states have been done, the WAIT* signal will go high. The Wait State Timing Controller will then drive the DTACK* signal (A6U3-19) low after the next low to high transition of the system clock (A6U3-1) to indicate to the Microprocessor that the data transfer has been acknowledged and the read or write access may be completed.

MEMORY CARD CONTROLLER 2A-73.

The Memory Card Controller provides a register-based interface for the Microprocessor to use to access data stored on industry standard PCMCIA memory cards. A 26-bit counter controls the address bus (CA<0> through CA<25>) to the PCMCIA Memory Card Connector (A6P1). A 16-bit data bus (CD<0> through CD<15>) and memory card control signals (REG*, CE1*, CE2*, CRD*, and CWR*) control accesses to memory on the card.

The REG* signal (A6U1-86) is like an additional address bit. When REG* is low (A6U1-86), read and write accesses go to "attribute" memory on the card. Attribute memory is typically a small EEPROM on the memory card that contains special information that specifies the manufacturer of the card, type and size of memory on the card, memory speed, etc. When REG* is high, read and write accesses go to the "common" memory on the card. Common memory is the Static RAM on the memory cards used in this instrument.

Typically, information is read and written to the memory card in a sequential manner where the address counter automatically increments after the end of each read or write cycle. When the Memory Card Controller reads data from the lower byte of the memory card data bus (CD<0> through CD<7>), CE1* (A6U1-2) goes low followed by CRD* (A6U1-9) going low. The data from the memory card then goes through the Memory Card controller and is read by the Microprocessor on the XD8 through XD15 data bus lines. When the Memory Card Controller reads data from the upper byte of the memory card data bus (CD<8> through CD<15>), CE2* (A6U1-3) goes low followed by CRD* (A6U1-9) going low. The data from the memory card then goes through the Memory Card controller and is read by the Microprocessor on the XD8 through XD15 data bus lines. Data is written to the memory card in a similar manner, except that the data goes from the Microprocessor through the Memory Card Controller and to the Memory Card with CWR* (A6U2-10) going low to enable the writing of the data to the memory. The purpose of A6U2 and resistors A6R2, A6R5, A6R6, and A6R7 is to ensure that data on the Memory Card is not accidentally modified during the time that the instrument is being powered up or down. Each of the Memory Card data bus lines (CD<0> through CD<15>) has a series resistor (A6R8, A6R9, A6Z2, and A6Z3) that helps ensure that the instrument meets EMI/EMC performance requirements.

The Memory Card Controller detects the insertion and removal of a Memory Card and interrupts the Microprocessor by driving the MCINT* signal (A6U1-112) low. When a Memory Card is inserted in the PCMCIA Memory Card Connector, the CD1 (A6U1-40) and CD2 (A6U1-38) inputs on the Memory Card Controller are driven to 0V dc, and Microprocessor (A1U1) is interrupted. The Microprocessor then powers up the Memory Card by setting A6U1-102 low, which turns on FET A6Q1 by driving the gate low through resistor A6R13. When FET A6Q1 is turned on, the Memory Card power (CVCC and CVPP) is approximately +5.0V dc. When the Microprocessor has completed a data transfer with the Memory Card, FET A6Q1 is turned off again by driving A6U1-102 high.

When a Memory Card is inserted and powered up, the Memory Card outputs some status signals to the Memory Card Controller. If the Memory Card write-protect switch is protecting data on the card, the WP signal (A6U1-97) is high. The status of the Memory Card battery is output on the BVD1 (A6P1-63) and BVD2 (A6P1-62) pins of the Memory Card Connector. If either of these battery status signals is low when the Memory Card is powered up, then the Microprocessor will turn on LED A6DS2 by driving A6U1-118 low. The Busy status LED (A6DS1) is turned on by driving A6U1-119 low when the Microprocessor has powered up the Memory Card and is transferring data to or from the card.

PCMCIA MEMORY CARD CONNECTOR 2A-74.

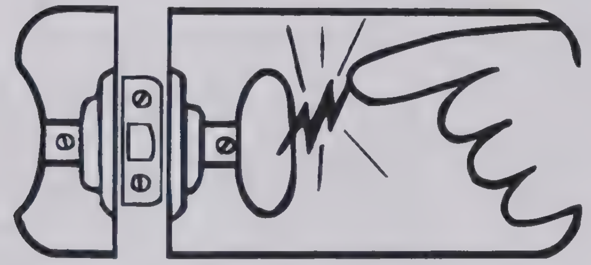
The PCMCIA Memory Card Connector (A6P1) is a 68-pin connector that meets the requirements of the Personal Computer Memory Card International Association. This connector has pins that are three different lengths: the card detection pins (CD1 and CD2) are the shortest, the power and ground pins are the longest, and the rest of the pins are a length in between. This ensures that on memory card insertion, the power and ground pins are mated first, followed by the reset of the input/output signals, with the card detection signals mating last. This sequence is reversed on memory card removal.

The PCMCIA Memory Card Connector has a metal shell that is connected to chassis ground to help ensure that the instrument meets EMI/EMC and ESD performance requirements. A push-button mechanism is included to allow easy ejection of the Memory Card.

static awareness

A Message From

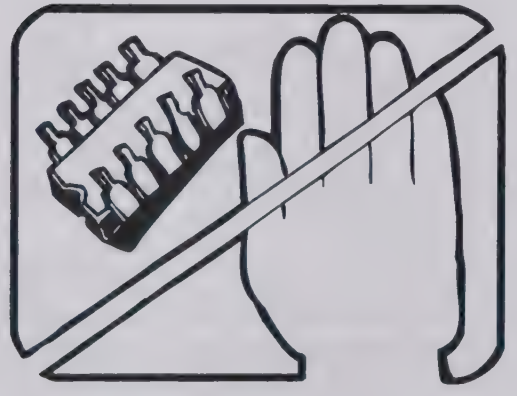
Fluke Corporation



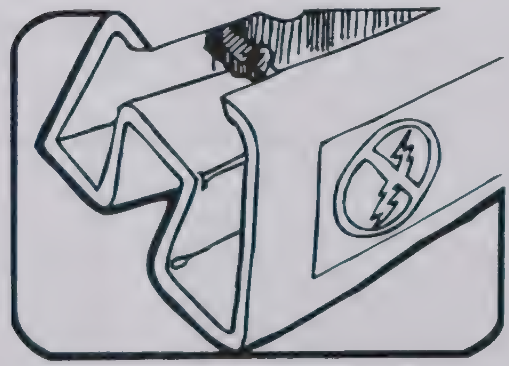
Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

1. Knowing that there is a problem.
2. Leaning the guidelines for handling them.
3. Using the procedures, packaging, and bench techniques that are recommended.

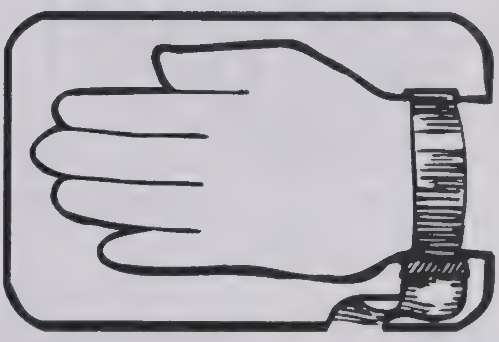
The following practices should be followed to minimize damage to S.S. (static sensitive) devices.



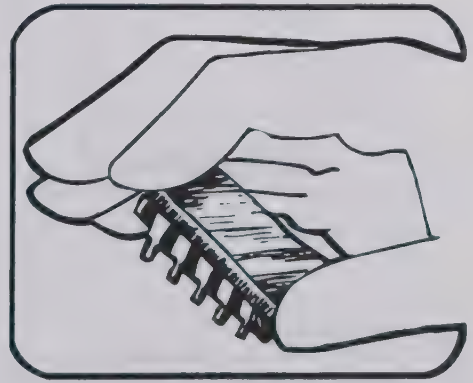
1. MINIMIZE HANDLING



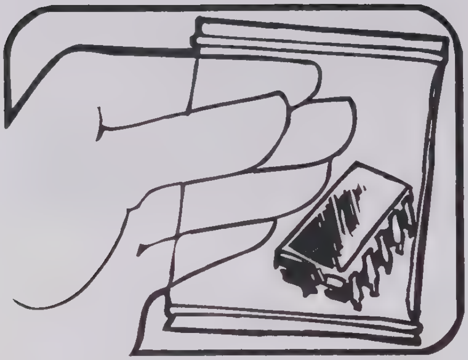
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



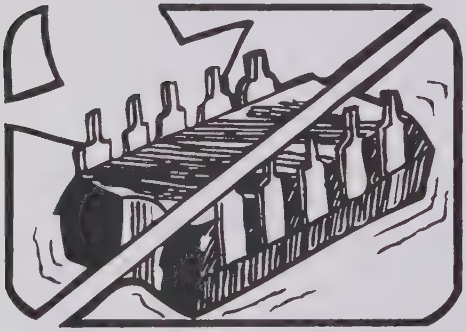
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES. USE A HIGH RESISTANCE GROUNDING WRIST STRAP.



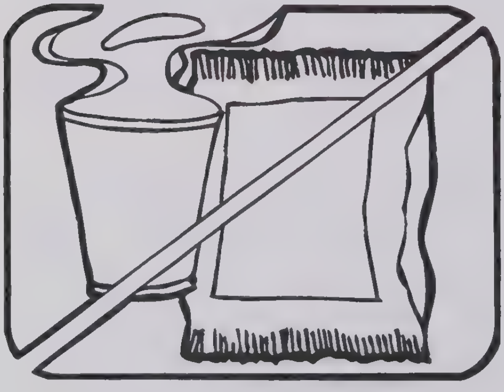
4. HANDLE S.S. DEVICES BY THE BODY.



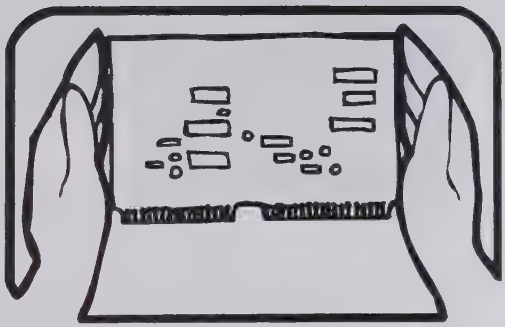
5. USE STATIC SHIELDING CONTAINERS FOR HANDLING AND TRANSPORT.



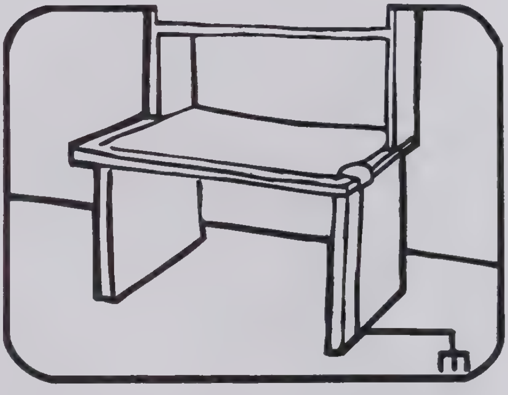
6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE.



7. AVOID PLASTIC,VINYL AND STYROFOAM® IN WORK AREA.



8. WHEN REMOVING PLUG-IN ASSEMBLIES HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR HELPS PROTECT INSTALLED S.S. DEVICES.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION.

10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.

11. ONLY GROUNDED-TIP SOLDERING IRONS SHOULD BE USED.

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Section 3

General Maintenance

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INTRODUCTION 3-1.

This section provides handling, cleaning, fuse replacement, disassembly, and assembly instructions.

WARRANTY REPAIRS AND SHIPPING 3-2.

If your instrument is under warranty, see the warranty information at the front of this manual for instructions on returning the unit. The list of authorized service facilities is included in Section 6.

GENERAL MAINTENANCE 3-3.

Required Equipment 3-4.

Equipment required for calibration, troubleshooting, and repair of the instrument is listed in Section 4 (Table 4-1.)

Refer to the Fluke "Surface Mount Device Soldering Kit" for a list of special tools required to perform circuit assembly repair. (In the USA, call 1-800-526-4731 to order).

Power Requirements 3-5.

WARNING

TO AVOID SHOCK HAZARD, CONNECT THE INSTRUMENT POWER CORD TO A POWER RECEPTACLE WITH EARTH GROUND.

If you have not already done so, plug the line cord into the connector on the rear of the instrument. The instrument operates on any line voltage between 90V ac and 264V ac and at any frequency between 45 and 440 Hz. However, the instrument is warranted only to meet published specifications at 50/60 Hz. The instrument also operates from dc power (9 to 16V dc). DC input power is connected to the rear input connector J6, pin 8 (DCH), and pin 7 (DCL). If both ac and dc power sources are connected to the instrument, the ac power source is used if the ac line voltage exceeds approximately 8.3 times the dc voltage. Automatic switchover between ac and dc occurs without interrupting instrument operation. The instrument draws a maximum of 10 VA on ac line power or 4W on dc power.

Static Safe Handling 3-6.

All integrated circuits, including surface mounted ICs, are susceptible to damage from electrostatic discharge (ESD). Modern integrated circuit assemblies are more susceptible to damage from ESD than ever before. Integrated circuits today can be built with circuit lines less than one micron thick, allowing more than a million transistors on a 1/4-inch square chip. These submicron structures are sensitive to static voltages under 100 volts. This much voltage can be generated on a dry day by simply moving your arm. A person can develop a charge of 2,000 volts by walking across a vinyl tile floor, and polyester clothing can easily generate 5,000 to 15,000 volts during movement against the wearer. These low voltage static problems are often undetected because a static charge must be in the 30,000 to 40,000 volt range before a person feels a shock.

Most electronic components manufactured today can be degraded or destroyed by ESD. While protection networks are used in CMOS devices, they merely reduce, not eliminate component susceptibility to ESD.

ESD may not cause an immediate failure in a component; a delayed failure or wounding effect is caused when the semiconductor's insulation layers or junctions are punctured. The static problem is thus complicated in that failure may occur anywhere from two hours to six months after the initial damage.

Two failure modes are associated with ESD. First, a person who has acquired a static charge can touch a component or assembly and cause a transient discharge to pass through the device. The resulting current ruptures the junctions of a semiconductor. The second failure mode does not require contact with another object. Simply exposing a device to the electric field surrounding a charged object can destroy or degrade a component. MOS devices can fail when exposed to static fields as low as 30 volts.

Observe the following rules for handling static-sensitive devices:

1. HANDLE ALL STATIC-SENSITIVE COMPONENTS AT A STATIC-SAFE WORK AREA.

   Use grounded static control table mats on all repair benches, and always wear a grounded wrist strap. Handle boards by their nonconductive edges only. Store plastic, vinyl, and Styrofoam objects outside the work area.

2. STORE AND TRANSPORT ALL STATIC-SENSITIVE COMPONENTS AND ASSEMBLIES IN STATIC SHIELDING BAGS OR CONTAINERS.

   Static shielding bags and containers protect components and assemblies from direct static discharge and external static fields. Store components in their original packages until they are ready for use.

Servicing Surface-Mount Assemblies 3-7.

Hydra incorporates Surface-Mount Technology (SMT) for printed circuit assemblies (pca's). Surface-mount components are much smaller than their predecessors, with leads soldered directly to the surface of a circuit board; no plated through-holes are used. Unique servicing, troubleshooting, and repair techniques are required to support this technology.

Refer to Section 5 for additional information. Also, refer to the Fluke "Surface Mount Device Soldering Kit" for a complete discussion of these techniques (in the USA, call 1-800-526-4731 to order).

CLEANING 3-8.

WARNING

TO AVOID ELECTRICAL SHOCK OR DAMAGE TO THE INSTRUMENT, NEVER ALLOW WATER INSIDE THE CASE. TO AVOID DAMAGING THE INSTRUMENT'S HOUSING, NEVER APPLY SOLVENTS TO THE INSTRUMENT.

If the instrument requires cleaning, wipe it down with a cloth that is lightly dampened with water or a mild detergent. Do not use aromatic hydrocarbons, chlorinated solvents, or methanol-based fluids when wiping the instrument. Dry the instrument thoroughly after cleaning.

LINE FUSE REPLACEMENT 3-9.

The line fuse (125 mA, 250V, slow blow, Fluke Part Number 822254) is located on the rear panel. The fuse is in series with the power supply. For replacement, unplug the line cord and remove the fuse holder (with fuse) as shown in Figure 3-1. The instrument is shipped with a replacement fuse loosely secured in the fuse holder.

DISASSEMBLY PROCEDURES 3-10.

The following paragraphs describe disassembly of the instrument in sequence from the fully assembled instrument to the chassis level. Start and end your disassembly at the appropriate heading levels.

WARNING

OPENING THE CASE MAY EXPOSE HAZARDOUS VOLTAGES. ALWAYS DISCONNECT THE POWER CORD AND MEASURING INPUTS BEFORE OPENING THE CASE. AND REMEMBER THAT REPAIRS OR SERVICING SHOULD BE PERFORMED ONLY BY QUALIFIED PERSONNEL.

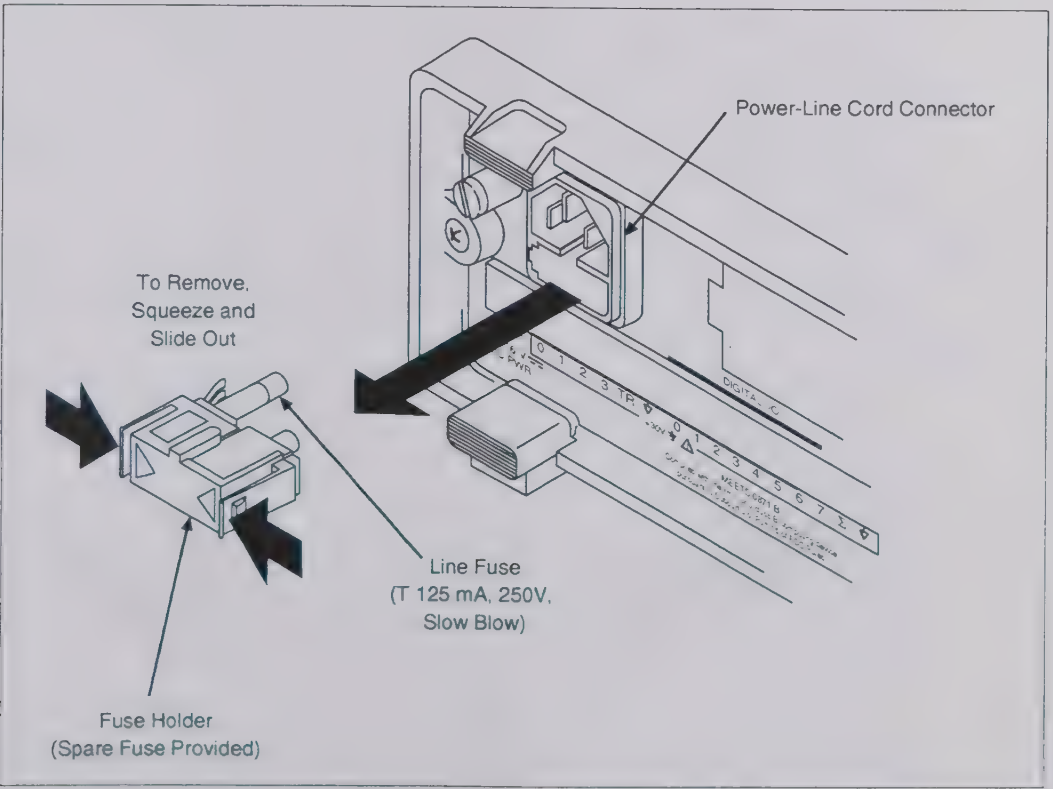

Power-Line Cord Connector
To Remove, Squeeze and Slide Out
Line Fuse (T 125 mA, 250V, Slow Blow)
Fuse Holder (Spare Fuse Provided)

Figure 3-1. Replacing the Line Fuse

Remove the Instrument Case 3-11.

Use the following procedure to remove the instrument case.

1. Make sure the instrument is powered off and disconnected from the power source (ac or dc).
2. Remove the screw from the bottom of the case, and remove the two screws from the rear bezel as shown in Figure 3-2. While holding the front panel, slide the case and rear bezel off the chassis. (At this point, the rear bezel is not secured to the case.)

Remove Handle and Mounting Brackets 3-12.

Refer to Figure 3-3 during this procedure. Pull each handle pivot out slightly at the handle mounting brackets, then rotate the handle up over the display. With the handle pointing straight up, pull out and disengage one pivot at a time.

Use a Phillips screwdriver to remove the two handle mounting brackets. Note that these brackets must be reinstalled in their original positions. Therefore, the inside of each bracket is labeled (R for right, L for left) as viewed from the front of the instrument.

Remove the Front Panel Assembly 3-13.

NOTE

Parts referenced by letter (e.g., **A***) are shown in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A).*

Use the following procedure to remove the Front Panel Assembly (E):

1. Remove the leads connected to the two input terminals. Using needle nose pliers, pull and disconnect the wires at the rear of the VΩ and COM input terminals.
2. Using needle nose pliers, disconnect the display ribbon cable (G) on the Main PCA (H) by alternately pulling up on each end of its connector. Avoid breaking the alignment tabs on the Main PCA side of this connection.
3. Remove the Front Panel Assembly by releasing the four snap retainers (I) securing it to the chassis. Using needle nose pliers, disconnect the display ribbon cable (G) on the Display PCA (K) by alternately pulling up on each end of its connector. Avoid breaking the alignment tabs on the Display PCA side of this connection. The ribbon cable (G) may be left attached to the chassis.
4. The green power switch activator rod (J) extending from the power switch on the Main PCA through the Front Panel Assembly can now be removed. Squeeze the end of the rod at the power switch and lift up; the bar disengages smoothly from the switch.

Remove the Display PCA 3-14.

Two movable tabs hold the Display PCA (K) in place on the back of the Front Panel Assembly. Release one tab at a time. Then, while prying slightly at the top of the Display PCA, lift the pca out of its securing slots. Parts referenced by letter (e.g., A) are shown in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A).

NOTE

The Display PCA provides a space for a center securing screw. If the two tabs are intact, this screw is not necessary. If a tab is broken, a screw can be used as an additional securing device.

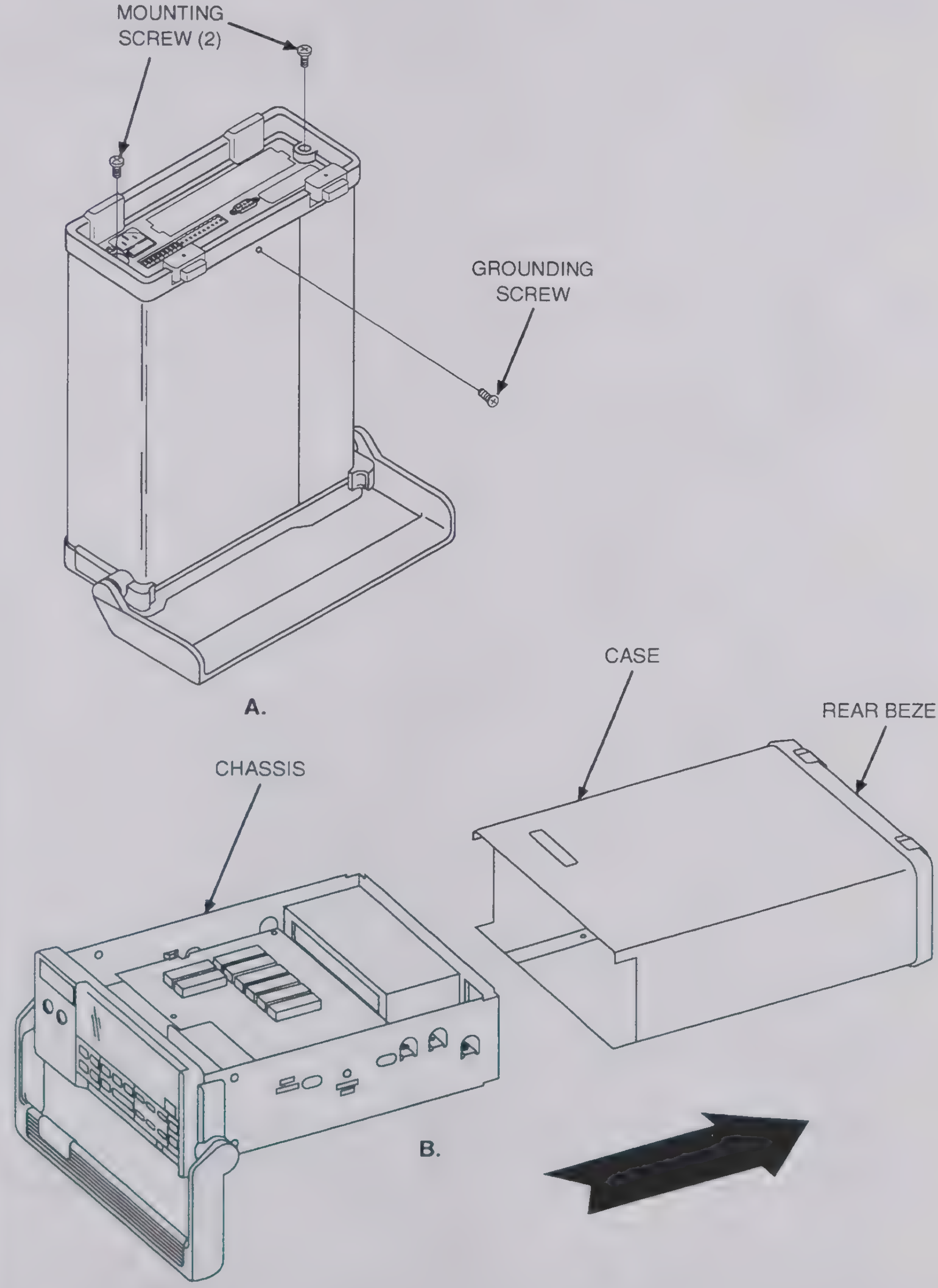

MOUNTING SCREW (2)
GROUNDING SCREW
A.
CASE
REAR BEZEL
CHASSIS
B.

Figure 3-2. Removing the Case

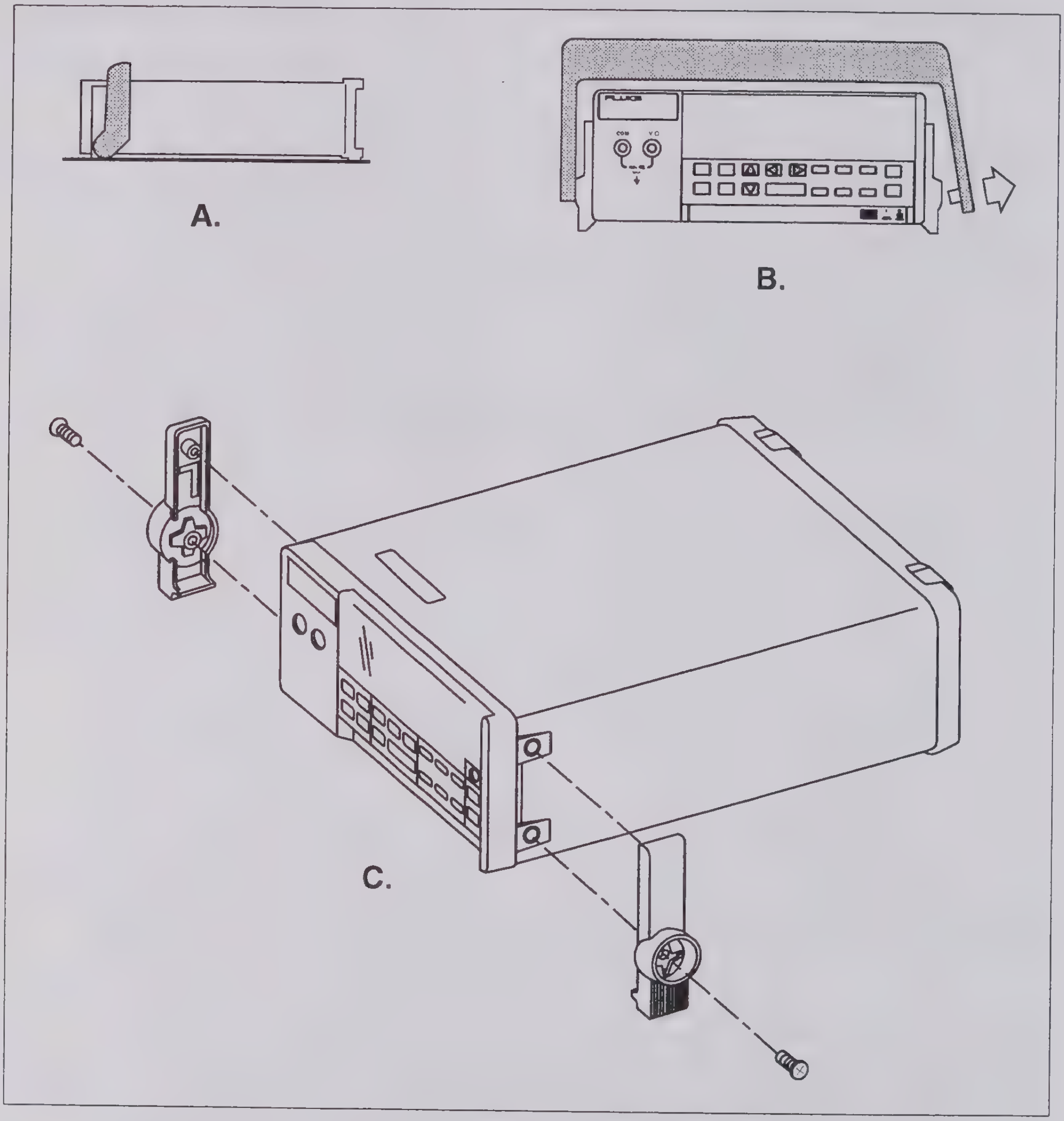


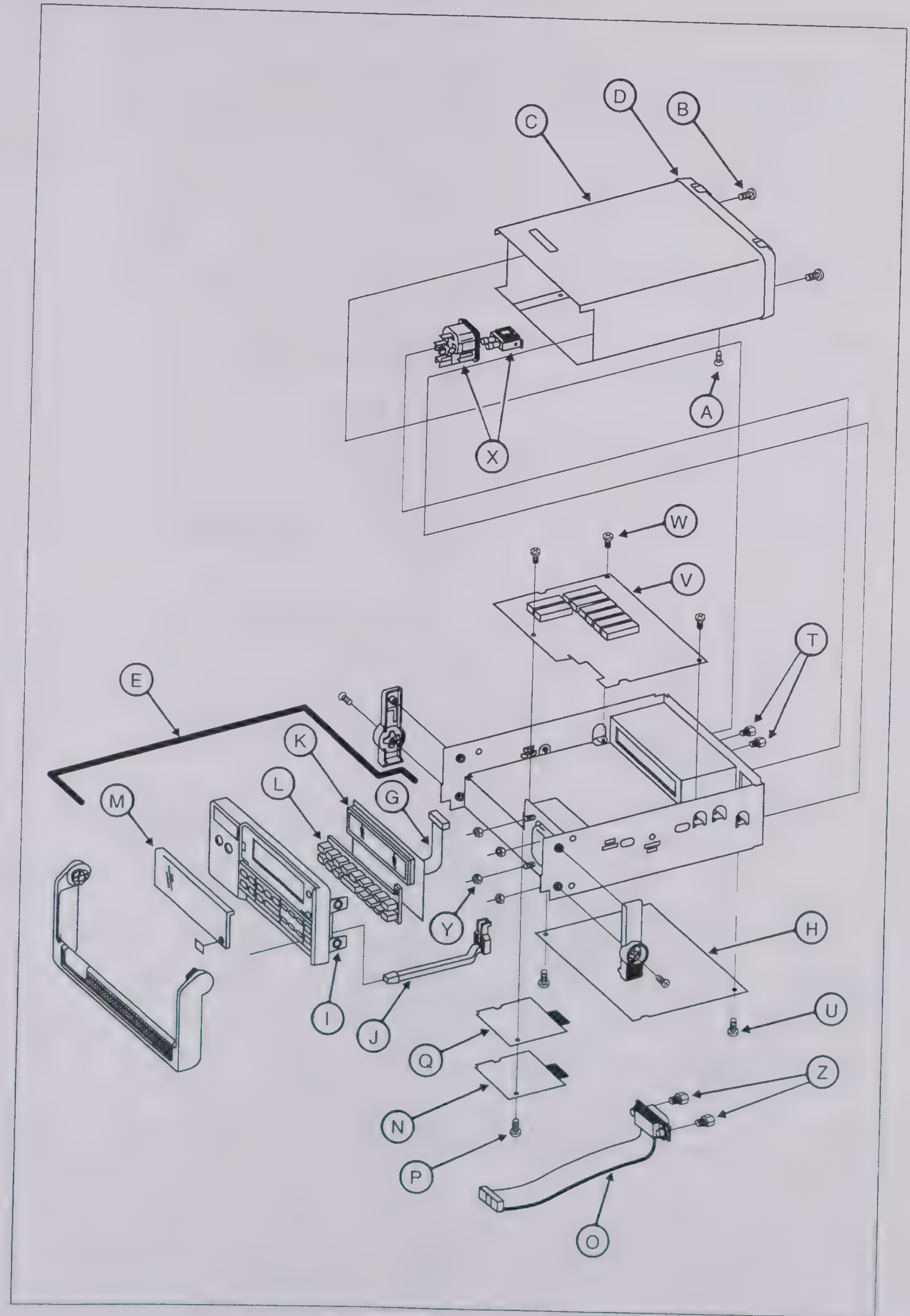
Figure 3-3. Removing the Handle and Handle Mounting Brackets

The elastomeric Keypad Assembly (L) can now be lifted away from the Front Panel Assembly.

Only if necessary, gently remove the display window (M) by releasing the two snaps along its inside, bottom edge. While pushing slightly on the rear of the window, gently lever each snap by pressing against an adjacent edge on the keypad housing.

CAUTION

Avoid using ammonia or methyl-alcohol cleaning agents on either the Front Panel or the display window. These types of cleaners can damage surface features and markings. Use an isopropyl-based cleaning agent or water to clean the Front Panel and the display window.


D
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W
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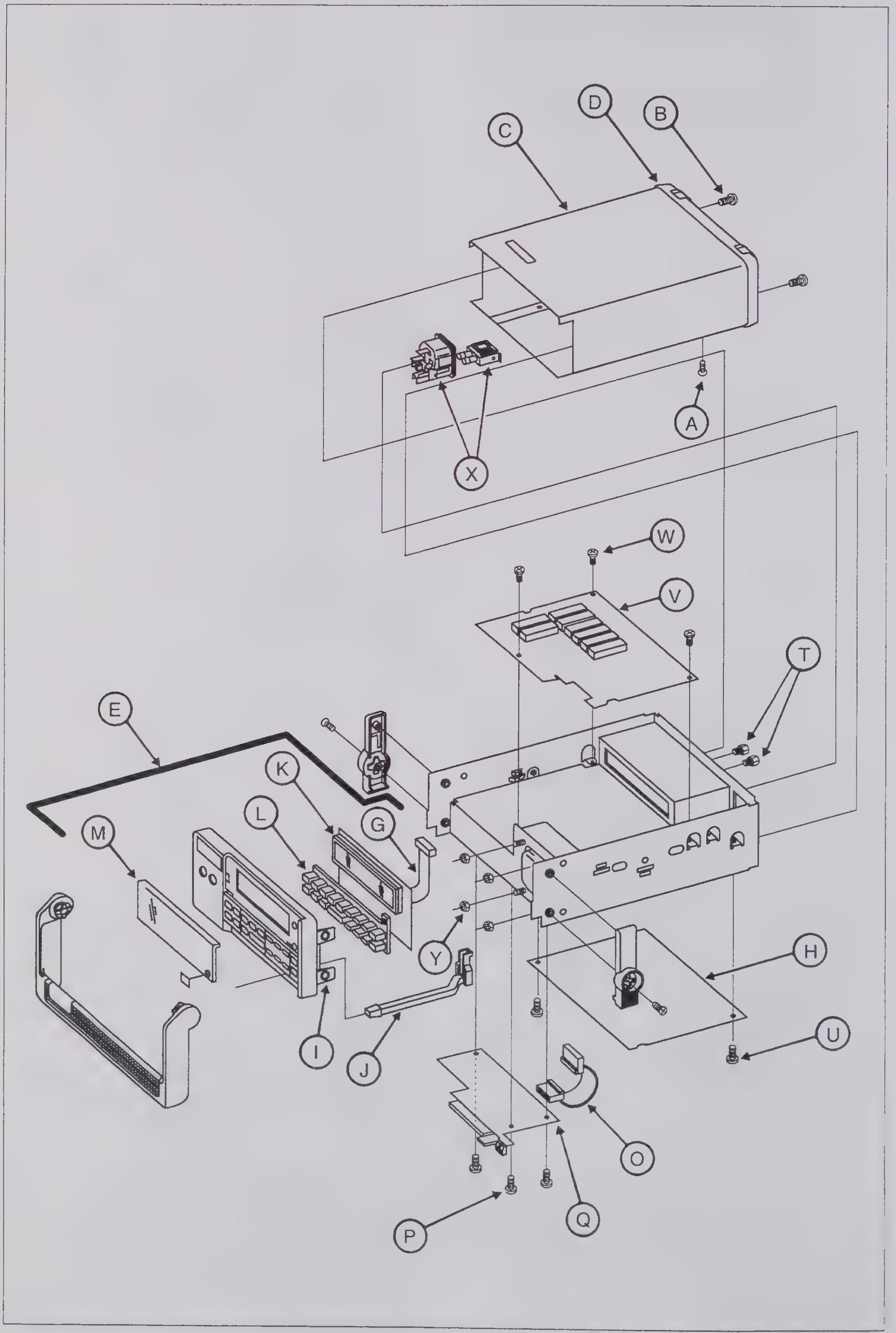
Figure 3-4. 2620A and 2625A Assembly Details


D
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T
E
K
L
G
M
Y
H
I
J
U
O
P
Q

Figure 3-5. 2635A Assembly Details

Remove the IEEE-488 Option (2620A Only) 3-15.

Section 7 of this manual provides a detailed removal procedure for the IEEE-488 option. The following removal instructions provide the essentials of this procedure. Parts referenced by letter (e.g., A) are shown in Figure 3-4. If necessary, refer to the complete procedure in Section 7.

1. From the bottom of the instrument, locate the IEEE-488 PCA (N). This pca is connected to the front of Main PCA, with a ribbon cable (O) leading across both pca's to the Rear Panel.
2. Use needle nose pliers to disconnect the 24-line cable assembly at the IEEE-488 PCA, alternately pulling on each end of the cable connector. Leave the other end of this cable attached to its Rear Panel connector.
3. Remove the 6-32, 1/4-inch panhead Phillips screw (P) securing the IEEE-488 PCA.
4. Disengage the IEEE-488 PCA by sliding it away from the Main PCA.

Remove the Memory PCA (2625A Only) 3-16.

Use the following procedure to remove the Memory PCA from the 2625A Data Logger. Parts referenced by letter (e.g., A) are shown in Figure 3-4.

1. From the bottom of the instrument, locate the Memory PCA (Q). This pca is connected to front of the Main PCA.

NOTE

You might want to verify that this is the Memory PCA. The Memory PCA and the IEEE-488 PCA occupy the same position and use the same connection to the Main PCA. The Memory PCA is a standard part of the Hydra Data Logger (Model 2625A). The IEEE-488 PCA is not available with the 2625A but is optional with the Hydra Data Acquisition Unit (Model 2620A).

2. Remove the panhead Phillips screw (P) securing the Memory PCA.
3. Disengage the Memory PCA by sliding it away from the Main PCA.

Remove the Memory Card I/F PCA (2635A Only) 3-17.

Use the following procedure to remove the Memory Card I/F PCA from the 2635A Data Bucket. Parts referenced by letter (e.g., A) are shown in Figure 3-5.

1. From the bottom of the instrument, locate the Memory Card I/F PCA (Q). This pca is in the front of the instrument near the center, and is connected to the Main PCA by a high-density ribbon cable (O).
2. Remove the three 6-32, 1/4-inch panhead Phillips screws (P) securing the Memory Card I/F PCA.
3. Disconnect the high-density ribbon cable (O) from the connector on the Memory Card I/F PCA (Q) and remove the assembly from the chassis.

Remove the Main PCA 3-18.

With the IEEE-488 option (2620A) and the Memory PCA (2625A) or Memory Card I/F PCA (2635A) removed, the Main PCA (H) can be removed. Parts referenced by letter (e.g., A) are shown in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A). Use the following procedure:

1. If it is still attached, remove the green power switch activator rod (J) extending from the power switch on the Main PCA through the Front Panel Assembly. Squeeze the end of the rod at the power switch and lift up; the bar disengages smoothly from the switch.
2. Using needle nose pliers, disconnect the display ribbon cable (G) on the Main PCA (H) by alternately pulling up on each end of its connector. Avoid breaking the alignment tabs on the Main PCA side of this connection. (This connector has already been detached if the Front Panel Assembly was removed.)
3. Detach the transformer connector at the Main PCA.
4. Detach the Main-to-A/D Converter cable at the A/D Converter PCA.
5. If installed, pull off the ALARM OUTPUTS and DIGITAL I/O terminal strips from the Rear Panel.
6. Remove the RS-232 connector screws (T) at the Rear Panel. Use a 3/16-inch nut driver to loosen the connector securing hardware.
7. If installed, remove the IEEE-488 connector. Use a 7-mm nutdriver to loosen the two securing screws on the rear panel.
8. Now remove the two screws (U) securing the Main PCA to the chassis. Slide the Main PCA forward. Then, while matching the pca edge indentations to the guide tabs on each chassis side, lift the Main PCA up and away from the chassis.

Remove the A/D Converter PCA 3-19.

Use the following procedure to remove the A/D Converter PCA (V). Parts referenced by letter (e.g., A) are shown in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A).

1. If necessary, remove the leads connecting the two front panel input terminals to the A/D Converter PCA. Using needle nose pliers, pull and disconnect the wires at the rear of the VΩ (red) and COM (black) input terminals. (These leads are already disconnected if the Front Panel Assembly has been removed.)
2. At the A/D Converter PCA, detach the cable leading to the Main PCA.
3. From the Rear Panel, pull out the Input Module.
4. Remove the three Phillips head screws (W) securing the A/D Converter PCA to the chassis.
5. Now slide the A/D Converter PCA forward to match the indentations in the pca edges to the guides in the chassis. Then lift the pca out.

Disconnect Miscellaneous Chassis Components 3-20.

Use the following procedure to disconnect the remaining hardware from the chassis. Parts referenced by letter (e.g., A) are shown in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A).

1. Use needle nose pliers to remove the internal connections at the line power plug (X). Remove the ground screw prior to disconnecting the ground wire from the plug.
2. Remove the power plug by releasing its two snaps one at a time.
3. Disconnect the power transformer by removing the four 5/16-inch nuts (Y) that secure it to the right side of the chassis.
4. If installed, remove the 7-mm IEEE-488 connector screws (Z) (2620A only).

ASSEMBLY PROCEDURES 3-21.

Generally, assembly procedures follow a reverse sequence of disassembly procedures. As some differences do apply, assembly is described separately in the following paragraphs. Begin assembly at the appropriate level, as defined by the heading. References are made to items in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A) for assembly details of standard instrument parts.

NOTE

Parts referenced by letter (e.g., A) are shown in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A).

Install Miscellaneous Chassis Components 3-22.

Use the following procedure to replace any items that have been removed from the basic chassis.

1. Replace the power transformer along the right side of the chassis. Use four 5/16-inch hex nuts (Y).
2. Snap the power plug into position.
3. Use needle nose pliers to replace the interior connections at the power plug. Also, attach the ground wire at its chassis connection.

Install the A/D Converter PCA 3-23.

1. Fit the A/D Converter PCA (L) so that the chassis guides pass through notches on both sides of the pca. Then slide the pca back until it is snug against the Input Module enclosure.
2. Fasten the A/D Converter PCA to the chassis with three 6-32, 1/4-inch panhead screws (W).
3. If the Front Panel Assembly is installed, attach the leads connecting the two input terminals to the A/D Converter PCA. Using needle nose pliers, push the wire connectors firmly onto the recessed input terminal pins (red to VΩ and black to COM.)
4. At the A/D Converter PCA, attach the cable leading to the Main PCA.
5. From the Rear Panel, push the Input Module back into place.

Install the Main PCA 3-24.

1. Fit the Main PCA (H) so that the chassis guides pass through notches on both sides of the pca. Then slide the pca back until it is snug against the Rear Panel.
2. Replace the RS-232 connector screws (T) on the rear of the chassis. Use a 3/16-inch nut driver to tighten the connector hardware.
3. Fasten the Main PCA to the chassis with two 6-32, 1/4-inch panhead screws (U).
4. Connect the transformer cable at connector J3 on the Main PCA. Verify that the connector is aligned correctly (all three pins connected.)
5. Plug the Front Panel cable onto its connector (J2) on the Main PCA.
6. From the Rear Panel, push the ALARM OUTPUTS and DIGITAL I/O terminal strips onto their appropriate connectors.

Install the IEEE-488 Option (2620A only) 3-25.

Both the instruction sheet provided with the IEEE-488 Option and Section 7 of this manual fully describe installation. The following instructions provide installation procedure essentials. If necessary, refer to Section 7, paying particular attention to Figures 7-2 and 7-3.

1. Place the IEEE-488 PCA (N) into position so that the edge of the pca fits into the chassis guide. Then line up connecting pins with the matching connector on the Main PCA, and slide the pca into position.
2. Install the single 6-32, 1/4-inch panhead Phillips screw in the corner of the IEEE-488 PCA.
3. If necessary, attach the rear panel connector using a 7-mm nut driver.
4. At the pca, attach the ribbon cable leading from the rear panel connector.

Install the Memory PCA (2625A only) 3-26.

NOTE

The Memory PCA and the IEEE-488 PCA occupy the same position and use the same connection to the Main PCA. The Memory PCA is a standard part of the Hydra Data Logger (Model 2625A). The IEEE-488 PCA is not available with the 2625A but is optional with the Hydra Data Acquisition Unit (Model 2620A).

1. Place the Memory PCA into position so that the edge of the pca fits in the chassis guide. Then line up connecting pins with the matching connector on the Main PCA, and slide the pca into position.
2. Install the single 6-32, 1/4-inch panhead Phillips screw in the corner of the Memory PCA.

Install the Memory Card I/F PCA (2635A only) 3-27.

1. Place the Memory Card I/F PCA (Q) into position so that the three mounting holes line up with the chassis supports located at the front-center of the chassis.
2. Install the three 6-32, 1/4-inch panhead Phillips screws in the mounting holes of the Memory Card I/F PCA.
3. Reconnect the high-density ribbon cable (O) to the connector on the Memory Card Interface PCA (Q).

Assemble the Front Panel Assembly 3-28.

As appropriate, use the following steps to assemble the Front Panel Assembly.

1. Clean the lens (M) with deionized air and, if necessary, isopropyl alcohol. Then gently snap the lens into the front panel tabs.
2. Fit the elastomeric keypad assembly (L) through the Front Panel Assembly.
3. Slide the Display PCA into the bottom securing tabs on the back of the Front Panel Assembly. Then gently snap the pca into place.

NOTE

The Display PCA provides a space for a center screw. If the peripheral tabs are intact, this screw is not necessary. If some of the tabs are broken, the screw can be used as an additional securing device.

4. Connect the 20-pin cable (G) to the Display PCA.

Install the Front Panel Assembly 3-29.

Use the following procedure when installing the Front Panel Assembly:

1. Position the Front Panel Assembly into place and snap the four tab retainers (I) onto the chassis.
2. Observing the alignment orientation provided by tabs on the connector, attach the display ribbon cable connector (G) on the Main PCA.
3. Using needle nose pliers, connect the wires at the rear of the recessed input terminals (Red to VΩ, Black to COM).

Install the Handle and Mounting Brackets 3-30.

Refer to Figure 3-3 during the following procedure. Use a Phillips head screwdriver to attach the two handle mounting brackets. Note that these brackets must be reinstalled in their original positions. Therefore, the inside of each bracket is labeled with an R or an L, in reference to the front view of the instrument.

Now, engage the handle. Point the handle straight up. Then pull out on each end of the handle to engage the respective pivot in its bracket. Pull out slightly on both pivots to rotate the handle to the desired position.

Install the Instrument Case 3-31.

Reinstall the instrument case, checking that it seats properly in the front panel. Attach the rear bezel with the two panhead Phillips screws and secure the case with the flathead Phillips screw in the bottom. Refer to Figure 3-2.

Section 4

Performance Testing and Calibration

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INTRODUCTION 4-1.

This section of the Service Manual provides performance tests that can be used at any time to verify that Hydra (2620A, 2625A, or 2635A) operation is within published specifications. A complete calibration procedure is also included. The performance test and, if necessary, the calibration procedure can be performed periodically as well as after service or repair.

REQUIRED EQUIPMENT 4-2.

Equipment required for Performance Testing and Calibration is listed in Table 4-1.

Table 4-1. Recommended Test Equipment

INSTRUMENT TYPE	MINIMUM SPECIFICATIONS			RECOMMENDED MODEL
Multifunction Calibrator	DC Voltage: Range: 90 mV to 300V dc. Accuracy: 0.005%			Fluke 5700A
	AC Voltage:			
	FREQUENCY	VOLTAGE	ACCURACY	
	1 kHz	29 mV to 300V	0.05%	
	100 kHz	15 mV to 300V	1.25%	
	Frequency:			
	10 kHz	1V rms	.0125%	
Decade Resistance Source		Accuracy		Fluke 5450A/AB or Fluke 5700A
	290Ω or 190Ω	0.003%		
	2.9 kΩ 1.9 kΩ	0.003%		
	29 kΩ 19 kΩ	0.003%		
	290 kΩ 190 kΩ	0.003%		
	2.9 MΩ 1.9 MΩ	0.0005%		
Mercury Thermometer	0.02 degrees Celsius resolution			Princo ASTM-56C
Thermocouple Probe	Type K			Fluke P-20K
Room Temperature Oil/Water Bath	Thermos bottle and cap			
Multimeter	Measures +5V dc.			Fluke 77.
Signal Generator	Sinewave, 0.5 to 1V rms 10 Hz to 5 kHz			Fluke 6011A

ALTERNATE EQUIPMENT LIST
(Minimum specifications are the same as in the Standard Equipment List, except where noted.)

INSTRUMENT TYPE	RECOMMENDED MODEL
DC Voltage Calibrator	Fluke 5440B
DMM Calibrator	Fluke 5100B (for AC Volts only)
Function/Signal Generator	Philips PM5193 or Fluke 6011A
Decade Resistance Source	Gen Rad 1433H or General Resistance RDS 66A (Accuracy 0.0125%)

PERFORMANCE TESTS 4-3.

When received, the instrument is calibrated and in operating condition. The following performance verification procedures are provided for acceptance testing upon initial receipt or to verify correct operation at any time. All tests may be performed in sequence to verify overall operation, or the tests may be run independently.

If the instrument fails any of these performance tests, calibration adjustment and/or repair is needed. To perform these tests, use a Fluke 5700A Multifunction Calibrator or equipment that meets the minimum specifications given in Table 4-1.

Each of the measurements listed in the following steps assumes the instrument is being tested after a 1/2 hour warmup, in an environment with an ambient temperature of 18 to 28 degrees Celsius and with a relative humidity of less than 70%.

NOTE

All measurements listed in the performance test tables are made in the slow reading rate unless otherwise noted.

WARNING

HYDRA CONTAINS HIGH VOLTAGES THAT CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE INSTRUMENT.

Accuracy Verification Test 4-4.

1. Power up the instrument and wait 1/2 hour for its temperature to stabilize.
2. Connect a cable from the Output VA HI and LO connectors of the 5700A to the VΩ and COM connectors on the Hydra front panel. Select the channel 0 function and range on Hydra and the input level from the 5700A using the values listed in Table 4-2. Press MON to measure and display the measurement value for channel 0. The display should read between the minimum and maximum values (inclusive) listed in the table.

Channel Integrity Test 4-5.

Verify that the Accuracy Verification Test for channel 0 meets minimum acceptable levels before performing this test.

1. Switch OFF power to the instrument and disconnect all high voltage inputs.
2. Remove the Input Module from the rear of the instrument. Open the Input Module and connect a pair of test leads to the H (high) and L (low) terminals of channel 1. Reinstall the Input Module into the instrument.
3. Connect the ends of the test leads together to apply a short (0 ohms).
4. Reconnect power, and turn the instrument ON.
5. For channel 1, select the 2-terminal ohms function and 300-ohms range on Hydra. Press MON and ensure that the display reads a resistance of less than or equal to 1.5Ω. (This test assumes that lead wire resistances are less than 0.1Ω.)
6. Open the ends of the test leads and ensure that the display reads “OL” (overload).
7. Press MON to stop the measurement.
8. Connect a cable from the Output VA HI and LO of the 5700A to the Input Module test leads (observe proper polarity).

Table 4-2. Performance Tests (Voltage, Resistance, and Frequency)

FUNCTION	RANGE	INPUT LEVEL	FREQUENCY	DISPLAY ACCURACY (1 Year, 18-28°C)	
				MIN	MAX
DC Volts	90 mV *	short (0)	—	-0.007	0.007
	90 mV *	90 mV	—	89.962	90.038
	300 mV	short (0V)	—	-0.02	0.02
	300 mV	150 mV	—	149.93	150.07
	300 mV	290 mV	—	289.89	290.11
	900 mV* **	900 mV	—	899.70	900.30
	3V	2.9V	—	2.8988	2.9012
	3V	-2.9V	—	-2.9012	-2.8988
	30V	29V	—	28.990	29.010
	150V	150V	—	149.94	150.06
	300V	290V	—	289.90	290.10
* Range only used on 2635A (not used in autoranging). ** Computer I/F only (see FUNC command).					
NOTE *Voltages greater than 150V can only be applied to channels 0, 1, and 11.*					
AC Volts	300 mV	20 mV	1 kHz	19.71	20.28
	300 mV	20 mV	100 kHz	18.50	21.50
	300 mV	290 mV	1 kHz	289.26	290.74
	300 mV	290 mV	100 kHz	275.00	305.00
	3V	2.9V	1 kHz	2.8934	2.9066
	30V	29V	1 kHz	28.931	29.069
	150V	150V	1 kHz	149.54	150.46
	300V	290V	1 kHz	289.34	290.66
NOTE *Voltages greater than 150V can only be applied to channels 0, 1, and 11. The rear Input Module must be installed when measuring ac volts on channel 0.*					
Resistance (4-Terminal)					
NOTE *For 2-terminal measurements, the resistance accuracy given in this table applies to channel 0 only and makes allowance for up to 0.05Ω of lead wire resistance. You must add any additional lead wire resistance present in your set up to the resistance values given in this table.*					
Using inputs in decades of 3:					
	300Ω	short		0.00	0.09
	-	300Ω		299.80	300.27
	3 kΩ	short		0.0000	0.0003
	-	3 kΩ		2.9981	3.0020
	30 kΩ	30 kΩ		29.980	30.020
	300 kΩ	300 kΩ		299.81	300.19
	3 MΩ	3 MΩ		2.9979	3.0021
Using inputs in decades of 1.9:					
	300Ω	short		0.00	0.09
	-	190Ω		189.87	190.20
	3 kΩ	short		0.0000	0.0003
	-	1.9 kΩ		1.8987	1.9014
	30 kΩ	19 kΩ		18.987	19.013
	300 kΩ	190 kΩ		189.87	190.13
	3 MΩ	1.9 MΩ		1.8986	1.9014

Table 4-2. Performance Tests (Voltage, Resistance, and Frequency) (cont)

FUNCTION	RANGE	INPUT LEVEL	FREQUENCY	DISPLAY ACCURACY (1 Year, 18-28°C)	
				MIN	MAX
Using inputs in decades of 1:					
	300Ω	short		0.00	0.09
	-	100Ω		99.92	100.15
	3 kΩ	short		0.0000	0.0003
	3 kΩ	1 kΩ		0.9992	1.0009
	30 kΩ	10 kΩ		9.992	10.008
	300 kΩ	100 kΩ		99.92	100.08
	3 MΩ	1 MΩ		0.9992	1.0008
	10 MΩ*	10 MΩ		9.986	10.014
	* Optional test point if standards available.				
NOTE *All channels (0 through 20) can accommodate 2-terminal resistance measurements. Channel 0, with only two connections, cannot be used for 4-terminal measurements. Four-terminal resistance measurements can be defined for channels 1 through 10 only. Channels 11 through 20 are used, as required, for 4-terminal to provide the additional two connections. For example, a 4-terminal set up on channel 1 uses channels 1 and 11, each channel providing two connections.*					
Frequency	90 kHz	10 kHz/2V p-p		9.994	10.006

9. Select the VDC function and 300-volt range on Hydra and apply 0V dc from the 5700A. Then apply 290V dc input from the 5700A. Ensure the display reads between the minimum and maximum values as shown in Table 4-2 for the 0 and 290V dc input levels.

NOTE

Channels 0, 1, and 11 can accommodate a maximum input of 300V dc or ac. However, the maximum input for all other channels can only be 150V dc or ac.

10. With the exception of the selected voltage range and input voltage from the 5700A, repeat steps 1 through 9 for each remaining Input Module channel (2 through 20). Channels 2 through 10 and 12 through 20 should be configured for the 150V dc range and an input voltage of 150 volts.

Thermocouple Measurement Range Accuracy Test 4-6.

Verify that the Accuracy Verification Test for channel 0 meets minimum acceptable levels before performing this test.

Thermocouple temperature measurements are accomplished using the Hydra internal 100 mV and 1V dc ranges. (The ranges are not configurable by the operator.) This procedure provides the means to test these ranges.

Testing the 100 mV and 1V dc ranges requires computer interfacing with a host (terminal or computer). The host must send commands to select these ranges. These ranges cannot be selected from the Hydra front panel.

1. Ensure that communication parameters (i.e., transmission mode, baud rate, parity, and echo mode) on Hydra and the host are properly configured to send and receive serial data. Refer to Section 4 of the Hydra Users Manual.
2. Power up Hydra, and wait 1/2 hour for its temperature to stabilize.
3. Connect a cable from the Output VA HI and LO connectors of the 5700A to the VΩ and COM connectors on the Hydra front panel.
4. Set the 5700A to output 0V dc.
5. Using either a terminal or a computer running a terminal emulation program as the selected host, send the following commands to Hydra:

   ```
   FUNC 0,VDC,I100MV < CR>

   MON 1,0 < CR>

   MON_VAL? < CR>
   ```

   The returned value for channel 0 should be 0 mV ±0.007 mV.

   Set the 5700A to output 90 mV DC. Send the following command:

   ```
   MON_VAL? < CR>
   ```

   The value returned should now be 90 mV ±0.038 mV (between 89.962 and 90.038 mV).
6. Change the Hydra channel 0 function to the internal 1V dc range by redefining channel 0. Send the following commands:

   ```
   MON 0 < CR>

   FUNC 0,VDC,I1V < CR>
   ```

   Set the 5700A to output 0.9V dc. Send the following commands:

   ```
   MON 1,0 < CR>

   MON_VAL? < CR>
   ```

   The value returned should be 900 mV ±0.22 mV (899.78 to 900.22 mV.)

4-Terminal Resistance Test 4-7.

Verify that the channel 0 accuracy verification tests for dc volts and ohms meet minimum acceptable levels.

1. Switch OFF power to the instrument and disconnect all high voltage inputs.
2. Remove the Input Module from the rear of the instrument. Open the Input Module and connect a pair of test leads (keep as short as possible) to the H (high) and L (low) terminals of channel 1 and a second pair of test leads to the H and L terminals of channel 11. Reinstall the Input Module into the instrument.

3. Observing polarity, connect the channel 1 test leads to the Sense HI and LO terminals of the 5700A and the channel 11 test leads to the Output HI and LO terminals of the 5700A. Route wires with the method shown in Figure 4-1. Connect the wires to the terminals shown in Figure 4-2.

NOTE

4-terminal connections are made using pairs of channels. 4-terminal measurements can be made only on channels 1 through 10. The accompanying pairs are channels 11 through 20.

4. Switch the instrument ON.
5. Select the 4-terminal OHMS function, AUTO range, for channel 1 on Hydra.
6. Set the 5700A to output the resistance values listed in Table 4-2 (Use decades of 1.9).
7. On Hydra press MON and ensure the display reads between the minimum and maximum values (inclusive) shown in Table 4-2.
8. The 4-terminal Resistance Test is complete. However, if you desire to perform this test on other Input Module channels (2 through 10), repeat steps 1 through 7, substituting in the appropriate channel number.

Thermocouple Temperature Accuracy Test 4-8.

Verify that the Thermocouple Measurement Range Accuracy Test meets minimum acceptable levels before performing this test.

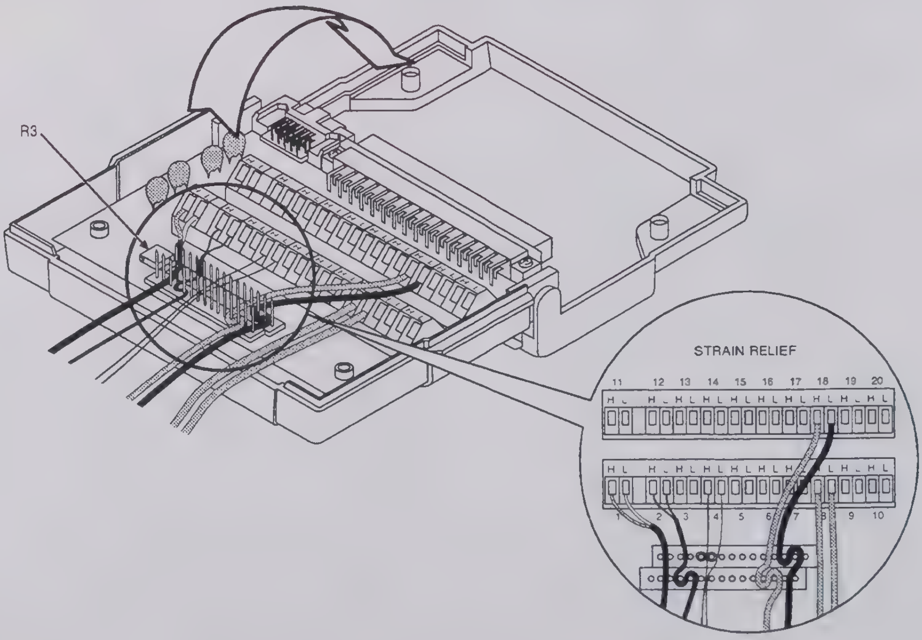
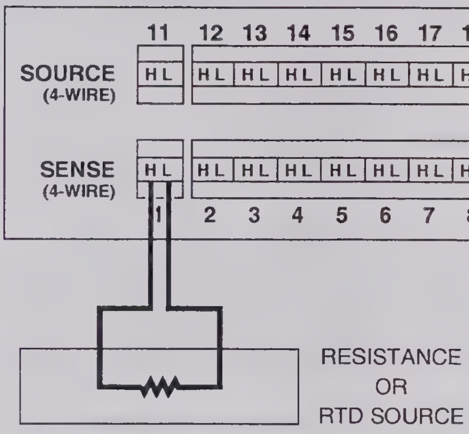

R3
STRAIN RELIEF
11 12 13 14 15 16 17 18 19 20
H L H L H L H L H L H L H L H L H L H L
H L H L H L H L H L H L H L H L H L H L
1 2 3 4 5 6 7 8 9 10

Figure 4-1. Input Module

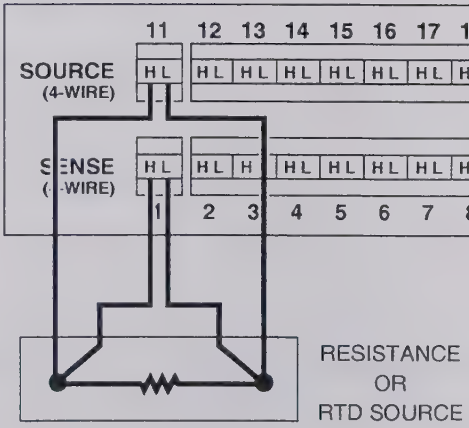
2-WIRE (2T) CONNECTION


11 12 13 14 15 16 17 18 19 20
SOURCE
(4-WIRE)
H L
SENSE
(4-WIRE)
H L
1 2 3 4 5 6 7 8 9 10
RESISTANCE
OR
RTD SOURCE

USE H AND L TERMINALS FOR ANY CHANNEL.

- CHANNEL 0 ON FRONT PANEL
- CHANNELS 1 THROUGH 20 ON REAR PANEL INPUT MODULE (CHANNEL 1 SHOWN HERE).

4-WIRE (4T) CONNECTION


11 12 13 14 15 16 17 18 19 20
SOURCE
(4-WIRE)
H L
SENSE
(4-WIRE)
H L
1 2 3 4 5 6 7 8 9 10
RESISTANCE
OR
RTD SOURCE

USE H AND L TERMINALS FOR TWO CHANNELS ON REAR PANEL INPUT MODULE. CONNECTIONS FOR CHANNEL 1 SHOWN HERE WITH CHANNEL 11 PROVIDING ADDITIONAL TWO CONNECTIONS.

FOR EACH 4-WIRE CONNECTION, ONE SENSE CHANNEL (1 THROUGH 10) AND ONE SOURCE CHANNEL (SENSE CHANNEL NUMBER +10 = 11 THROUGH 20) ARE USED.

Figure 4-2. 2T and 4T Connections

1. Switch OFF power to the instrument and disconnect all high voltage inputs.
2. Remove the Input Module from the rear of the instrument. Open the Input Module, and connect a K-type thermocouple to the H (high) and L (low) terminals of channel 1. (See Table 4-3 for lead colors). Then reinstall the Input Module into the instrument.

NOTE

If other than a K type thermocouple is used, be sure that the instrument is set up for the type of thermocouple used.

3. Reconnect power and switch the instrument ON.
4. Insert the thermocouple and a mercury thermometer (.02 degrees Celsius resolution) in a room temperature bath. Allow 20 minutes for thermal stabilization.
5. Select the temperature function and K thermocouple type for channel 1. Then press MON.
6. The value displayed should be the temperature of the room temperature bath (within tolerances given in Table 4-4) as measured by the mercury thermometer.
7. The Thermocouple Temperature Accuracy Test is complete. However if you desire to perform this test on any other Input Module channel (2 through 20) repeat steps 1 through 6 substituting in the appropriate channel number.

Open Thermocouple Response Test

4-9.

Use the following procedure to test the open thermocouple response:

Table 4-3. Thermocouple Information

TYPE	POSITIVE LEAD MATERIAL	POSITIVE LEAD COLOR		NEGATIVE LEAD MATERIAL	USABLE RANGE (°C)
		ANSI*	IEC**		
J	Iron	White	Black	Constantan	-200 to 760
C†	Tungsten (5% Rhenium)	White	-	Tungsten (26% Rhenium)	0 to 2316
b	Platinum (30% Rhodium)	Gray	-	Platinum (6% Rhodium)	0 to 1820
S	Platinum	Black	Orange	Platinum (10% Rhodium)	-50 to 1768
R	Platinum	Black	Orange	Platinum (13% Rhodium)	-50 to 1768
N	NICROSIL	Orange	-	NISIL	-270 to 1300
T‡	Copper	Blue	Brown	Constantan	-270 to 400
E	Chromel	Purple	Violet	Constantan	-270 to 1000
K	Chromel	Yellow	Green	Alumel	-270 to 1372

* American National Standards Institute (ANSI) device negative lead is always Red.

** International Electrotechnical Commission (IEC) device negative lead is always White.

† Not an ANSI designation but a Hoskins Engineering Company designation.

‡ An ANSI type T is supplied with the meter.

Table 4-4. Performance Tests for Thermocouple Temperature Function

Thermocouple Type	Thermocouple Accuracy Specifications 1 Year @ 18-28 Degrees C
J	± 0.4 °C
K	± 0.5 °C
N	± 0.6 °C
E	± 0.4 °C
T	± 0.5 °C

1. Switch OFF power to the instrument and disconnect all high voltage inputs.

2. Remove the Input Module from the rear of the instrument. Open the Input Module and connect test leads to the H (high) and L (low) terminals of channel 1. Reinstall the Input Module into the instrument.

3. Reconnect power and switch the instrument ON.

4. Connect the test leads from the Input Module to an 820 ohm resistor.

5. Select the temperature function and K thermocouple type for channel 1. Then press MON.

6. The value displayed should approximate the ambient temperature.

7. Replace the 820-ohm resistor with a 4-kilohm resistor to simulate a high resistance or open thermocouple.

8. Verify a reading of “otc”.

9. The Open Thermocouple Response Test is complete. However if you desire to perform this test on any other Input Module channel (2 through 20) repeat steps 1 through 8, substituting the appropriate channel number.

RTD Temperature Accuracy Test 4-10.

The following two RTD Temperature Accuracy Tests are different in that one uses a Decade Resistance Source and the other uses an RTD. Only one of the tests needs to be performed to verify operation.

RTD TEMPERATURE ACCURACY TEST (USING DECADE RESISTANCE SOURCE) 4-11.

Verify that the channel 0 accuracy verification tests for dc volts and 300-ohm range meet minimum acceptable levels.

1. Switch OFF power to the instrument and disconnect all high voltage inputs.

2. Remove the Input Module from the rear of the instrument. Open the Input Module and connect a pair of test leads (keep as short as possible) to the H (high) and L (low) terminals of channel 1. For 4-terminal performance testing, connect a second pair of test leads to the H (high) and L (low) terminals of channel 11. Reinstall the Input Module into the instrument.

3. Connect the channel 1 test leads to the Output HI and LO terminals on the Decade Resistance Source. For 4-terminal performance testing, also connect channel 11's test leads to the Output HI and LO terminals of the Decade Resistance Source. Connect as shown in Figures 4-1 and 4-2.

NOTE

4-terminal connections are made using pairs of channels. 4-terminal measurements can only be made on channels 1 through 10. The accompanying pairs are channels 11 through 20.

4. Switch the instrument ON.
5. Select the 4-terminal RTD temperature function, RTD type PT, for channel 1 on Hydra.
6. Press MON. For each resistance, ensure that the display reads within the range shown in Table 4-5.
7. The RTD Temperature Accuracy test is complete. However, if you desire to perform this test on Input Module channels (2 through 10), repeat steps 1 through 5 substituting in the appropriate channel number.

NOTE

The only type of temperature measurement that can be made on channel 0 is 2-terminal RTD. Channels 11 through 20 support only 2-terminal RTDs.

RTD TEMPERATURE ACCURACY TEST (USING DIN/IEC 751) 4-12.

1. Switch OFF power to the instrument and disconnect all other high voltage inputs.
2. Remove the Input Module from the rear of the instrument. Open the Input Module and connect a Platinum RTD, conforming to the European Standards IEC 751 (DIN 43760).

   2-terminal RTD: Connect the RTD excitation leads to the H (high) and L (low) terminals of channel 1.

Table 4-5. Performance Tests for RTD Temperature Function (Resistance Source)

Decade Resistance Source	Simulated Degree C Temperature		Temperature Accuracy Specifications 1 Year @ 18-28 °C
	before M5.6*	after M5.5*	
100Ω	0	0	± 0.24 °C
200Ω	266.58	266.34	± 0.48 °C
300Ω	558.00	557.70	± 0.75 °C

* RTD temperature linearization changed between versions 5.5 and 5.6 of the Hydra instrument firmware. From the Hydra front panel, simultaneously press [ltb] and [rtb]. The main software version number (e.g., "5.5") appears in the left display.

These figures assume that RTD R0 is set to 100.00Ω for each channel.

Accuracy given is for 4-wire measurements only. For 2-wire measurements, degrade the accuracy specifications by 5.2 °C per ohm of single lead wire resistance. For 2-wire measurements, degrade the accuracy by an additional 4 °C (channels 1 .. 20) or 0.05 °C (channel 0).

4-terminal RTD: Connect the RTD excitation leads (one red and one black wire) to the H (high) and L (low) terminals of channel 11. Connect the second pair of RTD red and black leads to the H and L leads of channel 1. (Refer to Figures 4-1 and 4-2 for proper connection.) Reinstall the Input Module into the instrument.

NOTE

4-terminal connections are made using pairs of channels. 4-terminal measurements can only be made on channels 1 through 10. Their accompanying pairs are channels 11 through 20.

3. Switch the instrument ON.
4. Insert the RTD probe and a mercury thermometer in a room temperature bath. Allow 20 minutes for thermal stabilization.
5. Depending on the type of connection made in step 2, select either the 2-Terminal or 4-Terminal RTD temperature function, RTD type PT (DIN IEC 751), for channel 1 on Hydra. Press MON and ensure the display reads the temperature of the room temperature bath (within tolerances shown in Table 4-6) as measured by the mercury thermometer.
6. The RTD Temperature Accuracy test is complete. However, if you desire to perform this test on any other channel (0 or 2 through 20), repeat steps 1 through 5, substituting the appropriate channel number.

NOTE

The only type of temperature measurement that can be made on channel 0 is 2-terminal RTD. Channels 11 through 20 support only 2-terminal RTDs.

Digital Input/Output Verification Tests 4-13.

Digital Input/Output verification testing requires computer interfacing with a host (terminal or computer). The host must send commands to the instrument to control the digital lines for this test. Refer to Section 4 of the Hydra Users Manual for a description of configuring and operating the instrument.

Table 4-6. Performance Tests for RTD Temperature Function (DIN/IEC 751)

RTD Type (DIN 43760 RTD)	Temperature Accuracy Specifications 1 Year @ 18-28 Degrees C
2-wire (channel 0)	-0.65 °C to +0.70 °C
2-wire (channels 1-20)	-0.65 °C to +4.65 °C
4-wire	±0.65 °C
(Assumes RTD R0 is set to 100.00Ω for each channel.)	

DIGITAL OUTPUT TEST 4-14.

1. Ensure that communication parameters (i.e., transmission mode, baud rate, parity, and echo mode) on Hydra and the host are properly configured to send and receive serial data.

2. Switch OFF power to the instrument and disconnect all high voltage inputs.

3. Remove the ten-terminal Digital I/O connector from the rear of the instrument and all external connections to it. Connect short wires (to be used as test leads) to the ground (⏚) and 0 through 7 terminals. Leave the other wire ends unconnected at this time. Reinstall the connector.

4. Switch power ON to both Hydra and the host. Verify that Hydra is not scanning. If Hydra is scanning, press SCAN to turn scanning off, then cycle power off and on again.

5. Using a digital multimeter (DMM), verify that all digital outputs (0-7) are in the OFF or HIGH state. This is done by connecting the low or common of the multimeter to the ground test lead and the high of the multimeter to the digital output and verifying a voltage greater than +3.8V dc.

6. Using either a terminal or a computer running a terminal emulation program, set up Hydra to turn Digital Outputs ON (LOW state).

   In sequence send the following commands to Hydra and measure that the correct Digital Output line measures less than +0.8V dc (LOW state.)

   ```
   DO_LEVEL 0,0 < CR>
   ```

   Verify that output 0 measures a LOW state.

   ```
   DO_LEVEL 1,0 < CR>
   ```

   Verify that output 1 measures a LOW state.

   ```
   DO_LEVEL 2,0 < CR>
   ```

   Verify output 2 measures a LOW state.

   Repeat the command for all eight outputs.

7. Set up Hydra to turn Digital Outputs OFF (HIGH state).

   Send the following commands to Hydra in sequence, and measure that the correct Digital Output line measures greater than +3.8V dc (HIGH state.)

   ```
   DO_LEVEL 0,1 < CR>
   ```

   Verify that output 0 measures a HIGH state.

   ```
   DO_LEVEL 1,1 < CR>
   ```

   Verify that output 1 measures a HIGH state.

   Repeat the command for all eight outputs.

DIGITAL INPUT TEST 4-15.

1. Perform the DIGITAL OUTPUT TEST steps 1 through 5.
2. Using either a terminal or a computer running a terminal emulation program, read the Hydra Digital Input lines.

   Send the following command to Hydra:

   DIO_LEVELS? < CR>

   Verify that the returned value is 255.

   NOTE

   The number returned is the decimal equivalent of the Digital Input binary word (status of inputs 0 through 7). See Table 4-7 to determine if the number returned corresponds to the inputs jumpered to ground in this test.

3. Jumper input 0 to ground by connecting the ground test lead to the input 0 test lead.

   Then send the following command to Hydra:

   DIO_LEVELS? < CR>

   Verify that the returned value is 254.
4. Disconnect input 0 from ground, then jumper input 1 to ground.

   Send the command: DIO_LEVELS? < CR>

   Verify that the returned value is 253.
5. Repeat step 4 for each input and verify the correct returned value (See Table 4-7).

TOTALIZER TEST 4-16.

This totalizer verification test requires toggling Digital Output line 0 and using it as the Totalizer input. The test requires computer interfacing with a host (terminal or computer). The host must send commands to Hydra to control the digital line for this test.

Table 4-7. Digital Input Values

TERMINAL GROUNDED	STATE OF DIGITAL INPUTS	DECIMAL VALUE
none	inputs 0-7, all HIGH	255
0	inputs 1-7 HIGH, input 0 LOW	254
1	inputs 0,2-7 HIGH, input 1 LOW	253
2	inputs 0-1 and 3-7 HIGH, input 2 LOW	251
3	inputs 0-2 and 4-7 HIGH, input 3 LOW	247
4	inputs 0-3 and 5-7 HIGH, input 4 LOW	239
5	inputs 0-4 and 6-7 HIGH, input 5 LOW	223
6	inputs 0-5 and 7 HIGH, input 6 LOW	191
7	inputs 0-6 HIGH, input 7 LOW	127

1. Ensure that communication parameters (i.e., transmission mode, baud rate, parity, and echo mode) on Hydra and the host are properly configured to send and receive serial data. Refer to Section 4 of the Hydra Users Manual.
2. Switch OFF power to the instrument and disconnect all high voltage inputs.
3. Remove the ten-terminal Digital I/O connector from the rear of the instrument and all external connections to it. Connect short wires (to be used as test leads) to the 0 terminal and the Totalizer (Σ) terminal. Leave other ends of wires unconnected at this time. Reinstall the connector.
4. Switch ON power to both Hydra and the host.
5. Press the TOTAL button on the front panel of Hydra.

   Verify that Hydra displays a 0 value.
6. Jumper output 0 to the Totalizer (Σ) input by connecting the (Σ) terminal test lead to the output 0 test lead.
7. Using either a terminal or a computer running a terminal emulation program, set up Hydra to toggle (turn ON and OFF) Digital Output 0.

   Send the following commands to Hydra in sequence, and verify that Hydra measures and displays the correct total value:

   ```
   DO_LEVEL 0,0 < CR>

   DO_LEVEL 0,1 < CR>
   ```

   Verify that Hydra displays a totalizer count of 1.
8. Send the following commands in sequence:

   ```
   DO_LEVEL 0,0 < CR>

   DO_LEVEL 0,1 < CR>
   ```

   A totalizer count of 2 should now be displayed.
9. Repeat step 8 for each incremental totalizing count.
10. Set the Hydra totalized count to a value near full range (65535) and test for overload.

    Send the following commands to Hydra:

    ```
    TOTAL 65534 < CR>

    DO_LEVEL 0,0 < CR>

    DO_LEVEL 0,1 < CR>
    ```

    A totalizer count of 65535 should be displayed.
11. Send:

    ```
    DO_LEVEL 0,0 < CR>

    DO_LEVEL 0,1 < CR>
    ```

    The Hydra display should now read “OL”, indicating that the counter has been overrun.

TOTALIZER SENSITIVITY TEST 4-17.

1. Perform a successful Totalizer Test.
2. Remove the jumper connecting the Σ terminal test lead to the output 0 test lead.
3. Verify that Hydra is still in the total measuring mode. If not, press the TOTAL button. Reset the totalizer count shown on the display by pressing the SHIFT and TOTAL(ZERO) buttons.

   The Hydra display should now show a value of 0.
4. Connect the output of the signal generator to the Σ and ⏚ terminals.
5. Program the signal generator to output a 1.5V rms sine signal at 10 Hz.

   The Hydra display should now show the totalizing value incrementing at a 10 count per second rate.

Dedicated Alarm Output Test 4-18.

The Dedicated Alarm Output Test verifies that Alarm Outputs 0 through 3 are functioning properly. Because this test is dependent on voltage readings the Accuracy Verification Test for channel 0 and the Channel Integrity Test for channels 1 through 3 should be performed if voltage readings are suspect.

1. Switch OFF power to the instrument and disconnect all high voltage inputs.
2. Remove the eight-terminal Alarm Output connector from the rear of Hydra and all external connections to it. Connect short wires (to be used as test leads) to the ⏚ and 0 through 3 terminals. Leave the other ends of the wires unconnected at this time. Reinstall the connector.
3. Remove the Input Module from the rear of Hydra. Open the Input Module and jumper the H (high) terminal of channels 1, 2, and 3 together. Connect a test lead to the H of channel 1. Also jumper the L (low) terminals of channel 1, 2, and 3 together. Connect a second test lead to the L of channel 1. Reinstall the Input Module into Hydra. Refer to Figure 4-3.
4. Switch power ON.
5. Using a digital multimeter (DMM), verify that alarm outputs 0 through 3 are in the OFF or HIGH state. Perform this test by connecting the low or common of the multimeter to the ground test lead and the high of the multimeter to the alarm output. Verify a voltage greater than +3.8V dc.
6. Connect a cable from the Output VA HI and LO connectors of the 5700A to the VΩ and COM connectors on the front panel of Hydra. Then jumper the Hydra VΩ terminal to the H (high) test lead of the Input Module and the COM terminal to the L (low) test lead.
7. On Hydra, select the VDC function, 3V range, and assign a HI alarm limit of +1.0000 for channels 0 through 3. Set up all other channels (4-20) to the OFF function. Select a scan interval of 5 seconds.
8. Set the 5700A to output +0.9900 volts.
9. Press SCAN. Hydra should scan channels 0 through 3 every 5 seconds.
10. Using a digital multimeter, again verify that alarm outputs 0 through 3 are in the OFF or HIGH state.
11. Set the 5700A to output +1.1000 volts. Verify that the alarm outputs 0 through 3 are in the ON or LOW state (measure less than +0.8V dc).

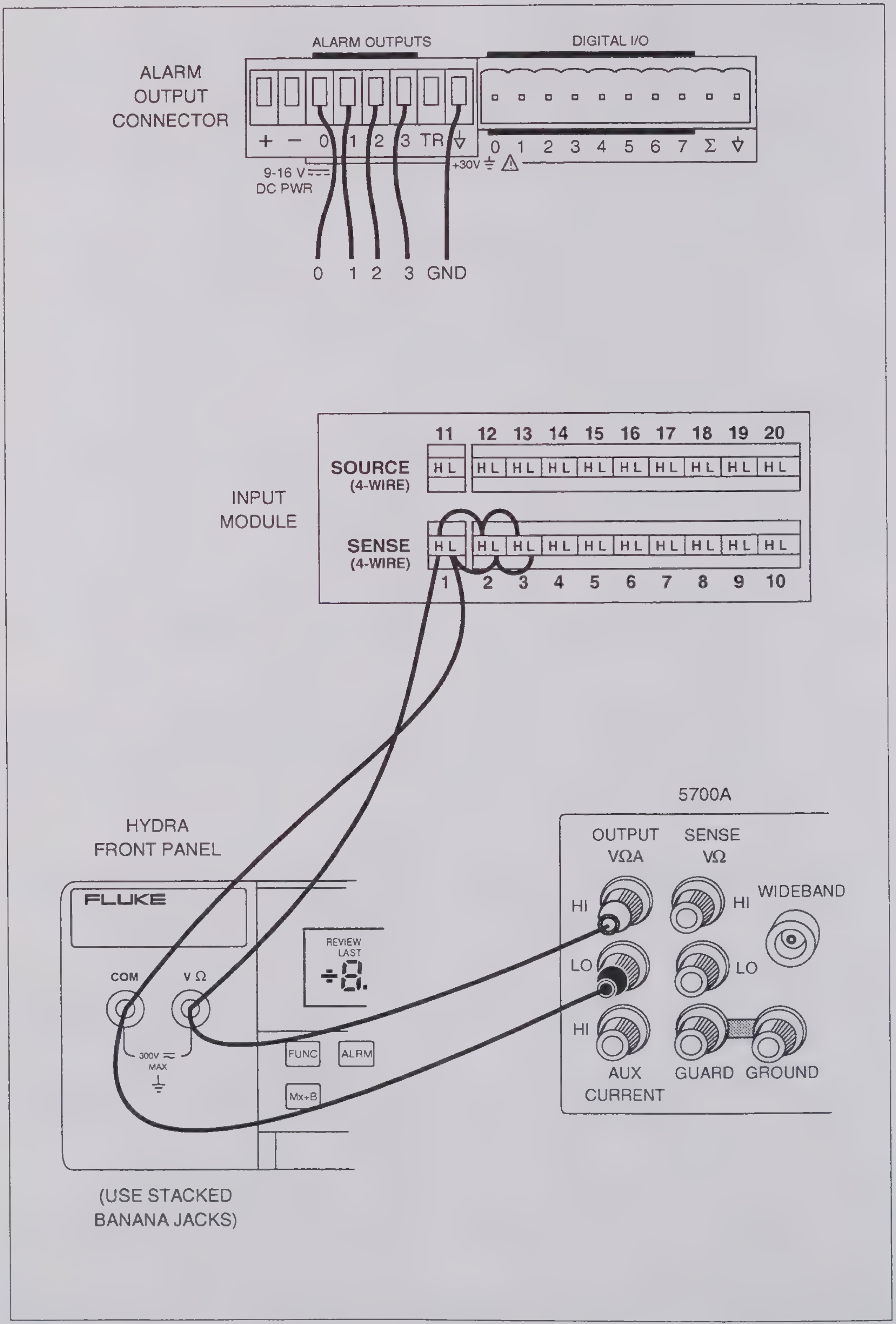

ALARM OUTPUT CONNECTOR
ALARM OUTPUTS
DIGITAL I/O
+ − 0 1 2 3 TR
9-16 V DC PWR
+30V
0 1 2 3 4 5 6 7 Σ
0 1 2 3 GND
INPUT MODULE
SOURCE (4-WIRE)
SENSE (4-WIRE)
11 12 13 14 15 16 17 18 19 20
H L
1 2 3 4 5 6 7 8 9 10
HYDRA FRONT PANEL
FLUKE
COM
V Ω
300V MAX
REVIEW LAST
FUNC
ALRM
Mx+B
5700A
OUTPUT VΩA
SENSE VΩ
HI
LO
WIDEBAND
AUX CURRENT
GUARD
GROUND
(USE STACKED BANANA JACKS)

Figure 4-3. Dedicated Alarms Test

External Trigger Input Test 4-19.

The External Trigger Input Test verifies that the rear panel trigger input of Hydra is functioning properly.

1. Switch OFF power to the instrument and disconnect all high voltage inputs.
2. Remove the eight-terminal Alarm Output connector from the rear of Hydra and all external connections to it. Connect short wires (to be used as test leads) to the ⏚ and TR terminals. Leave other ends of wires unconnected at this time. Reinstall the connector. Refer to Figure 4-4.
3. Switch power ON.
4. On Hydra, select the VDC function, 30V range for channels 0 through 5. Select a scan interval of 30 seconds.
5. Select trigger ON to enable the external trigger input. Press SHIFT, then MON(TRIGS). (The display shows TRIG.) Then press either the up or down arrow buttons until the display shows ON. Finally, press ENTER.
6. Press the Hydra SCAN button. Hydra should scan channels 0 through 5 once every 30 seconds.
7. During the interval when scanning is not occurring, connect (short) the test leads of the TR and ground Alarm Output terminals.

   Ensure the connection causes a single scan to occur.
8. Disconnect (open) the TR and ground connection.

   Ensure the scan continues to execute at its specified interval.

CALIBRATION 4-20.

Hydra calibration is controlled with computer interface commands. The 2620A may be calibrated by using the IEEE-488 or RS-232 interface, but the 2625A and 2635A may only be calibrated via their RS-232 interface. Local (front panel) calibration is not possible.

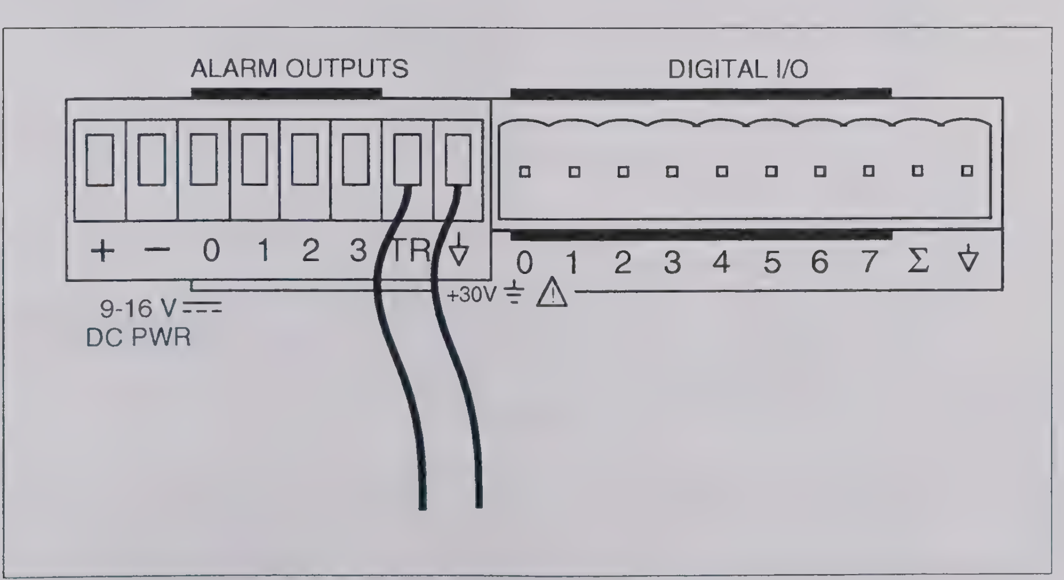


Figure 4-4. External Trigger Test

Activate calibration mode by pressing and holding the CAL Enable button (front panel) for approximately 4 seconds. Release the button after Hydra beeps and the CAL annunciator lights.

NOTE

The CAL Enable button is located on the right side of the display and is recessed beneath a calibration seal. Press this button with a blunt-tipped object. Avoid using a sharper-tipped object (such as a pencil). Do not press CAL ENABLE unless you intend to calibrate the instrument. If you have activated Calibration and wish to exit calibration immediately, press CAL ENABLE momentarily a second time.

The instrument must be stabilized in an environment with ambient temperature of 22 to 24°C and relative humidity of less than 70% and have been turned on for at least 1/2 hour prior to calibration.

The instrument should normally be calibrated on a regular cycle, typically every 90 days or 1 year. The chosen calibration cycle depends on the accuracy specification you wish to maintain. The instrument should also be calibrated if it fails the performance test or has undergone repair.

The instrument features closed-case calibration controlled over the Computer Interface. Using known reference sources, closed-case calibration has many advantages. There are no parts to disassemble, no mechanical adjustments to make, and the instrument can be calibrated by an automated instrumentation system.

Once the instrument is in calibration mode, closed-case calibration can be made for the four calibration groups: Volts DC, Volts AC, Resistance, and Frequency. Once begun, each group must be completed successfully for the results of the calibration to be made permanent. It is not necessary to perform all calibration groups. Each group is independent of the other three groups; completion of a group sets the constants for that group.

Analog inputs are made at the rear-panel Input Module, and computer interface commands are used to control each step of the process. Either of the following two closed-case calibration procedures can be used:

- Using Hydra Starter Calibration Software

  This procedure uses software supplied with this Service Manual. Instructions for each step are presented on the PC screen.

- Using a Terminal

  This procedure relies on individual commands for each step. A summary of these commands is presented in Table 4-8.

With either closed-case procedure, an additional procedure (reference junction calibration) may be used to calibrate the thermocouple temperature function. This procedure requires physical access to the rear panel Input Module.

NOTE

The instrument returns a Device Dependent Error prompt (!>) if a calibration step fails. Usually, this happens if the reference is not within an anticipated range (5 to 15%, depending on the step). At this point, the response to the CAL_STEP? command equals the raw, uncalibrated reading taken on the reference input. Refer to Calibration Failures in Section 5 for more information.

Table 4-8. Calibration Mode Computer Interface Commands

<table>
<tr><th>COMMAND</th><th>DESCRIPTION</th></tr>
<tr><td>CAL x</td><td>Start calibration of a new function.
<table>
<tr><td>x</td><td>Function to calibrate</td></tr>
<tr><td>1</td><td>VDC</td></tr>
<tr><td>2</td><td>VAC</td></tr>
<tr><td>3</td><td>ohms</td></tr>
<tr><td>4</td><td>Frequency</td></tr>
</table></td></tr>
<tr><td>CAL_CLR</td><td>Reset all calibration constants to nominal values, clearing present calibration.</td></tr>
<tr><td>CAL_CONST? xx</td><td>Return the value of the calibration constant indicated by xx.</td></tr>
<tr><td>CAL_REF?</td><td>Return the present calibration reference.</td></tr>
<tr><td>CAL_REF <value></td><td>Calibrate to <value>, rather than the default calibration reference value.</td></tr>
<tr><td>CAL_STEP?</td><td>Calibrate and return the calibrated value of the input.</td></tr>
<tr><td>EEREG? xx</td><td>Return the contents of the specified EEPROM register (xx).</td></tr>
<tr><td colspan="2">The following additional computer interface commands can be used in calibration mode. Use of any other command results in an execution error. Refer to Section 4 of the Hydra Users Manual for complete information about these computer interface commands.
*CLS *ESE *ESE? *ESR? *IDN? *OPC *OPC? *RST *SRE *SRE? *STB? *TRG *WAI IEE IEE? IER? LOCS LWLS REMS RWLS</td></tr>
</table>

To provide accuracy at full range, calibration is not recommended below one-third of full range (10000 counts).

Using Hydra Starter Calibration Software 4-21.

This procedure uses the Hydra Starter Package (with Calibration Software) for closed-case calibration. This software runs on an IBM PC or equivalent using the RS-232 interface. It consists of the following three files:

- An executable file (CAL.EXE)
- A help text file (CAL.HLP)
- A configuration initialization file (CAL.INI)

SETUP PROCEDURE USING STARTER 4-22.

Use the following procedure to set up Hydra and the PC prior to using the calibration feature of the Hydra Starter Package:

1. Connect a pair of test leads to the channel 1 H (high) and L (low) terminals on the Input Module. Connect a second pair of test leads to channel 11. (This second pair is used only for 4-wire resistance calibration.) Install the Input Module into Hydra.

2. Using the RS40 Terminal Interface Cable, connect the PC COM port to the Hydra RS-232 port. Use an RS40 and an RS41 cable in series to connect to the COM port on an IBM PC/AT.

3. From the CAL directory on the PC, type CAL. Then press any key to start the program and access the SETUP menu.

4. On Hydra, press POWER ON. After the initialization process has concluded, use the following procedure to set up communications:
    a. Press SHIFT and then LIST(COMM).
    b. With 'BAUd' displayed, use the UP or DOWN arrow key to select the desired baud rate. Then press ENTER.
    c. With 'PAR' (parity) displayed, use the UP or DOWN arrow key to select the parity. Then press ENTER.
    d. With 'CtS' (2635A only; Clear to Send) displayed, use the UP or DOWN arrow key to select the Clear to Send flow control 'OFF'. Then press ENTER.
    e. With 'ECHO' displayed, use the UP or DOWN arrow key to select 'OFF'. Then press ENTER. Communications setup for Hydra is now complete.
5. On the PC, use the SETUP menu to match the communication parameters defined above for Hydra.
6. On Hydra, break the calibration seal on the front panel display. Then press and hold the CAL Enable button (approximately 4 seconds) until 'CAL' is displayed. Press this button with a blunt-tipped object. Avoid using a sharper-tipped object (such as a pencil).
7. On the PC, use the right and left arrow keys to select CAL. Then press the ENTER key. A message asking if you want to calibrate is displayed. Press Y and ENTER. The next displayed message specifies the voltage to be applied to channel 1.

CALIBRATION PROCEDURE USING STARTER 4-23.

Use the following procedure to calibrate Hydra with the Hydra Starter Package:

1. Connect the channel 1 test leads to the 5700A output.
2. On the 5700A, select the output voltage specified on the PC (step 7 above.)
3. On the PC, press ENTER. If the input voltage is within a predetermined acceptable boundary, Hydra performs a calibration for this step. The program then prompts you for the next input value.

NOTE

"Bad Calibration Input Value" is returned if the input is not acceptable (the calibration step could not be executed.) Verify that the input to Hydra channel 1 is the correct value and polarity. Also verify that the 5700A is in OPERATE mode. If the input is correct and "Bad Calibration Input Value" is still returned, repair of Hydra may be required.

4. Following the prompts, complete all steps for this calibration group.
5. You will then be asked if you want to perform the next calibration group. Press Y - ENTER.
6. Following the prompts, complete all steps in the remaining calibration groups.

Using a Terminal 4-24.

This procedure can be used with either a terminal or a computer running a terminal emulation program.

SETUP PROCEDURE USING A TERMINAL 4-25.

Use the following procedure to set up Hydra and the PC:

1. Connect a pair of test leads to the high and low terminals of channel 1 on the Hydra Input Module. Connect a second pair of test leads to channel 11.
2. Install the Input Module into Hydra.
3. Connect the COM port of the PC or terminal to the Hydra RS-232 port using an RS40 Terminal Interface Cable. Use an RS40 and an RS41 cable in series to connect to the COM port on an IBM PC/AT.
4. On Hydra, press POWER ON. After the initialization process has concluded, use the following procedure to set up communications:
    a. Press SHIFT and then LIST(COMM).
    b. With ‘BAUd’ displayed, use the UP or DOWN arrow key to select the desired baud rate. Then press ENTER.
    c. With ‘PAR’ (parity) displayed, use the UP or DOWN arrow key to select the parity. Then press ENTER.
    d. With ‘CtS’ (2635A only; Clear to Send) displayed, use the UP or DOWN arrow key to select the Clear to Send flow control ‘OFF’. Then press ENTER.
    e. With ‘ECHO’ displayed, use the UP or DOWN arrow key to select ‘ON’. Then press ENTER. Communications setup for Hydra is now complete.
5. On the terminal, match the communication parameters used for Hydra (above).
6. On Hydra, break the calibration seal on the front panel display. Then press and hold the CAL Enable button (approximately 4 seconds) until CAL is shown on the Hydra display. Press this button with a blunt-tipped object. Avoid using a sharper-tipped object (such as a pencil).
7. Connect the channel 1 test leads to the output of a 5700A.

CALIBRATION PROCEDURE USING A TERMINAL 4-26.

Calibration procedures using a terminal (or a computer program that emulates a terminal) are presented in the following tables:

- DC Volts (CAL 1) Calibration: Table 4-9
- AC Volts (CAL 2) Calibration: Table 4-10
- Ohms (CAL 3) Calibration: Tables 4-11, 4-12
- Frequency (CAL 4) Calibration: Table 4-13

In the tables, the CAL_REF? query asks Hydra for the next calibration reference value. If some other value is to be used, the CAL_REF xxx.xxxx command tells Hydra the calibration reference value to expect.

To provide accuracy at full range, calibration is not recommended below one-third of full range (10000 counts).

Once the calibrator output has been set to Hydra, the CAL_STEP? query performs the calibration step and returns the calibrated value of the input. The response to CAL_STEP? must be received before each new step can begin. With some steps, a noticeable delay may be encountered.

Ohms Calibration 4-27.

Resistor values of 290Ω, 2.9 kΩ, 29 kΩ, 290 kΩ, and 2.9 MΩ are preferred. Use either fixed resistors or a decade resistance source having the required accuracy (see Table 4-1.) Connect the channel 11 test leads and the channel 1 test leads to the source resistance. Refer to Figure 4-5 and Table 4-11 for related setup and calibration procedures.

The 5700A can also be used as a resistance source. Connect the 5700A to Hydra for 4-Wire Ohms Calibration. Connect the channel 11 test leads to the 5700A OUTPUT terminals and the channel 1 test leads to the 5700A SENSE terminals. Verify that 5700A EXT SNS is ON. Select the 5700A output as specified in each step. Refer to Figure 4-6 and Table 4-12 for related setup and calibration procedures.

NOTE

The 300 kΩ, 3 MΩ, and 10 MΩ ranges are sensitive to noise. Any movement of the input leads can cause noisy readings. Use shielded leads and verify these two calibration points at the conclusion of calibration.

Reference Junction Calibration 4-28.

NOTE

This procedure is necessary only if the Input Module has been repaired or damaged, or if R3 on the Input Module has been inadvertently adjusted.

If thermocouple readings taken in the Thermocouple Temperature Accuracy Test section of the performance tests are found to be out of tolerance, the Input Module Reference Junction may require calibration. First, check the volts dc calibration. If volts dc calibration is correct, perform the following steps:

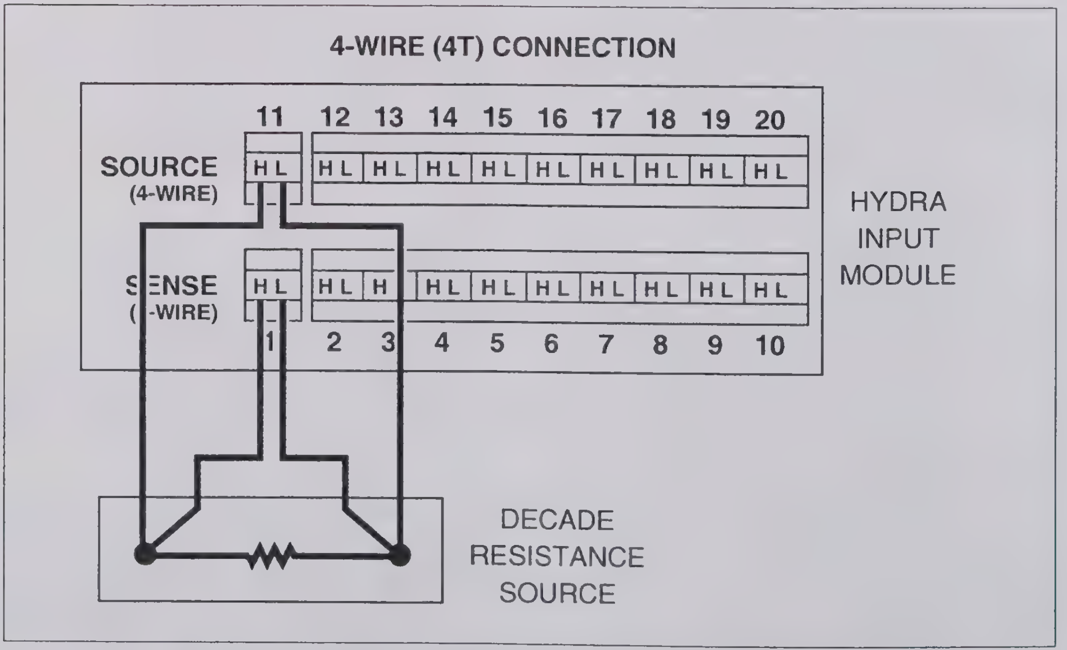


Figure 4-5. 4-Terminal Connections to Decade Resistance Source

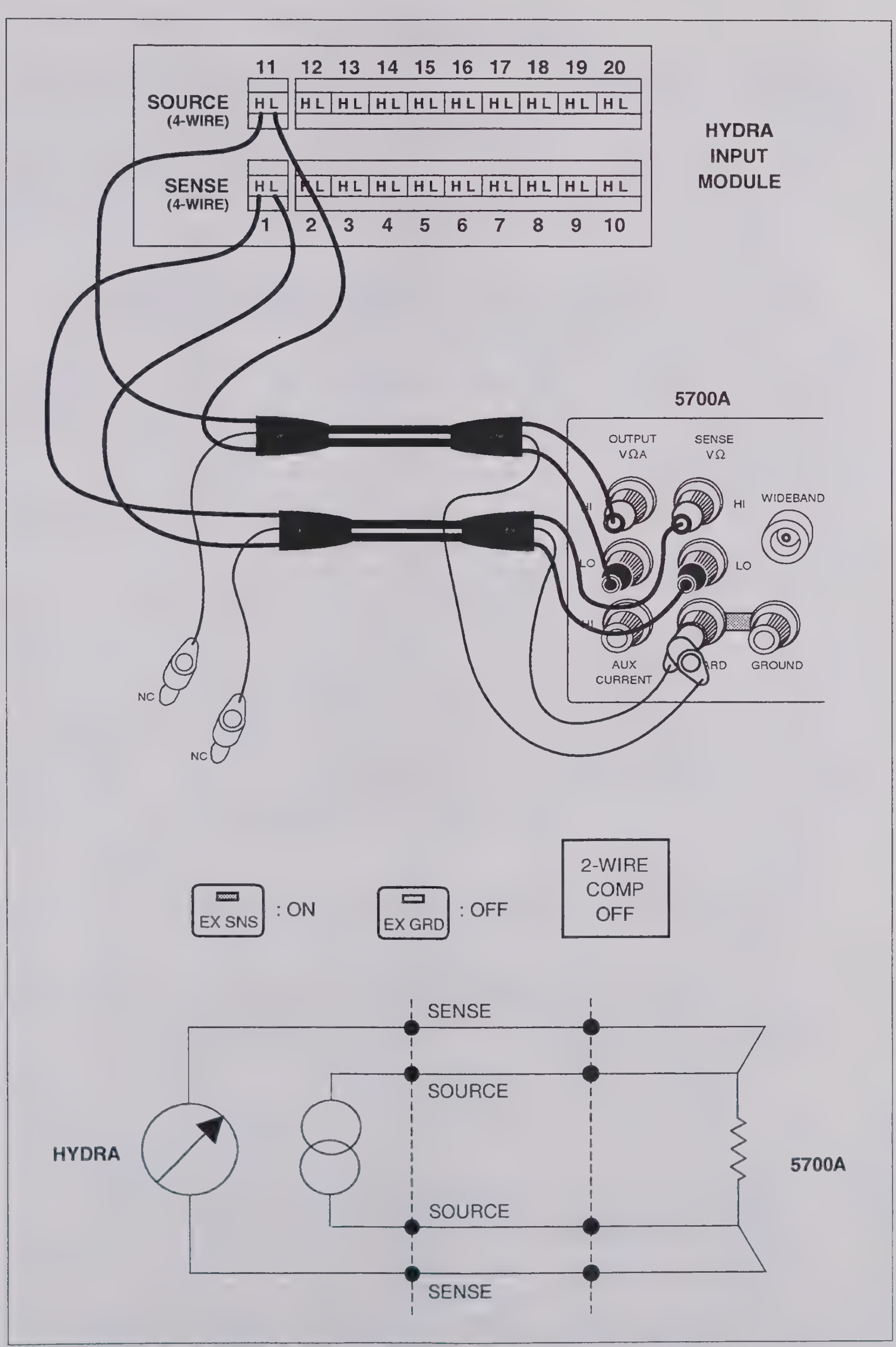

11 12 13 14 15 16 17 18 19 20
SOURCE
(4-WIRE)
H L
SENSE
(4-WIRE)
1 2 3 4 5 6 7 8 9 10
HYDRA
INPUT
MODULE
5700A
OUTPUT
VΩA
SENSE
VΩ
HI
LO
WIDEBAND
AUX
CURRENT
GUARD
GROUND
NC
NC
EX SNS
: ON
EX GRD
: OFF
2-WIRE
COMP
OFF
SENSE
SOURCE
HYDRA
SOURCE
SENSE
5700A

Figure 4-6. 4-Terminal Connections to the 5700A

Table 4-9. DC Volts Calibration

COMMAND	RESPONSE	ACTION
CAL 1	=>	Puts Hydra in VDC Calibration.
CAL_REF?	+90.000E-3	You output 90 mV dc from the 5700A. Wait about 10 seconds.
CAL_STEP?		Hydra computes calibration constant 1 and returns the calibrated reading (for example, +90.000E-3.)
NOTE *If the input is incorrect, the "!>" response signifies that a Device Dependent Error was generated. The calibration step could not be executed. Verify that the input to Hydra channel 1 is the correct value and polarity. Also verify that the 5700A is in OPERATE mode. If the input is correct, Hydra may require repair.*		
CAL_REF?	+900.00E-3	You output 900 mV dc from the 5700A. Wait 4 seconds.
CAL_STEP?		Hydra computes calibration constant 2 and returns the calibrated reading.
CAL_REF?	+290.00E-3	You output 290 mV dc and wait 4 seconds.
CAL_STEP?		Hydra computes calibration constant 3 and returns the calibrated reading.
CAL_REF?	+2.9000E+0	You output 2.9V dc and wait 4 seconds.
CAL_STEP?		Hydra computes calibration constant 4 and returns the calibrated reading.
CAL_REF?	+29.000E+0	You output 29V dc and wait 4 seconds.
CAL_STEP?		Hydra computes calibration constant 5 and returns the calibrated reading.
CAL_REF?	+290.00E+0	You output 290V dc and wait 4 seconds.
CAL_STEP?		Hydra computes calibration constant 6 returns the calibrated reading. Now change the 5700A output to 0.0V dc.

1. Perform the Volts DC group calibration.
2. Switch OFF power to Hydra, and remove the Input Module from the rear of the instrument.
3. Remove the module top cover by loosening the two securing screws, fully opening the module top and gently prying either of the hinge ears away from the main body of the module. Refer to Figure 4-1.
4. Connect a KNBS thermocouple to the H (high) and L (low) terminals of channel 15. Refer to Table 4-3 for thermocouple lead colors. Reinstall the module (without the top cover) into the instrument.
5. Press the Hydra POWER button ON.
6. Insert the thermocouple and a mercury thermometer in a stable, thermally-isolated, room-temperature bath. Allow 20 minutes for thermal stabilization.
7. Select the temperature function and K thermocouple type for channel 15. Select the slow measurement rate. Then press MON.
8. Adjust resistor R3 (see Figure 4-1) on the Input Module until Hydra displays the same temperature reading as the mercury thermometer.
9. Calibration of the Input Module is now complete. Remove the Input Module and disconnect the thermocouple. Then attach and secure the module cover.

Table 4-10. AC Volts Calibration

COMMAND	RESPONSE	ACTION
CAL 2	=>	Puts Hydra in VAC Calibration.
CAL_REF?	+029.00E-3	You output 29 mV ac at 1 kHz from the 5700A. Wait about 8 seconds.
CAL_STEP?		Hydra computes calibration constant 7 and returns the calibrated reading (for example, +029.00E-3.)
NOTE *If the input is incorrect, the "!>" response signifies that a Device Dependent Error was generated. The calibration step could not be executed. Verify that the input to Hydra channel 1 is the correct value and polarity. Also verify that the 5700A is in OPERATE mode. If the input is correct, Hydra may require repair.*		
CAL_REF?	+290.00E-3	You output 290 mV at 1 kHz from the 5700A. Wait 8 seconds.
CAL_STEP?		Hydra computes calibration constant 8 and returns the calibrated reading.
CAL_REF?	+0.2900E+0	You output 290 mV at 1 kHz from the 5700A and wait 8 seconds.
CAL_STEP?		Hydra computes calibration constant 9 and returns the calibrated reading.
CAL_REF?	+2.9000E+0	You output 2.9V at 1 kHz from the 5700A and wait 8 seconds.
CAL_STEP?		Hydra computes calibration constants 10 and 11 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 10 only.)
CAL_REF?	+29.000E+0	You output 29V at 1 kHz and wait 8 seconds.
CAL_STEP?		Hydra computes calibration constants 12 and 13 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 11 only.)
CAL_REF?	+290.00E+0	You output 290V at 1 kHz and wait 8 seconds.
CAL_STEP?		Hydra computes calibration constant 14 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 12.) Now set the 5700A output to 0 volts.

Concluding Calibration 4-29.

At the conclusion of this type of calibration, first make sure the source is cleared. Then press the CAL Enable button on the instrument to exit calibration mode.

Calibration mode can also be exited at any time by sending the *RST Computer Interface command. If this command is sent prior to completion of all calibration points for the selected function, no changes are made to nonvolatile calibration memory for that function.

UPDATING 2635A DATA BUCKET EMBEDDED INSTRUMENT FIRMWARE 4-30.

The instrument firmware in the 2635A Hydra Data Bucket can be easily updated without even opening the instrument case or replacing any parts. The instrument firmware is stored in electrically eraseable and programmable Flash memory.

A diskette which contains the necessary software and the latest release of 2635A Data Bucket firmware may be obtained from either your local Fluke authorized service center or the Fluke factory. The local service centers are listed in Section 6 of this manual.

Table 4-11. 4-Wire Ohms Calibration (Fixed Resistor)

COMMAND	RESPONSE	ACTION
CAL 3	=>	Puts Hydra in OHMS Calibration.
CAL_REF?	+290.00E+0	You source 290Ω from the decade resistance source or fixed resistor.
CAL_STEP?		Hydra computes calibration constant 15 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 13.)
NOTE *If the input is incorrect, the "!>" response signifies that a Device Dependent Error has been generated. The calibration step could not be executed. Verify that the input to Hydra channel 1 is the correct value. If the input is correct, Hydra may require repair.*		
CAL_REF?	+2.9000E+3	You source 2900Ω .
CAL_STEP?		Hydra computes calibration constant 16 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 14.)
CAL_REF?	+29.000E+3	You source 29000Ω .
CAL_STEP?		Hydra computes calibration constant 17 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 15.)
CAL_REF?	+290.00E+3	You source 290000Ω .
CAL_STEP?		Hydra computes calibration constant 18 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 16.)
CAL_REF?	+2.9000E+6	You source 2900000Ω .
CAL_STEP?		Hydra computes calibration constants 19 and 20 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constants 17 and 18.)

Contact the one nearest you. To request the "2635A Embedded Firmware Memory Loader" diskette from the factory, telephone or send a fax to:

John Fluke Mfg. Co. Data Acquisition Sales Support Telephone: (206) 356-5870 FAX: (206) 356-5790

Using the PC Compatible Firmware Loader Software 4-31.

This procedure uses the 2635A Embedded Firmware Memory Loader Package for closed-case updating of the internal firmware in the 2635A. This software runs on an IBM PC or equivalent using the RS-232 interface. It consists of the following files:

- An executable file (LD2635.EXE)
- A text file containing usage information (README.TXT)
- A 2635A instrument firmware file (DB_6_9.HEX for example)
- A batch file to load the firmware via COM port #1 (LOADC1.BAT)
- A batch file to load the firmware via COM port #2 (LOADC2.BAT)

Firmware downloading may be accomplished by using either of the two methods that are described in the following paragraphs.

- Default Instrument Firmware Download Procedure
- Using LD2635 Firmware Loader Directly

Table 4-12. 4-Wire Ohms Calibration (5700A)

COMMAND	ACTION
CAL 3	Puts Hydra in OHMS Calibration.
NOTE *With the following CAL_REF commands, send the actual resistance value (e.g., xxx.xxxxx) displayed by the 5700A.*	
	Source 190Ω from the 5700A. Then wait 4 seconds for the 5700A to settle.
CAL_REF xxx.xxxxx	
CAL_STEP?	Hydra computes calibration constant 15 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 13.)
NOTE *If the input is incorrect, the "!>" response signifies that a Device Dependent Error has been generated. The calibration step could not be executed. Verify that the input to Hydra channel 1 is the correct value. Also verify that the 5700A is in OPERATE mode. If the input is correct, Hydra may require repair.*	
	Source 1.9 kΩ from the 5700A. Then wait 4 seconds for the 5700A to settle.
CAL_REF xxxx.xxxx	
CAL_STEP?	Hydra computes calibration constant 16 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 14.) Source 19 kΩ from the 5700A. Then wait 4 seconds for the 5700A to settle.
CAL_REF xxxxx.xxx	
CAL_STEP?	Hydra computes calibration constant 17 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 15.) Source 190 kilohms from the 5700A. Then wait 4 seconds for the 5700A to settle.
CAL_REF xxxxxx.xx	
CAL_STEP?	Hydra computes calibration constant 18 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 16.) Source 1.9 megohms from the 5700A. Then wait 4 seconds for the 5700A to settle.
CAL_REF xxxxxxx.x	
CAL_STEP?	Hydra computes calibration constants 19 and 20 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constants 17 and 18.) Now set the 5700A output to 0.

SETUP PROCEDURE FOR FIRMWARE DOWNLOAD 4-32.

Use the following procedure to set up the 2635A and the PC, before attempting to download firmware to the instrument:

1. Copy the files from the diskette to your PC hard drive. All following PC operations should be done in the directory on the PC where these files are located.
2. Using the RS40 Terminal Interface Cable, connect the PC COM port to be used to the 2635A RS-232 port. Use an RS40 and an RS41 cable in series to connect to the COM port on an IBM PC/AT.
3. On the 2635A, press POWER ON. After the initialization process has concluded, use the following procedure to set up communications:
   a. Press SHIFT and then LIST(COMM).
   b. With ‘BAUd’ displayed, use the UP or DOWN arrow key to select ‘19200’ baud. Then press ENTER.
   c. With ‘PAR’ (parity) displayed, use the UP or DOWN arrow key to select ‘no’ parity. Then press ENTER.
   d. With ‘CtS’ displayed, use the UP or DOWN arrow key to select the Clear to Send flow control ‘On’. Then press ENTER.
   e. With ‘ECHO’ displayed, use the UP or DOWN arrow key to select ‘OFF’. Then press ENTER. Communications setup for the 2635A is now complete.

DEFAULT INSTRUMENT FIRMWARE DOWNLOAD PROCEDURE 4-33.

Use the following procedure to download the version of 2635A instrument firmware that is distributed on the diskette:

1. If it is important to retain the channel programming information in the instrument, store a copy of the instrument configuration setup on a memory card. Refer to section on “Using SETUP STORE” in section 3 of the 2635A Data Bucket Users Manual.
2. To load the instrument firmware, run ‘LOADC1.BAT’ if COM port #1 is to being used. Otherwise, run ‘LOADC2.BAT’ if COM port #2 is to being used. These batch files execute ‘LD2635’ in batch mode with the proper command line switches to download the default instrument firmware via the proper COM port.
3. After successful loading of the instrument firmware, the instrument will be reset to begin normal operation. It is not abnormal to see an “ERROR 6” indication displayed by the instrument as it begins operation again. This just indicates that the internal instrument configuration has been reset to factory defaults. If you saved the instrument configuration during step 1, you can reload it into the instrument now. Refer to section “Using SETUP LOAD” in section 3 of the 2635A Data Bucket Users Manual.

USING LD2635 FIRMWARE LOADER DIRECTLY 4-34.

The ‘LD2635’ program may be used interactively or in batch mode by using command line switches. The command line syntax is

```
LD2635 [/B /Cn /Fname]
```

where the command line switches are defined as follows:

/B	Execute in batch mode; program exits when firmware programming is complete. If batch mode is not specified, user is asked whether or not another instrument is to be updated each time an instrument is completed. (/Cn and /Fname switches must be included if batch mode is specified.)

Table 4-13. Frequency Calibration

COMMAND	RESPONSE	ACTION
CAL 4	=>	Put Hydra in Frequency Cal.
CAL_REF?	+10.000E+3	Output 2.9 volts ac at 10 kHz from the 5700A. Wait about 8 seconds.
CAL_STEP?		Hydra computes calibration constant 21 and returns the calibrated reading (for example, +10.000E+3.) (For software versions lower than 5.4, this step computes calibration constant 19.)
NOTE *If the input is incorrect, the "!>" response signifies that a Device Dependent Error has been generated. The calibration step could not be executed. Verify that the input to Hydra channel 1 is the correct value. Also verify that the 5700A is in OPERATE mode. If the input is correct, Hydra may require repair.*		
		Now set the 5700A output to 0V dc.

/Cn	Use COMM port #n (n = 1 or 2)
/Fname	Download named firmware file to the 2635A

For example, to program multiple instruments with version 6.9 of the instrument firmware via COM port #2, execute:

```
ld2635 /fdb_6_9.hex /c2
```

or to do the same with only one instrument:

```
ld2635 /b /fdb_6_9.hex /c2
```

The 'ld2635' program can be used interactively by running it without any command line switches. It will then request the name of the firmware file and the COM port to be used before going on to update the firmware in the instrument. Since this is not batch mode, the user is asked whether or not another instrument is to be updated each time an instrument is completed.

If any errors are detected in establishing communication with the 2635A or updating the firmware in the instrument, descriptive error messages will be printed to the PC console before the program exits. Make sure that the PC is connected to the 2635A as previously described, and that the 2635A communication parameters have been set correctly.

Section 5

Diagnostic Testing and Troubleshooting (2620A/2625A)

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INTRODUCTION 5-1.

Hydra provides error code information and semi-modular design to aid in troubleshooting. This section explains the error codes and describes procedures needed to isolate a problem to a specific functional area. Finally, troubleshooting hints for each functional area are presented.

But first, if the instrument fails, check the line voltage fuse and replace as needed. If the problem persists, verify that you are operating the instrument correctly by reviewing the operating instructions found in the Hydra Users Manual.

WARNING

OPENING THE CASE MAY EXPOSE HAZARDOUS VOLTAGES. ALWAYS DISCONNECT THE POWER CORD AND MEASURING INPUTS BEFORE OPENING THE CASE. AND REMEMBER THAT REPAIRS OR SERVICING SHOULD BE PERFORMED ONLY BY QUALIFIED PERSONNEL.

Required equipment is listed in Section 4 of this manual.

Signal names followed by a '*' are active (asserted) low. Signal names not so marked are active high.

SERVICING SURFACE-MOUNT ASSEMBLIES 5-2.

Hydra incorporates Surface-Mount Technology (SMT) for printed circuit assemblies (pca's). Surface-mount components are much smaller than their predecessors, with leads soldered directly to the surface of a circuit board; no plated through-holes are used. Unique servicing, troubleshooting, and repair techniques are required to support this technology. The information offered in the following paragraphs serves only as an introduction to SMT. It is not recommended that repair be attempted based only on the information presented here. Refer to the Fluke "Surface Mount Device Soldering Kit" for a complete demonstration and discussion of these techniques. (In the USA, call 1-800-526-4731 to order.)

Since sockets are seldom used with SMT, "shotgun" troubleshooting cannot be used; a fault should be isolated to the component level before a part is replaced. Surface-mount assemblies are probed from the component side. The probes should make contact only with the pads in front of the component leads. With the close spacing involved, ordinary test probes can easily short two adjacent pins on an SMT IC.

This Service Manual is a vital source for component locations and values. With limited space on the circuit board, chip component locations are seldom labeled. Figures provided in Section 6 of this manual provide this information. Also, remember that chip components are not individually labeled; keep any new or removed component in a labeled package.

Surface-mount components are removed and replaced by reflowing all the solder connections at the same time. Special considerations are required.

- The solder tool uses regulated hot air to melt the solder; there is no direct contact between the tool and the component.
- Surface-mount assemblies require rework with wire solder rather than with solder paste. A 0.025-inch diameter wire solder composed of 63% tin and 37% lead is recommended. A 60/40 solder is also acceptable.
- A good connection with SMT requires only enough solder to make a positive metallic contact. Too much solder causes bridging, while too little solder can cause weak or open solder joints. With SMT, the anchoring effect of the through-holes is missing; solder provides the only means of mechanical fastening. Therefore, the pca must be especially clean to ensure a strong connection. An oxidized pca pad causes the solder to wick up the component lead, leaving little solder on the pad itself.

Refer to the Fluke "Surface Mount Device Soldering Kit" for a complete discussion of these techniques.

ERROR CODES 5-3.

At reset, the Hydra software performs power-up self-tests and initialization of ROM, NVRAM, Display, EEPROM, and measurement hardware. Self-test failures are reported on the display with "Error" in the left display and an error code (1-9,A,b,C) in the right display.

Several of these error codes might never be displayed. Certainly, errors 4 and 5, which signify a faulty or dead display, could not be reported in the normal (displayed) manner. Other errors might not appear on the display. Therefore, the following additional methods exist for accessing error information:

- The computer interfaces can be used to determine self-check status using the *TST? query. Refer to Section 4 of the Hydra Users Manual for a description of the *TST? response. Note that the extent of the error-producing damage could also cause the instrument to halt before the computer interfaces are operational.
- The POWERUP? computer interface command can be used to determine which errors were detected at power-up. POWERUP? uses the same response format as *TST?; refer to *TST? in Section 4 of the Hydra Users Manual.
- The keyboard scan lines (A1U4, SWR1-5), which are also used as status indicators, can be checked as a last resort for accessing error information. The software sets SWR1 (A1U4-21) low to indicate that the basic operation of the processor, ROM, and ROM decode circuitry is intact. SWR2 (A1U4-22) is set low if the ROM (A1U8) check passes. SWR3 (A1U4-23) is set low if the external NVRAM (A1U3) check passes, and SWR4 (A1U4-24) is set low if the internal RAM (A1U4) check passes. Then, if the display self-check passes, SWR5 (A1U4-25) is set low to indicate that the display is operational.

Table 5-1 describes the error codes.

NOTE

Each error code is displayed for 2 seconds.

Table 5-1. Error Codes

ERROR	DESCRIPTION
1	ROM (A1U8) checksum error
2	External RAM (A1U3) test failed
3	Internal RAM (A1U4) test failed
4	Display power-up test failure
5	Display not responding
6	Instrument configuration corrupted
7	EEPROM instrument configuration corrupted
8	EEPROM calibration data corrupted
9	A/D not responding
A	A/D ROM test failure (A3U9)
b	A/D RAM test failure (A3U9)
C	A/D self test failure
Refer to Troubleshooting information later in this section.	
Error 1	ROM (A1U8) checksum match failed. All the bytes in the ROM (including a checksum byte) are summed.
Error 2	External RAM (A1U3) check failed.
Error 3	Internal RAM (A1U4) check failed. Complementary patterns are alternately written and read from each RAM location for both external RAM and the 256 bytes internal to the 6303Y Microprocessor (A1U4). If the pattern read from any RAM location is not the same as the pattern written, the test fails.
Error 4	Display self-check failed.
Error 5	Display dead. The display processor automatically performs a self-check on power-up, and the Microprocessor attempts to read the result of this test.
Error 6	Instrument configuration The instrument configuration information stored in nonvolatile RAM (A1U3) has been corrupted. (The Cyclic Redundancy Checksum on this memory is not correct for the information stored there.) The instrument configuration is reset to the default configuration.
Error 7	EEPROM instrument configuration corrupted or EEPROM not initialized.
Error 8	EEPROM calibration data corrupted. The EEPROM (A1U1) is divided into two storage areas: the instrument configuration storage and calibration data storage. Each area uses a Cyclic Redundancy Checksum (CRC), against which the data is checked on power-up. • Error 7 is reported if the instrument configuration check finds an error; the instrument configuration is set to factory defaults. • If the calibration data CRC verification indicates that there is calibration data that is in error, the front panel CAL annunciator is turned on, and Error 8 is reported.
NOTE *Errors 7 and 8 should always appear the first time an instrument is powered up with a new, uninitialized EEPROM. Error 8 continues to appear at subsequent power-ups until the instrument is fully calibrated.*	
Error 9	A/D Microcomputer (A3U9) failed to respond This error is displayed if communication cannot be established with the 6301Y Microcomputer (A3U9).
Error A	A/D ROM test failure All bytes of internal ROM for the 6301Y Microcomputer (A3U9) (including the checksum byte) are summed.

Table 5-1. Error Codes (cont)

ERROR	DESCRIPTION
Error b	A/D RAM test failure Complementary patterns are alternately written to and read from each location of the 256 bytes of RAM internal to the 6301Y Microcomputer (A3U9).
Error C	A/D self test failed The Analog Measurement Processor (A3U8) is programmed to do self test measurements.

GENERAL TROUBLESHOOTING PROCEDURES 5-4.

Hydra allows for some fault isolation using self-diagnostic routines and descriptive error codes. However, these features are somewhat limited and do not provide in-depth troubleshooting tools.

Hydra incorporates a semi-modular design; determining modules not related to a problem constitutes the first step in the troubleshooting process.

As a first step, remove the IEEE-488 Option (if installed) from the Data Acquisition Unit (2620A) or the Memory PCA from the Data Logger (2625A). Refer to Section 3 of this manual for removal procedures. If removal of either of these assemblies results in improved instrument operation, refer to Section 7 for IEEE-488 Option troubleshooting or later in this section for Memory PCA troubleshooting.

Measuring the power supplies helps to isolate a problem further. Refer to Table 5-2 and Figure 5-1 for test point identification and readings. If power supply loading is suspected, disconnect the Display PCA at A1J2. If this action solves the loading problem, proceed to Display Assembly Troubleshooting elsewhere in this section. Otherwise, refer to Power Supply Troubleshooting.

If the power supplies appear good, check the E clock signal to determine whether the Main PCA or the Display PCA is causing the problem. A correct display depends on the E clock signal. Missing segments, intensified digits, a strobing display, or a blank display can be caused by a faulty E clock.

Use an oscilloscope to check for the E clock at Microprocessor A1U4, pin 68. Look for a 1.2288-MHz square wave that transitions from 0 to 5V dc (VCC).

- If this signal is present, the Display PCA is probably faulty. Refer to Display Assembly Troubleshooting elsewhere in this section.
- If the E clock is something other than a 1.2288-MHz square wave, isolate the digital section of the Main PCA by disconnecting the Display PCA at J2. Then check the E clock again, and refer to Digital Troubleshooting elsewhere in this section for further problem isolation.

Refer to the Schematic Diagrams in Section 8 during the following troubleshooting instructions. Also, these diagrams are useful in troubleshooting circuits not specifically covered here.

POWER SUPPLY TROUBLESHOOTING 5-5.

WARNING

TO AVOID ELECTRIC SHOCK, DISCONNECT ALL CHANNEL INPUTS FROM THE INSTRUMENT BEFORE PERFORMING ANY TROUBLESHOOTING OPERATIONS.

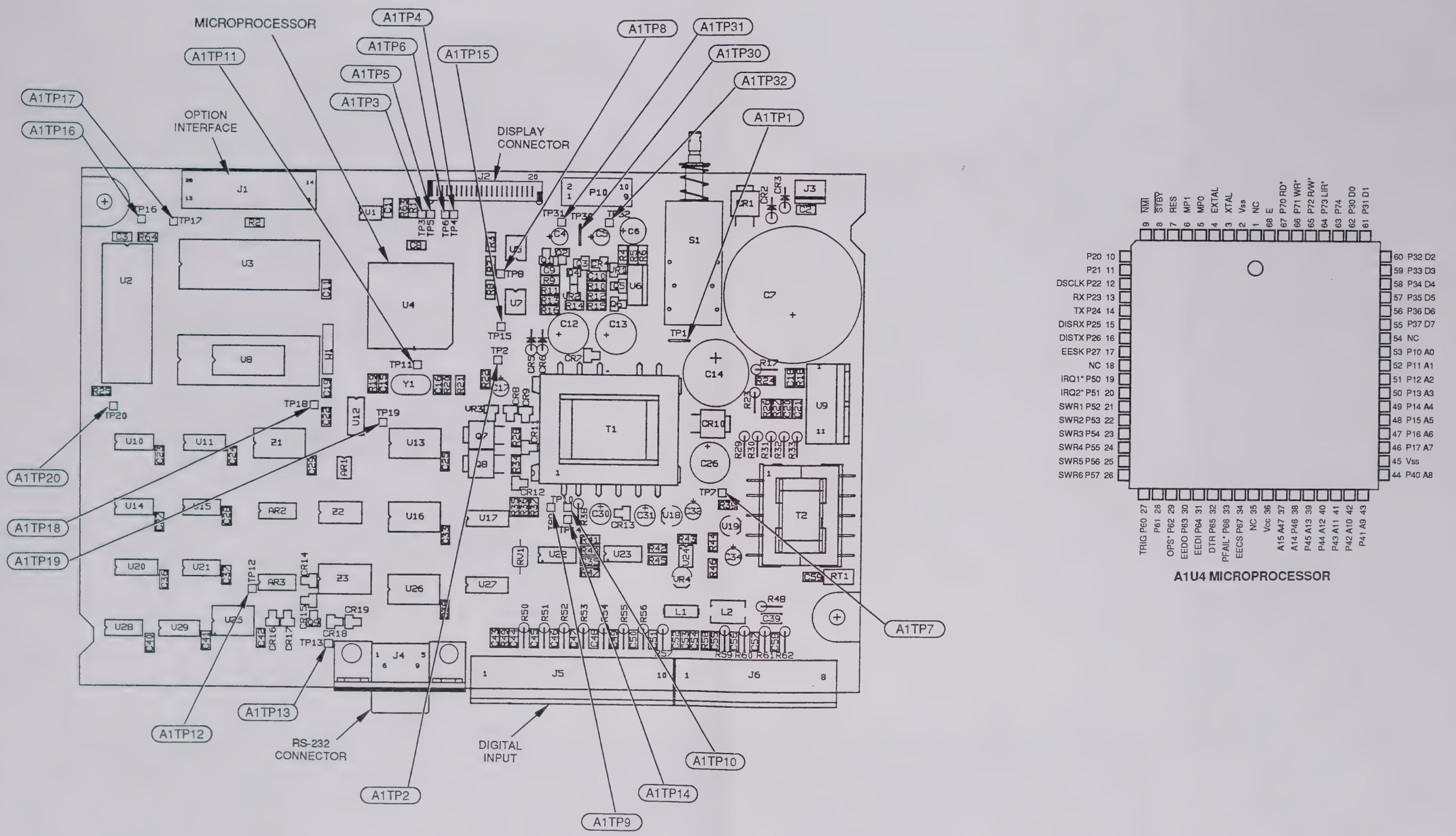

MICROPROCESSOR
A1TP4
A1TP6
A1TP5
A1TP3
A1TP11
A1TP15
A1TP8
A1TP31
A1TP30
A1TP32
A1TP1
A1TP17
A1TP16
OPTION INTERFACE
DISPLAY CONNECTOR
A1TP20
A1TP18
A1TP19
A1TP12
A1TP13
RS-232 CONNECTOR
DIGITAL INPUT
A1TP2
A1TP9
A1TP14
A1TP10
A1TP7
J1
J2
J3
J4
J5
J6
U2
U3
U4
U8
T1
T2
S1
C7
C14
Y1
P10
9 NMI
8 STBY
7 RES
6 MP1
5 MP0
4 EXTAL
3 XTAL
2 Vss
1 NC
68 E
67 P70 RD*
66 P71 WR*
65 P72 R/W*
64 P73 LIR*
63 P74
62 P30 D0
61 P31 D1
P20 10
P21 11
DSCLK P22 12
RX P23 13
TX P24 14
DISRX P25 15
DISTX P26 16
EESK P27 17
NC 18
IRQ1* P50 19
IRQ2* P51 20
SWR1 P52 21
SWR2 P53 22
SWR3 P54 23
SWR4 P55 24
SWR5 P56 25
SWR6 P57 26
60 P32 D2
59 P33 D3
58 P34 D4
57 P35 D5
56 P36 D6
55 P37 D7
54 NC
53 P10 A0
52 P11 A1
51 P12 A2
50 P13 A3
49 P14 A4
48 P15 A5
47 P16 A6
46 P17 A7
45 Vss
44 P40 A8
TRIG P60 27
P61 28
OPS* P62 29
EEDO P63 30
EEDI P64 31
DTR P65 32
PFAIL* P66 33
EECS P67 34
NC 35
Vcc 36
A15 A47 37
A14 P46 38
P45 A13 39
P44 A12 40
P43 A11 41
P42 A10 42
P41 A9 43
A1U4 MICROPROCESSOR

Figure 5-1. Test Point Locator, Main PCA (A1)

Table 5-2. Preregulated Power Supplies

PREREGULATED VOLTAGE	MEASUREMENT POINTS	RESULTING SUPPLY
-9.0V	A1CR13-2 to A1TP1	VEE
-30V	A1TP4 to A1TP1	VLOAD
+9.25V	A1CR5 cathode to A1TP30	VDD, VDDR
-8.75V	A1CR7 anode and A1TP30	VSS

Raw DC Supply 5-6.

With the instrument connected to line power (120V ac, 60 Hz) and turned ON, check for approximately 14V dc between A1TP1 (GND) and the "+" terminal of capacitor A1C7 (or the cathode of either A1CR2 or A1CR3). (This voltage is approximately 30V dc at 240V ac line.) If no voltage or a very low voltage is present, check for approximately 24V ac across the secondary of the power transformer (or approximately 50V ac at 240V ac line.)

The voltage at the output of A1U19 (also A1TP7), should be about +5.2V dc. At 120V ac, 60-Hz line power input, the line current is approximately 29 mA with the IEEE-488 Option installed or 20 mA without the IEEE-488 Option installed. At 50-Hz, 120V ac line power input, there is a 5-10% increase in these two current figures.

Power Fail Detection 5-7.

The Power Fail Detection circuit monitors the Raw Supply so that the Microprocessor can be signaled when power is failing. Check for approximately 1.23V dc between the inverting comparator input (A1U24-2) and GND (A1TP1). If the Raw Supply voltage is higher than approximately +8.3V dc, comparator output (A1U24-1) should be near VCC. If the comparator output is near 0V dc during normal operation, the Microprocessor will sense that power is failing and will not be able to complete a scan operation.

5-Volt Switching Supply 5-8.

Use an oscilloscope to troubleshoot the 5-volt switching supply. With the oscilloscope common connected to A1TP1, check the waveform at either A1U9, pin 7 (switch transistor collector) or A1T1, pin 2 to determine the loading on the 5-volt switching supply. The output voltage of the 5-volt switching supply at A1TP2 (VCC) is normally about 5.1V dc with respect to A1TP1 (GND). Note that a fault in the load (high or low resistance) can appear as a faulty output voltage of the 5-volt switching supply.

- Normal Load:

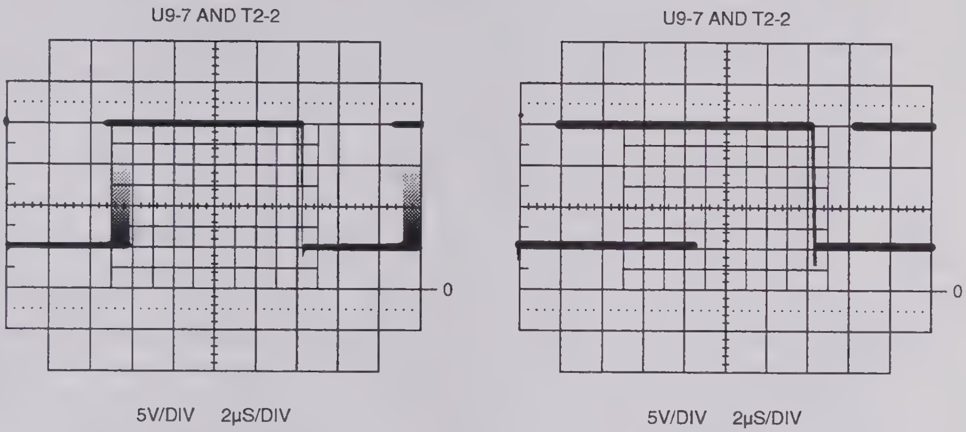
  The signal at A1U9-7 (with respect to A1TP1) is a square wave with a period of 13 μs to 15 μs and an ON (voltage is low) duty ratio of about 0.38 with the line voltage at 120V ac. The amplitude is usually about 15V p-p. The positive-going edge will be "fuzzy" as the duty ratio is varying to compensate for the ripple of the raw supply and the pulsing load of the inverter supply. See Figure 5-2 (NORMAL LOAD).

- Very Light Load or No Load:

  The 5-volt switching supply has a damped ringing sine wave of 1 to 5 cycles during the OFF interval (voltage is high). See Figure 5-2 (VERY LIGHT LOAD).

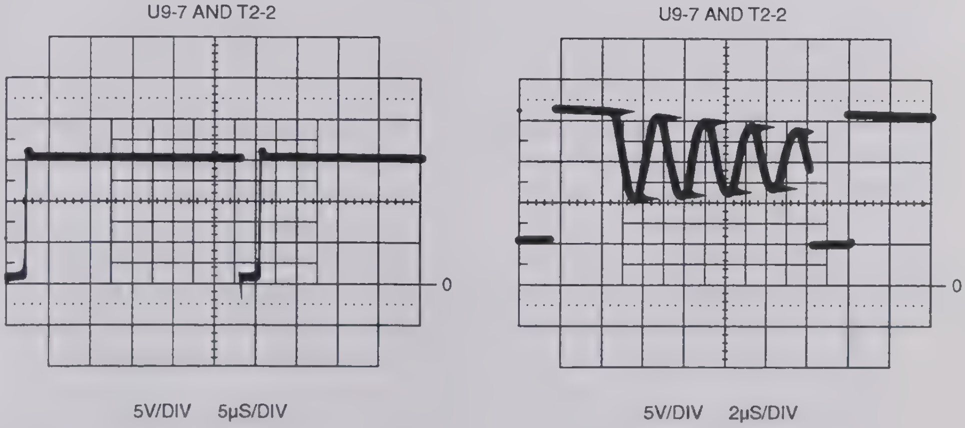
- Very Heavy Load or 5V Supply Shorted:

  The 5-volt switching supply goes into current limit and the duty cycle is low (near 0.1). In some cases, the period may increase to approximately 28 μs and the duty cycle will be around 0.1. For troubleshooting purposes, the inverter supply can be disconnected from the switcher by removing A1R38. See Figure 5-2 (VERY HEAVY LOAD or 5V SUPPLY SHORTED).



NORMAL LOAD

VERY HEAVY LOAD



5V SUPPLY SHORTED

VERY LIGHT LOAD

Figure 5-2. 5-Volt Switching Supply

If no square wave is present at A1U9-7, the oscillator can be checked by looking at the signal at A1U9-3. The oscilloscope should be ac-coupled for this measurement. This waveform should be a sawtooth signal with an amplitude of 0.6V p-p and a period of approximately 14 µs. Failure of the oscillator is usually caused by a defective capacitor A1C21 or defective A1U9.

The output current of the 5-volt switching supply can be determined by measuring the voltage across the current limit current sense resistors (A1R29, A1R30 and A1R31). The current shunt is approximately 0.167 ohms. With line voltage at 120V ac and the instrument not actively measuring, typical voltages across the current sense resistors are as follows:

- 2620A Instrument without options: 28 mV
- 2620A Instrument with IEEE-488 Option: 50 mV
- 2625A Instrument: 28 mV

Inverter 5-9.

Use an oscilloscope to troubleshoot the inverter supply. The outputs of the inverter supply are -5V dc, -30V dc, and 5.4V ac outguard, and +5.3V dc, -5.4V dc, and +5.6V dc inguard. Refer to Figure 5-3. The signal at the drains of the two inverter switch FETs (A1Q7 and A1Q8) should be a 10V peak square wave with a period of approximately 18 µs. The gate signal is a 5.1V peak square wave with rounded leading and trailing edges. The leading edge has a small positive rounded pulse with an amplitude of 1.8V peak and a pulse width of about 0.3 µs. The signal at A1U22-5 and A1U22-6 is a symmetrical square wave with an amplitude of 5.1V peak and a period of about 18 µs. The negative-going trailing edge of both square waves is slower than the rising edge and has a small bump at about 1.5 volts. The signal at A1U22-3 (TP14) is a symmetrical square wave with a period of about 9 µs.

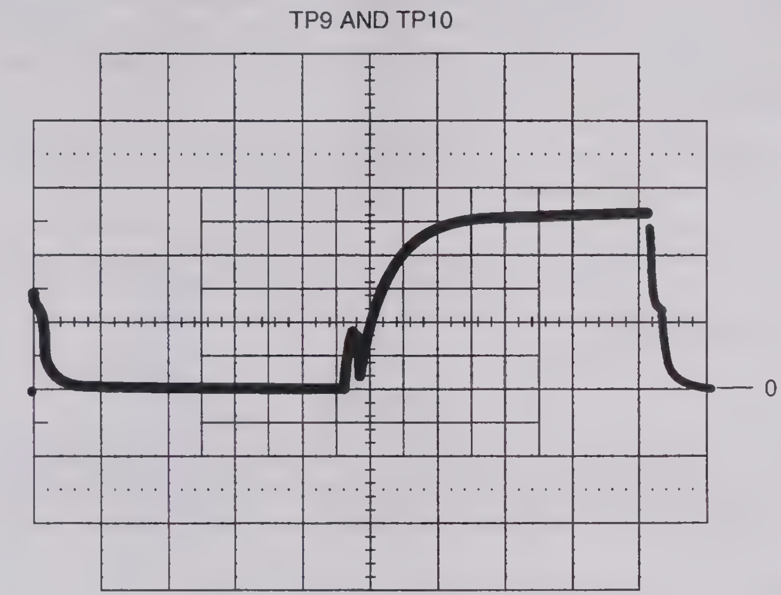
For the inverter to operate, the 110-kHz oscillator must be operating properly. If the signal at A1U22-3 is missing, begin by checking the voltage at A1TP7. The voltage should be about 5.1V dc. Then, using an oscilloscope, check for a square wave signal at A1U23-9 and a square wave signal at A1U23-8. If the FETs are getting proper drive signals, failures that heavily load the inverter supply will usually cause the inverter to draw enough current to make the switcher supply go into current limit. Shorted rectifier diodes and shorted electrolytic capacitors will cause heavy load conditions for the inverter.

NOTE

When making voltage measurements in the inverter circuit, remember that there are two separate grounds. The outguard ground is the 'GND' test point (A1TP1), and the inguard ground is the 'COM' test point (A1TP30).

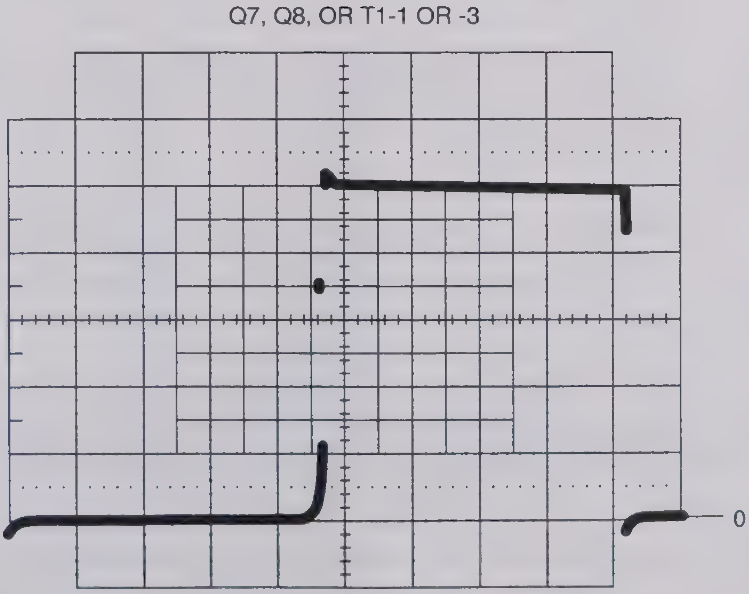
The inguard regulator circuits for VDD and VSS have current limits. Shorts and heavy loads between VDD and COM, VSS and COM, and VDD and VSS will cause one or both supplies to go into current limit. The current supplied by either supply can be checked by measuring the voltage across the current sense resistors, A1R13 and A1R15. The typical voltage across A1R13 is 0.30 and the typical voltage across A1R15 is 0.40V.

Generally, open electrolytic capacitors in the inverter supply will cause excessive ripple for the affected supply. Also, the rectified dc voltage for the supply with the open capacitor will be lower than normal. Normal voltage levels at the rectifier outputs for each inverter supply are shown in Table 5-2.


TP9 AND TP10

2V/DIV 2µS/DIV

FET GATE SIGNAL


Q7, Q8, OR T1-1 OR -3

2V/DIV 2µS/DIV

FET DRAIN SIGNAL

Figure 5-3. Inverter FET Drive Signals

The loads for the inguard supplies can be disconnected by removing the cable to the A/D Converter PCA at A3J10. The inguard regulator circuits and VDDR regulator will operate with no loads, and troubleshooting can be performed by making voltage measurements.

The normal input current to the inverter supply is about 11.25 mA, or 0.225 mV across A1R38 (when the instrument is not measuring).

Table 5-3 provides a Power Supply troubleshooting guide.

ANALOG TROUBLESHOOTING 5-10.

WARNING

TO AVOID ELECTRIC SHOCK, DISCONNECT ALL CHANNEL INPUTS FROM THE INSTRUMENT BEFORE PERFORMING ANY TROUBLESHOOTING OPERATIONS.

Refer to Figure 5-4 and Figure 5-5 for test point locations on the A/D Converter PCA.

First, check for analog-related errors displayed at power up. An ‘Error 9’ means that the Main Microprocessor A1U4 is not able to communicate with the A/D Microcontroller A3U9. ‘Error A’ and ‘Error b’ mean that a failure has occurred in the internal memory of the A/D Microcontroller A3U9. ‘Error C’ means that the Analog Measurement Processor A3U8 is not functioning properly.

Check the inguard power supplies on the Main PCA with and without the A/D Converter PCA connected. The inguard supplies must be measured with respect to COM testpoint A1TP30.

POWER SUPPLY	TEST LOCATION	ACCEPTABLE RANGE
VDD	A1TP31	5.00 to 5.70V dc
VSS	A1TP32	-5.10 to -5.75V dc
VDDR	A1C6+	5.30 to 5.95V dc

Check the inguard supply voltages on the A/D Converter PCA with respect to A3TP9. The following table lists the components nearest the power supply test points.

POWER SUPPLY	NEAREST COMPONENT	ACCEPTABLE RANGE
VDD	A3C8	5.00 to 5.70V dc
VSS	A3C9	-5.10 to -5.75V dc
VDDR	A3C19	5.30 to 5.95V dc
+VAC	A3CR1	4.7 to 5.7V dc
-VAC	A3C26	-4.8 to -5.7V dc

Table 5-3. Power Supply Troubleshooting Guide

SYMPTOM	FAULT
Line fuse blows.	- Shorted A1CR2 or A1CR3. - Shorted A1CR10. - Shorted A1C7. - Shorted A1C26.
Supply voltage for A1U23 and A1U22 is greater than 7V (7 to 30V).	Input-to-output short of A1U19. This fault may have caused damage to A1Q7 and A1Q8.
VCC (5.1V) supply is at the raw supply level (7.5 to 35V dc).	Shorted switch transistor in A1U9 (A1U9-5 to 7). Open A1C26 can cause switch transistor to short.
VCC (5.1V) supply shows excessive ripple (about 1V p-p).	A1C14 open.
VCC is below approximately 4.5V. Duty cycle of 5V switcher supply is very low (ON time near 0.1).	Drain-to-source short of A1Q7 or A1Q8.
VCC is about 1.5V. 5V switcher supply is in current limit.	Shorted A1CR5 or A1CR6.
VCC is below approximately 1V. 5V switcher supply is in current limit, with very low duty cycle (ON time near 0.1).	Shorted A1C14.
VCC is below approximately 4.5V. 5V switcher supply is in current limit, with very low duty cycle (ON time near 0.1).	- Q or Q* output of A1U22 stuck high. - A1U23 pin 8 output stuck high or low. - Shorted A1CR7. - Shorted A1CR9 (either diode), pins 1-3 or 2-3. - Shorted A1C30. A1CR13 may also be damaged. - Shorted A1C31. A1CR13 may also be damaged. - Shorted A1C12. - Shorted A1C13. - Shorted A1CR8 (either diode), pins 1-3 or 2-3.
VLOAD (-30V dc) Inverter Supply is at -36V.	Q output of A1U22 stuck low.
VLOAD (-30V dc) Inverter Supply is OFF.	Q* output of A1U22 stuck low.
VLOAD (-30V dc) Inverter Supply ripple.	- Open A1CR8 (either diode). - Open A1CR9 (either diode).
VDD (5.3V dc) supply at approximately 9.2V.	Emitter-to-collector short of A1Q2.
VSS (-5.4V dc) supply at approximately -9.2V.	Emitter-to-collector short of A1Q5.

Table 5-3. Power Supply Troubleshooting Guide (cont)

SYMPTOM	FAULT
VDDR (5.6V dc) supply at approximately 10V.	Input-to-output short of A1U6.
VDDR supply has 4-to-5 volt spikes when the A/D relays are switched (set or reset).	Open A1C12.
VEE (-5V dc) supply is low (near zero).	- Open A1C30. - A1CR13 open.
A1CR13, Diode 1-3 shorted or open.	A1C30 may be shorted.
VEE supply is high (near -9V).	Input-to-Output short of A1U18.
A1U18 input has large square wave component.	Open A1C31.
A1U18 hot.	Shorted A1C32.
A1U18 oscillates.	Open A1C32.
A1U19 oscillates.	Open A1C34.
A1U19 very hot.	- Shorted A1U22 (VCC to VSS). - Shorted A1U23 (VCC to VSS).
A1U19 hot.	Shorted A1C34.

Check that the inguard Microcontroller A3U9 RESET* line is de-asserted. Check VDD at A3TP1, referenced to A3TP9.

Check that the microcontroller crystal oscillator is running. When measured with a high input impedance oscilloscope or timer/counter, the oscillator output at A3TP10 should be a 3.6864-MHz sine wave (271.3 ns period), and the divided-down E clock output at A3U9 pin 68 should be a 921.6 kHz-square wave (1.085 μs period).

Check outguard to inguard communication. Setup an input channel and enable monitor measurements on that channel, causing the outguard to transmit to the inguard approximately every 10 seconds.

On the Main PCA, look for outguard-to-inguard communication (5.1V (VCC) to near 0V pulses) at A1TP15, referenced to A1TP1. On the A/D Converter PCA, check for 5.35V (VDD) to near 0V pulses at A3TP8, referenced to A3TP9.

At the start of outguard-to-inguard communication, the A/D Microcontroller (A3U9) should be RESET. Check for this reset pulse (5.35V (VDD) to near 0V, lasting approximately 1-ms) on A3TP1 with respect to A3TP9.

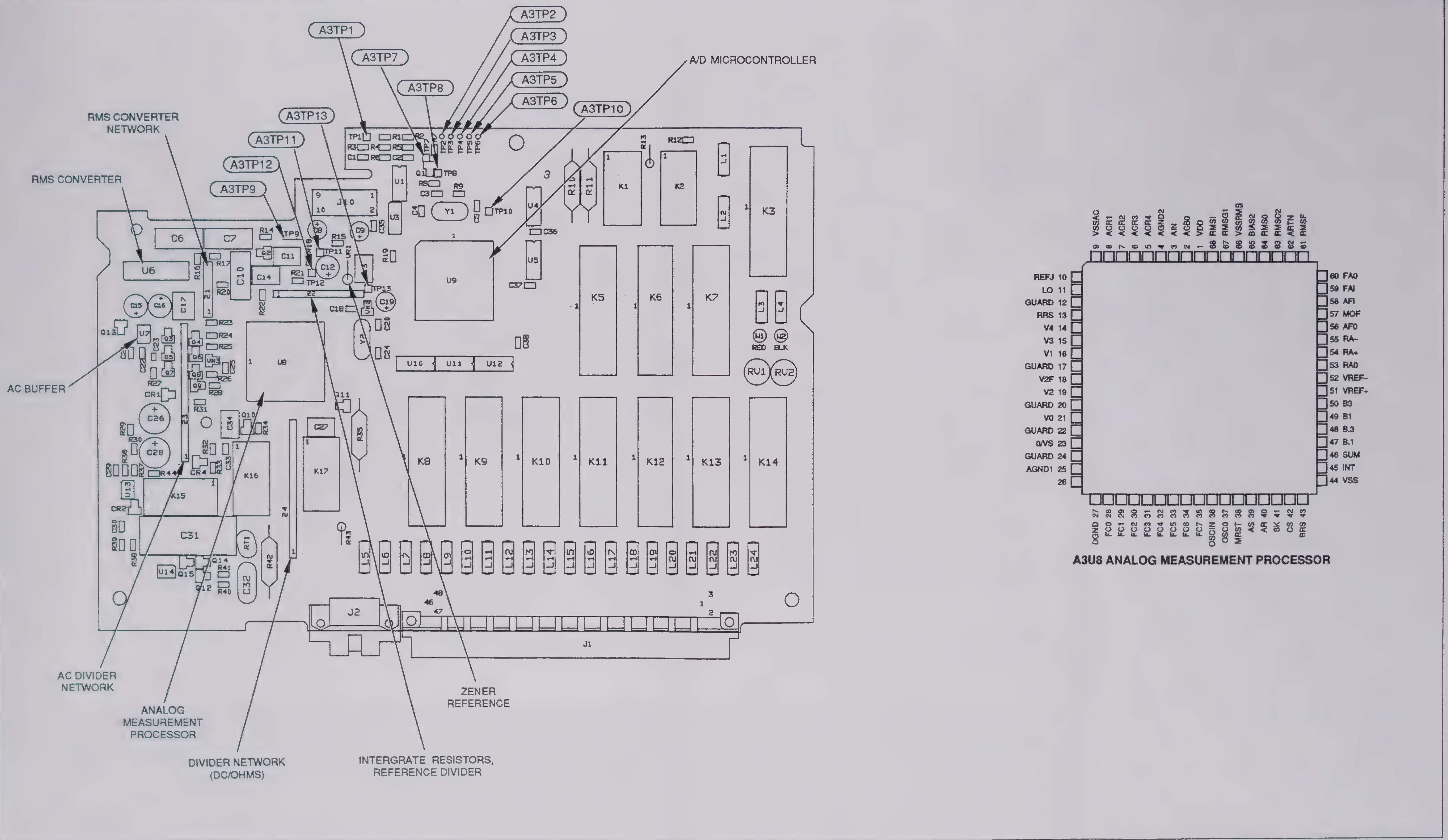

A3TP1
A3TP2
A3TP3
A3TP4
A3TP5
A3TP6
A3TP7
A3TP8
A3TP9
A3TP10
A3TP11
A3TP12
A3TP13
A/D MICROCONTROLLER
RMS CONVERTER NETWORK
RMS CONVERTER
AC BUFFER
AC DIVIDER NETWORK
ANALOG MEASUREMENT PROCESSOR
DIVIDER NETWORK (DC/OHMS)
INTERGRATE RESISTORS, REFERENCE DIVIDER
ZENER REFERENCE
U6
U8
U9
K1
K2
K3
K5
K6
K7
K8
K9
K10
K11
K12
K13
K14
K15
K16
K17
J1
J2
J10
RV1
RV2
RED
BLK
9 VSSAC
8 ACR1
7 ACR2
6 ACR3
5 ACR4
4 AGND2
3 AIN
2 ACB0
1 VDD
68 RMSI
67 RMSG1
66 VSSRMS
65 BIAS2
64 RMS0
63 RMSC2
62 ARTN
61 RMSF
REFJ 10
LO 11
GUARD 12
RRS 13
V4 14
V3 15
V1 16
GUARD 17
V2F 18
V2 19
GUARD 20
V0 21
GUARD 22
0/VS 23
GUARD 24
AGND1 25
26
60 FA0
59 FAI
58 AFI
57 MOF
56 AF0
55 RA-
54 RA+
53 RA0
52 VREF-
51 VREF+
50 B3
49 B1
48 B.3
47 B.1
46 SUM
45 INT
44 VSS
DGND 27
FC0 28
FC1 29
FC2 30
FC3 31
FC4 32
FC5 33
FC6 34
FC7 35
OSCIN 36
OSC0 37
MRST 38
AS 39
AR 40
SK 41
CS 42
BRS 43
A3U8 ANALOG MEASUREMENT PROCESSOR

Figure 5-4. Test Points, A/D Converter PCA (A3, A3U8)

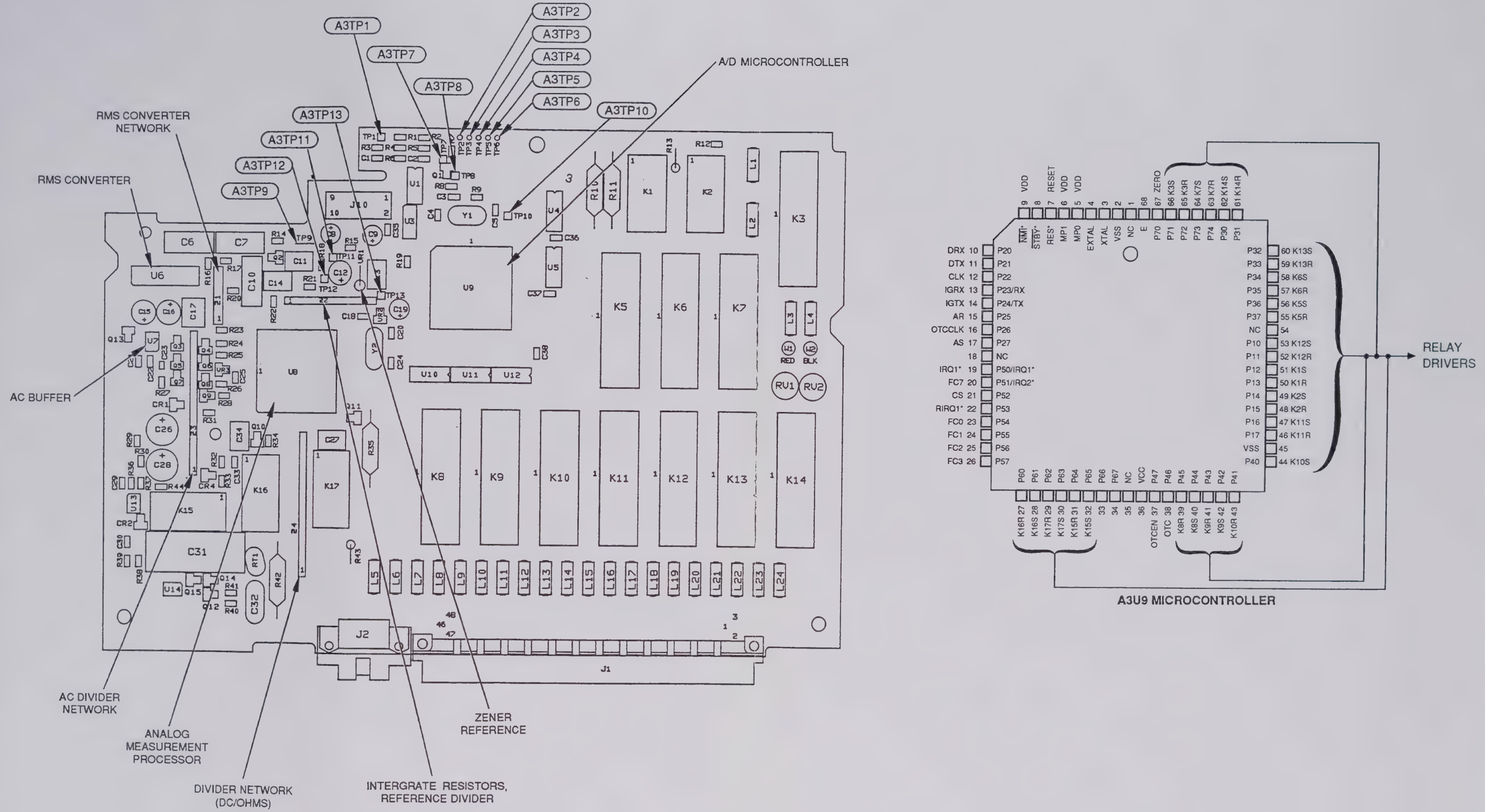

A3TP1
A3TP7
A3TP8
A3TP2
A3TP3
A3TP4
A3TP5
A3TP6
A3TP10
A3TP13
A3TP11
A3TP12
A3TP9
A/D MICROCONTROLLER
RMS CONVERTER NETWORK
RMS CONVERTER
AC BUFFER
AC DIVIDER NETWORK
ANALOG MEASUREMENT PROCESSOR
DIVIDER NETWORK (DC/OHMS)
INTERGRATE RESISTORS, REFERENCE DIVIDER
ZENER REFERENCE
U9
U8
J1
J2
K1
K2
K3
K5
K6
K7
K8
K9
K10
K11
K12
K13
K14
K15
K16
K17
A3U9 MICROCONTROLLER
RELAY DRIVERS
DRX 10 P20
DTX 11 P21
CLK 12 P22
IGRX 13 P23/RX
IGTX 14 P24/TX
AR 15 P25
OTCCLK 16 P26
AS 17 P27
18 NC
IRQ1* 19 P50/IRQ1*
FC7 20 P51/IRQ2*
CS 21 P52
RIRQ1* 22 P53
FC0 23 P54
FC1 24 P55
FC2 25 P56
FC3 26 P57
9 VDD NMI*
8 STBY*
7 RESET RES*
6 VDD MP1
5 VDD MP0
4 EXTAL
3 XTAL
2 VSS
1 NC
68 E
67 ZERO P70
66 K3S P71
65 K3R P72
64 K7S P73
63 K7R P74
62 K14S P30
61 K14R P31
P32 60 K13S
P33 59 K13R
P34 58 K6S
P35 57 K6R
P36 56 K5S
P37 55 K5R
NC 54
P10 53 K12S
P11 52 K12R
P12 51 K1S
P13 50 K1R
P14 49 K2S
P15 48 K2R
P16 47 K11S
P17 46 K11R
VSS 45
P40 44 K10S
P60 K16R 27
P61 K16S 28
P62 K17R 29
P63 K17S 30
P64 K15R 31
P65 K15S 32
P66 33
P67 34
NC 35
VCC 36
P47 OTCEN 37
P46 OTC 38
P45 K8R 39
P44 K8S 40
P43 K9R 41
P42 K9S 42
P41 K10R 43

Figure 5-5. Test Points, A/D Converter PCA (A3, A3U9)

Check for the following inguard-to-outguard communication activity:

PCA	TEST POINT	TO	PULSES
A/D Converter	A3TP7	A3TP9	5.55V (VDDR) to 0.7V
Main	A1TP8	A1TP1	0V dc to 5.1V (VCC)

Lack of outguard-to-inguard communication activity may be due to improper operation of circuit elements other than A3U9. Using a high input impedance oscilloscope or timer/counter, check for proper Analog Processor (A3U8) crystal oscillator operation. A 3.84-MHz sine wave (260 ns period) should be present at A3U8 pin 37 with respect to A3TP9.

Check the A/D Converter voltage reference:

A3TP12 to A3TP11 (across A3C12) = +1.05V (+0.10V, -0.02V)

Setup the instrument to measure ohms on the 300Ω range. Monitor ohms on a channel with an input of approximately 270Ω. Check that the Analog Processor IC (A3U8) is making A/D conversions. The integrator output waveform at A3TP13 (referenced to A3TP9) should resemble the waveform shown in Figure 5-6.

Check for channel relay operation by setting up a channel and selecting and de-selecting monitor measurement mode. One or more relays should click each time the monitor button is pressed or channels are changed.

In general, check that the relays are getting the proper drive pulse signals for specific functions and channels and that they are in the correct position.

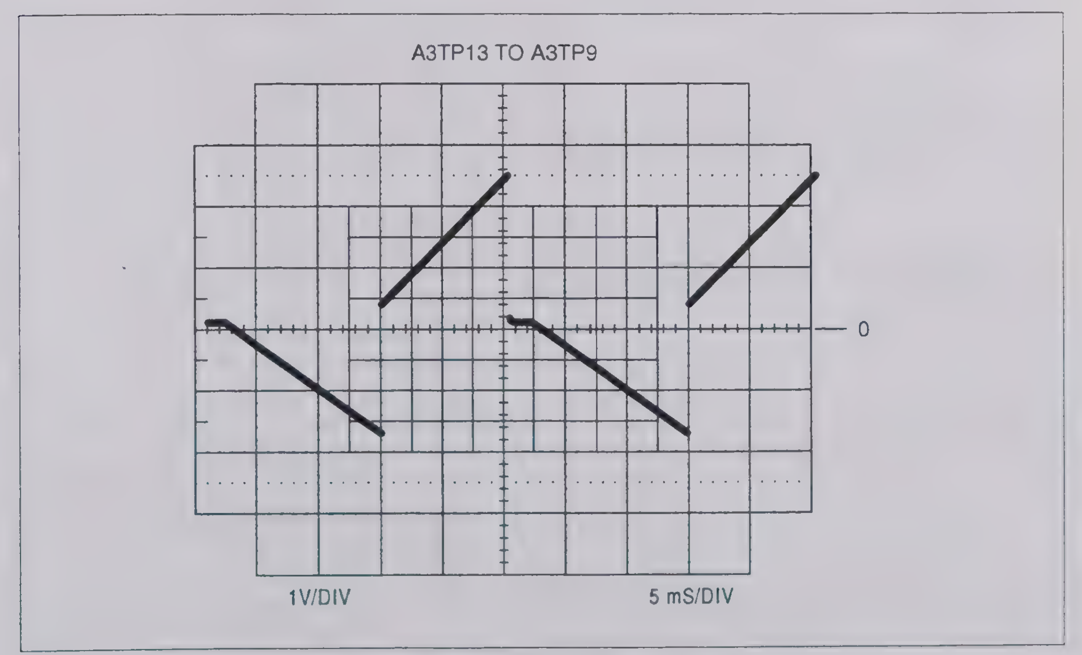


Figure 5-6. Integrator Output

DC Volts Troubleshooting 5-11.

Setup the instrument to measure a specific channel on the 300 mV or 3V range, and apply an input to that channel. Then trace the HI signal (referenced to the input channel LO terminal) as described in Table 5-4.

If the input HI path traces out properly, remove the input from the channel and trace continuity through the LO path. Check among A3L4-A3L24, A3K1-A3K14, A3R35, A3R43, and A3U8 pin 11.

AC Volts Troubleshooting 5-12.

Setup the instrument to measure a channel on the 300 mV ac range, and apply a signal to that channel. Then trace this HI signal (referenced to the input channel LO terminal) as described in Table 5-5.

If the input HI path traces out properly, remove the input from the channel, and trace continuity through the LO path. Check among A3L4 through A3L24, A3K1 through A3K14, A3R43, A3R34, A3K16, and A3U8 pin 13.

Ohms Troubleshooting 5-13.

Setup a channel with an open input for the desired ohms range and place the instrument in monitor mode on that channel. Use a meter with high input impedance to measure the open-circuit voltage at the channel input for the ohms range as listed in Table 5-6. If a high input impedance meter is not available, only the 30-kΩ and lower ranges can be checked.

Table 5-4. DC Volts HI Troubleshooting

CHECKPOINT	SIGNAL DESCRIPTION	POSSIBLE FAULT
A3R11 HI	Input	A3K1 through A3K14, A3U4, A3U5, A3U11, A3U12, A3L1, A3L2, A3L3
A3U8 pin 23	Input	A3R11, A3K17, A3R42, A3C32
A3U8 pin 58	Input, DC filter output	A3U8, A3Q2

Table 5-5. AC Volts HI Troubleshooting

CHECKPOINT	SIGNAL DESCRIPTION	POSSIBLE FAULT
A3R11 HI	Input	A3K1 through A3K14, A3U4, A3U5, A3U11, A3U12 A3L1, A3L2, A3L3
A3Z3 pin 1	Input	A3R11, A3C31, A3K15
A3U6 pin 13	Amplified (X 2.5) input	A3U7, A3Z3, A3Q3 through A3Q9, A3C15, A3C16, A3R24, A3A25, A3R26, A3R27, A3R28, A3C23, A3U6, A3Q13, A3U8
A3Z1 pin 2	DC equivalent of amplified input	A3U6, A3C17
A3U8 pin 61	DC equivalent of original input	A3Z1, A3U8, A3R20, A3C6, A3C7, A3C10, A3R16, A3R17

Table 5-6. Ohms Open-Circuit Voltages

RANGE	VOLTAGE
300Ω	3V
3 kΩ	1.3V
30 kΩ	1.3V
300 kΩ	3V
3 MΩ	3V
10 MΩ	3V

If the proper voltage is not measured, setup a channel on the 300Ω range (open input), and have the instrument monitor that channel. Check for 3V dc with respect to A3TP9, and work through the HI SOURCE and HI SENSE paths as described in Table 5-7.

If the HI path works correctly, trace continuity through the LO path. Check among A3L4 through A3L24, A3K1 through A3K14, A3R35, A3U8 pin 11, A3R43, A3K16, A3R34, and A3U8 pin 13.

DIGITAL KERNEL TROUBLESHOOTING 5-14.

At power-up, if the display does not light or lights up and fails to report errors or begin operation, use the following troubleshooting procedures.

First check the state of SWR1 (A1U4-21). If this status line is less than 0.8V, basic processor operation is intact. Examining SWR2 through SWR5 (A1U4-22 through -25, respectively) should indicate how far the software progressed before finding an error. If the state of SWR1 is not less than 0.8V, the problem may be in the 6303Y Microprocessor (A1U4), the ROM or NVRAM decode circuitry (A1U10 and A1U21), the ROM (A1U8) or NVRAM (A1U3), or the address/data lines among these parts.

NOTE

The functions of SWR1 through SWR5 as power-up status lines persist for only 3 to 4 seconds. These functions end when the keyboard scanner begins operation (if it can). Extremely difficult cases may require the use of an oscilloscope triggered on the falling edge of SWR1 to examine the states of SWR2 through SWR5.

To determine the relative health of the 6303Y Microprocessor (A1U4), first check for a valid E clock at pin 68. The default for the E clock after reset is a rectangular wave with a period of 1.221 µs and a duty cycle of about 67%.

Table 5-7. Ohms HI Troubleshooting

CHECKPOINT	SIGNAL DESCRIPTION	POSSIBLE FAULT
A3U8 pin 14	Ohms Source	A3U8
A3R10 HI SRC	Ohms Source	A3R10, A3K16, A3RT1, A3Z4, A3Q10
Channel HI	Ohms Source	A3K1 through A3K14, A3U4, A3U5, A3U11, A3U12, A3L1, A3L2, A3L3
A3U8 pin 23	Ohms Source	A3R11, A3K17, A3R42, A3C32
A3U8 pin 58	Ohms source, filter output	A3U8, A3Q2

If the processor is able to fetch instructions from the ROM, the software initializes the processor, and the E clock becomes a square wave with a period of 0.814 µs. Since this initialization occurs almost immediately with a working instrument, the resulting square wave on the E clock line is a good indication that the software has begun to execute.

If the E clock remains a 1.221 µs rectangular wave, the SWR2 (A1U4-22) keyboard scan line might be shorted to ground. This condition would cause the Microprocessor to HALT after reset. Check whether the 6303Y Microprocessor is attempting to access ROM; LIR* (A1U4-64) should transition for a short period of time after reset. If it does, the 6303Y Microprocessor is probably operational, and the problem is external to the processor.

The processor can execute an instruction that stops both itself and the E clock. Therefore, the absence of any activity on pin 68 does not necessarily mean that A1U4 or A1Y1 is bad. If some other failure prevents proper ROM access, the processor may have just "gone to sleep". This can be verified by checking for a rectangular wave occurring at pin 68 for a short time after RESET* transitions high on pin 7. A1U4 and A1Y1 are probably operational if this rectangular wave is at least momentarily present.

To check the ROM decode circuitry, verify that A1U10-6 is transitioning low and that these transitions correspond roughly to the low-going transitions of LIR*. Pin 6 must be low when LIR* is low. Verify that this signal also appears at the ROM Chip Enable, A1U8-20. If the ROM Chip Enable is present, the problem is with the ROM itself or there is a fault in the address/data lines among the 6303Y Microprocessor, ROM, NVRAM, and Option Connector.

If SWR1 (A1U4-21) and SWR2 (A1U4-22) transition low, but SWR3 (A1U4-23) remains high, the problem is with the NVRAM decode circuitry (A1U15, A1U21), the external NVRAM (A1U3), or the address/data/control lines between the NVRAM and the 6303Y Microprocessor.

To check the NVRAM decode circuitry, verify that A1U21-6 is transitioning low and that these transitions correspond approximately to the low-going transitions of WR* (A1U4-66). It may be necessary to continually reset (power on) the instrument to check these lines, since the activity probably halts quickly when the instrument software goes awry. Verify that the signal on A1U21-6 also appears at the NVRAM Chip Enable, A1U3-20. If the NVRAM Chip Enable is present, the problem is with either the NVRAM itself or the address, data, RD*, or WR* lines between the 6303Y Microprocessor and the external NVRAM.

Figure 5-7 shows the timing relationships of the 6303Y Microprocessor lines LIR* and WR* to the system clock (E) and the address lines A0..A15. The ROM and NVRAM Chip Enables correspond to the active (low) region shown for the address lines.

If the instrument powers up without any errors, but does not recognize front-panel button presses or computer interface commands, the problem may be in the Counter/Timer (A1U2). Normally, this component generates a regular 50-millisecond interrupt at the IRQ* output (A1U2-9). If this output is low (and never goes high), the Microprocessor (A1U4) is failing to recognize the interrupt or the microprocessor interface to A1U2 is not working correctly. Also check output A1U2-6 for a 10-Hz square wave. If this output is not correct, check for the E clock at A1U2-17, and verify the microprocessor interface signals (CNTR*, D0 .. D7, A0 .. A2, R/W*, and RESET*.)

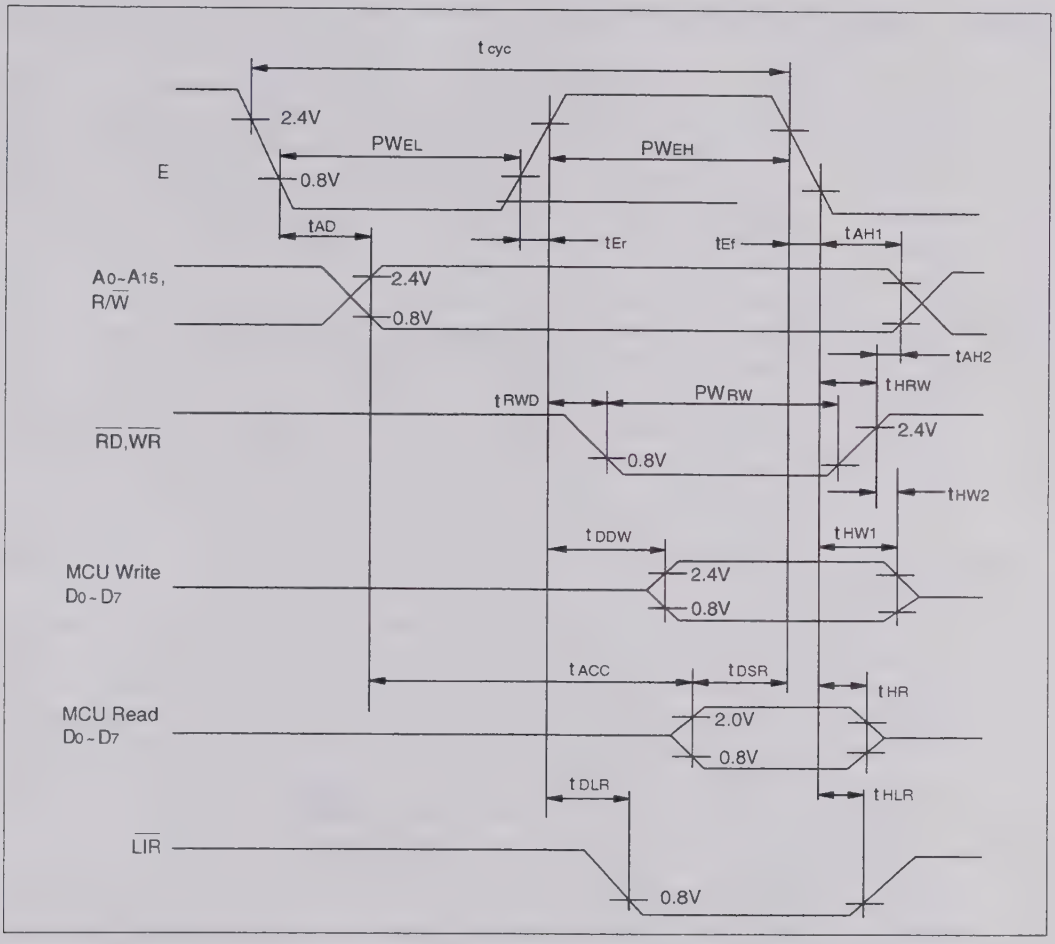

t cyc
2.4V
PWEL
E
0.8V
PWEH
tAD
tEr
tEf
tAH1
A0~A15,
R/W
2.4V
0.8V
tAH2
tHRW
tRWD
PWRW
RD,WR
2.4V
0.8V
tHW2
tDDW
tHW1
MCU Write
D0 ~ D7
2.4V
0.8V
tACC
tDSR
tHR
MCU Read
D0 ~ D7
2.0V
0.8V
tDLR
tHLR
LIR
0.8V

Figure 5-7. Microprocessor Timing

DIGITAL AND ALARM OUTPUT TROUBLESHOOTING 5-15.

Power up Hydra while holding down the CANCL button to reset the instrument configuration. Since the structure of the eight Digital Outputs and four Alarm Outputs is very similar, the troubleshooting procedure presented here does not refer to specific device and pin numbers. First verify that the input of the Output Driver (A1U17 or A1U27) is low and that the output is near +5V dc. If the input is high, the problem may be in the address decoding (A1U12 and A1U15) or the associated octal D-type flip-flop (A1U16 or A1U26). If the output is not near +5V dc, use an ohmmeter to check the pull-up resistor in A1Z2.

Use the proper computer interface command to change the state of the Digital Output (DO_LEVEL x,1) or Alarm Output (ALARM_DO_LEVEL x,1), where x is the number of the output being checked. Now verify that the input of the Output Driver is high and that the output is near +0.8V dc. If there is no change in the input, check the address decoding and operation of the associated octal D-type flip-flop (A1U16 or A1U26.) If the output failed to change, the problem is most likely the inverting output driver (A1U17 or A1U27).

DIGITAL INPUT TROUBLESHOOTING 5-16.

Power up Hydra while holding down the CANCL button to reset the instrument configuration. Verify that the Input Buffer Threshold circuit generates approximately 1.4V dc at A1TP18. Drive the Digital Input (A1J5) to be checked with a signal generator outputting a 100-Hz square wave that transitions from 0 to +5V dc. The signal generator output common should be connected to Common (A1J5-1). Verify that the output of the Input Buffer is a 100 Hz square wave that is the inverse of the input signal.

If the Input Buffer does not function correctly, the problem is probably A1Z1, A1Z3, or the associated comparator (A1AR2 or A1AR3). If the Input Buffer functions correctly, but Hydra is not able to read the state of the Digital Input correctly, the problem is most likely the tri-state buffer A1U13. If Hydra is not able to read the states of any of the eight Digital Inputs correctly, the problem is most likely the address decoding (A1U10 and A1U12) for the tri-state buffer.

TOTALIZER TROUBLESHOOTING 5-17.

Power up Hydra while holding down the CANCL button to reset the instrument configuration. Verify that the Input Buffer Threshold circuit generates approximately 1.4V dc at A1TP18. Drive the Totalizer Input (A1J5-2) with a signal generator outputting a 100-Hz square wave that transitions from 0 to +5V dc. The signal generator output common should be connected to Common (A1J5-1). Verify that the output of the Input Buffer (A1AR1-7) is a 100-Hz square wave that is the inverse of the input signal. Verify also that the input to the totalizer counter (A1TP20) is a buffered form of the signal just verified at the output of the Input Buffer.

Use the following procedure to troubleshoot the totalizer input debouncer, Enable the totalizer debouncer by sending the TOTAL_DBNC 1 Computer Interface command to the instrument; verify that A1U16-16 is now high. With the signal generator still connected and outputting a 100-Hz square wave, verify that A1U14 drives the clear input of the counter (A1U20-11) low for 1.67 milliseconds after each edge of the input signal. Verify that counter output A1U20-13 generates a 4.8-kHz clock while A1U20-11 is low. Verify that the shift register output (A1U29-9) changes to the same state as the totalizer input signal about 1.67 milliseconds after a transition occurs on the totalizer input signal (A1U29-10).

DISPLAY ASSEMBLY TROUBLESHOOTING 5-18.

The following discussion is helpful if it has been determined that the Display Assembly is faulty. Refer to Figure 5-8 for Display PCA test points. This initial determination may not be arrived at easily, since an improperly operating display may be the result of a hardware or software problem that is not a direct functional part of the Display Assembly. Consult the General Troubleshooting Procedures found earlier in this section for procedures to isolate the fault to the Display Assembly. Use the following discussion of display software operation when troubleshooting problems within a known faulty Display Assembly. A Display Extender Cable (PN 867952) is available for use during troubleshooting. Note that this cable must be twisted to mate correctly to the connectors on Display and Main PCAs.

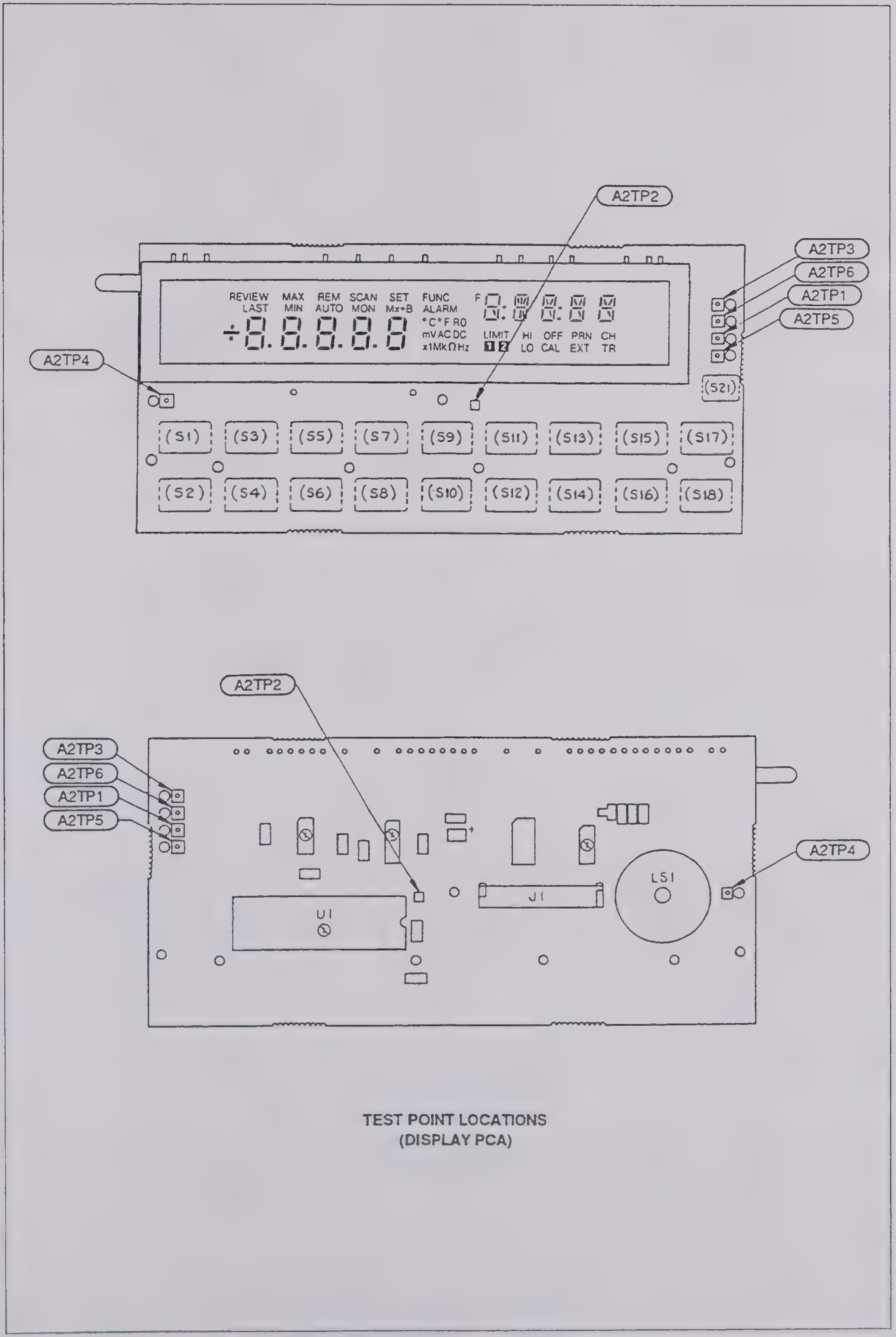

A2TP2
A2TP3
A2TP6
A2TP1
A2TP5
A2TP4
REVIEW LAST
MAX MIN
REM AUTO
SCAN MON
SET Mx+B
FUNC ALARM
°C°F RO
mVACDC
x1MkΩHz
LIMIT 1 2
HI LO
OFF CAL
PRN EXT
CH TR
(S1)
(S3)
(S5)
(S7)
(S9)
(S11)
(S13)
(S15)
(S17)
(S2)
(S4)
(S6)
(S8)
(S10)
(S12)
(S14)
(S16)
(S18)
(S21)
A2TP2
A2TP3
A2TP6
A2TP1
A2TP5
A2TP4
U1
J1
LS1
TEST POINT LOCATIONS
(DISPLAY PCA)

Figure 5-8. Test Points, Display PCA (A2)

The Display Controller reads the DTEST* and LTE* inputs to determine how to initialize the display memory. DTEST* and LTE* default to logic 1 and logic 0, respectively, to cause all display segments to be initialized to “on”. DTEST* is connected to test points A2TP4, and LTE* is connected to A2TP5. Either test point can be jumpered to VCC (A2TP6) or GND (A2TP3) to select other display initialization patterns. Display Test Patterns #1 and #2 are a mixture of “on” and “off” segments with a recognizable pattern to aid in troubleshooting problems involving individual display segments. When either of the special display patterns is selected, the beeper is also sounded for testing without interaction with the Microprocessor. Table 5-8 indicates the display initialization possibilities.

Figure 5-9 shows the timing of communications between the Microprocessor and the Display Controller. Figures 5-10 and 5-11 show Display Test Patterns #1 and #2, respectively. Refer to the Display Assembly schematic diagram in Section 8 for information on grid and anode assignments.

When a Hydra display is initially powered up, all display segments should come on automatically. If this display does not appear, proceed with the following steps:

Table 5-8. Display Initialization

A2TP4 DTEST*	A2TP5 LTE*	POWER-UP DISPLAY INITIALIZATION
1	1	All Segments OFF
1	0	All Segments ON (default)
0	1	Display Test Pattern #1
0	0	Display Test Pattern #2

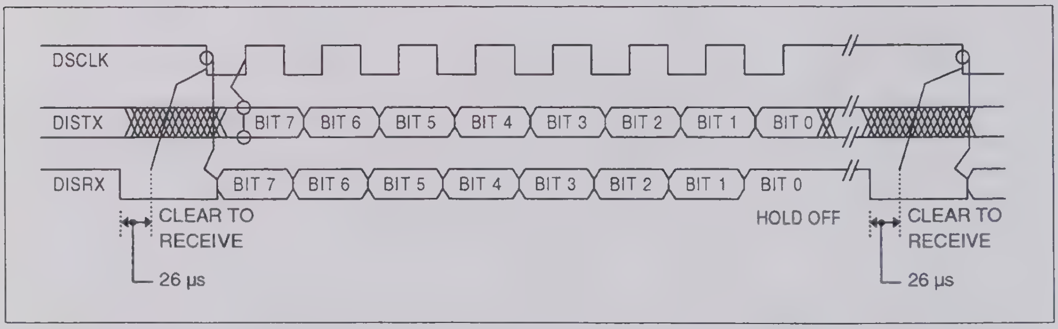

DSCLK
DISTX
DISRX
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
BIT 0
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
BIT 0
CLEAR TO RECEIVE
26 µs
HOLD OFF
CLEAR TO RECEIVE
26 µs

Figure 5-9. Display Controller to Microprocessor Signals

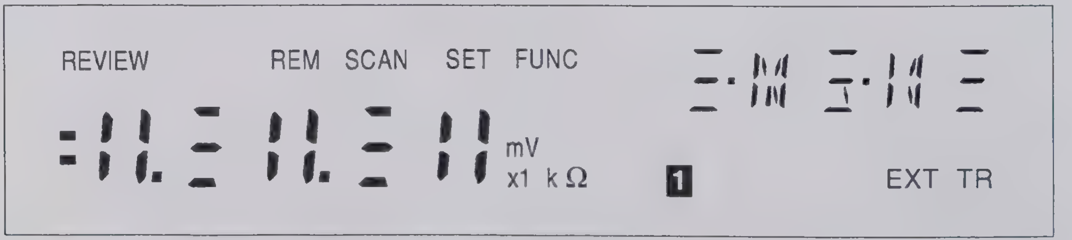

REVIEW
REM
SCAN
SET
FUNC
mV
x1 k Ω
1
EXT
TR

Figure 5-10. Display Test Pattern #1

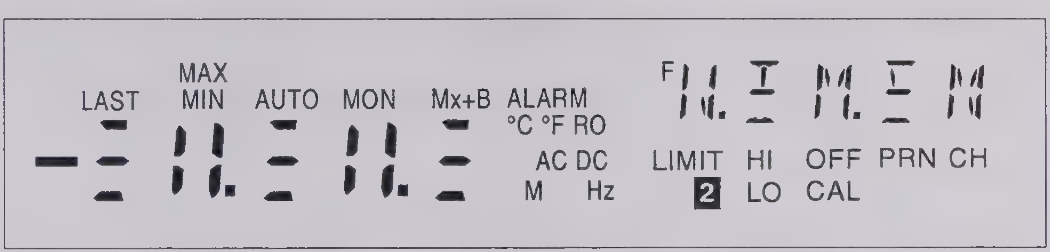


Figure 5-11. Display Test Pattern #2

NOTE

If the display is operational but has problems when front-panel buttons are pressed, proceed directly to step 9.

1. Check the three power supplies with respect to GND (A2TP3 or A2U1-42) on the Display Assembly.
   - VCC (A2U1-21) 4.85 to 5.35V dc
   - VEE (A2U1-4) -4.75 to -5.25V dc
   - VLOAD (A2U1-5) -28.5 to -32.0V dc
2. Check the filament drive signals FIL1 and FIL2; these connect to the last two pins on each end of A2DS1. These signals should be 5.4V ac with FIL2 biased to be about 6.8V dc higher than the VLOAD supply (nominally a -23.2V dc level). FIL1 and FIL2 should be 180 degrees out of phase. If the dc bias of FIL2 is not at about -23.2V dc, the display segments that should be “off” will show a shadowing (or speckling) effect.

NOTE

It may be necessary to disable the watchdog reset by jumpering A2TP1 (A2U5-3, A2U5-11) to GND (A2TP3) to verify the following items.

3. Check the clock signal CLK1 at A2TP2, A2U1-2, and A2U4-3. This signal should be a 614.4-kHz square wave (1.628 ms per cycle). This signal depends on an E clock signal of 1.2288 MHz from the Hydra Main Assembly. If the E clock is 819.2 kHz (1.221 ms per cycle), it is possible that SWR2 (A2J1-16) is shorted to ground, causing the Microprocessor to HALT at power-up.
4. Check the state of the RESET signal (A2U1-1). This signal should be low once the reset time is completed (after power-up). Also verify that the RESET* signal (A2U6-3) is high after the reset time is completed.
5. Verify that the DISRX signal (A2U1-39) goes low after RESET (A2U1-1) goes low. If this sequence does not occur, communication to the Microprocessor is held off with the DISRX signal high. If DISRX stays high but is not shorted to VCC, A2U1 must be faulty.
6. Verify activity for both the DISTX and DSCLK signals. These signals are driven by the Microprocessor and must be transitioning for the Display Controller to receive commands from the Microprocessor.

7. If all segments of a particular digit do not turn on at power-up, the grid drive from A2U1 may not be connected properly to A2DS1. Grids are numbered from 10 to 0 (left to right as the display is viewed). For a digit to be enabled, the respective grid drive signals (GRID(10:0)) must be at approximately VCC (4.85 to 5.35V dc.) For a digit to be disabled, the drive must be at VLOAD (-28.5 to -32.0V dc.)
8. If a segment under each of several (or all) grids fails to be turned on (or off) properly, one of the anode drive signals may not be connected properly from A2U1 to A2DS1. When an anode signal is at VCC, and a grid signal is at VCC, the corresponding segment on the display is illuminated.
9. If the Microprocessor has difficulty recognizing front-panel button presses, the switch scanning signals (SWR1 through SWR6, A1U4-21 through -26, respectively) should be checked. When no switch contacts are being closed, the switch scanning lines should have about 20 kΩ of resistance between each other (through two 10-kΩ pullup resistors to VCC). Unless one of the switches is closed, none of the switch scanning lines should be shorted directly to GND at any time.

VARIATIONS IN THE DISPLAY 5-19.

NOTE

The following procedure will not work with Hydra's Mainframe Firmware version 5.5.

Under normal operation, the display presents various combinations of brightly and dimly lit annunciators and digits. However, you may encounter other, random irregularities across different areas of the display under the following circumstances:

- After prolonged periods of displaying the same information.
- If the display has not been used for a prolonged period.

This phenomenon can be cleared by activating the entire display and leaving it on overnight (or at least for several hours). Use the following procedure to keep the display fully lit:

1. With power OFF, press and hold SHIFT, then press power ON.
2. Wait a moment for the instrument to beep, then release SHIFT. The entire display will now stay on until you are ready to deactivate it.
3. At the end of the activation period, press any button on the front panel; the instrument resumes the mode in effect prior to the power interruption (Active or Inactive.)

CALIBRATION FAILURES 5-20.

Introduction 5-21.

Calibration of Hydra through the computer interface is described in Section 4 of this manual. Generally, a calibration failure is indicated by a Device Dependent Error and a "!>" prompt after a CAL_STEP? command if the RS-232 interface is being used. If the IEEE-488 interface is being used, the Device Dependent Error may be detected by reading the Event Status Register (see the Hydra User Manual). These indications occur if the analog input varies from what the instrument expects to see by more than ±5% or ±15%, depending on the calibration step.

Before suspecting a fault with Hydra, verify that the calibration is being conducted properly.

- Check the connections between the source and the instrument. Are all the connections in place?
- Check the output of the calibration source. Does it equal the value called for by this calibration step?
- Check the calibration source. Is it in operate mode? Has it reverted to standby?

If a calibration step has failed, Hydra remains on that step so that the output from the calibration source may be corrected or the calibration reference value (CAL_REF) being used by Hydra may be changed if it was improperly entered. The calibration step may be repeated by sending the CAL_STEP? command to Hydra again.

Calibration of Hydra utilizes a simple "calibration by function" approach. If you suspect calibration errors, but the instrument does not exhibit the symptoms mentioned above, verify that you are observing the following calibration rules:

- Independent calibration of any function results in the storage of calibration constants for that function only.
- Once calibration is begun, all steps for that function must be completed before the calibration constants are stored. If all steps are not completed and the procedure is terminated, no constants for that function are stored; only calibration constants for previously completed functions are stored.

Calibration-Related Components 5-22.

If the calibration setup is correct, a faulty component within Hydra may be causing the failure. Each measurement function depends on a combination of components in and around the Analog Measurement Processor (A3U8).

RMS Converter	A3U6
AC Buffer	A3U7
Zener Reference	A3VR1
Divider Network (DC/Ohms)	A3Z4
Integrate Resistors, Reference Divider	A3Z2
AC Divider Network	A3Z3
RMS Converter Network	A3Z1

Basic dc measurements depend on the zener reference (A3VR1), reference divider network (A3Z2), and integrate resistors (A3Z2). Resistance measurements and dc measurements above three volts additionally depend on the resistors in the dc divider network (A3Z4). AC measurements depend on the ac divider network (A3Z3), ac buffer (A3U7), and RMS converter (A3U6), as well as the basic dc measurement components.

NOTE

During calibration, the measurement rate is selected automatically as required by the calibration step.

Table 5-9 or Table 5-10 may be useful in isolating a calibration problem to specific components. Table 5-9 can be used with a Hydra having a main software version number of 5.4 or higher. Table 5-10 can be used with main software versions lower than 5.4. Note that the software version number is not marked on the Hydra case. Use either of the following two methods to determine your software version number:

- From the Hydra front panel, simultaneously press [ltb] and [rtb]. The main software version number (e.g., "5.4") appears in the left display. (The A/D software version number (e.g., A4.7 appears in the right display.) Press [cnc] to return to normal front panel operation.
- Over the computer interface, send the *IDN? query. The main software version (e.g., "M5.4") is returned as part of the response. Refer to Section 4 of the Hydra Users Manual for a more detailed description of *IDN?.

Retrieving Calibration Constants 5-23.

If a calibration error is suspected, the stored constant can be retrieved and verified over the computer interface. Acceptable calibration constants for each function and range are listed in Table 5-9 (software version 5.4 and higher) or 5-10 (software versions lower than 5.4.) Retrieve the constant with the following command:

CAL_CONST? xx (where xx denotes the calibration constant number)

Table 5-9. Calibration Faults (for software versions 5.4 and above)

INPUT	RANGE	CALIBRATION CONSTANT		RELATED COMPONENTS
		NUMBER	ACCEPTABLE VALUES	
DC VOLTS				
0.09000V	100 mV	1	1.0315 to 1.1565	A3VR1, A3Z2
0.9000V	1V	2	1.0340 to 1.1540	A3VR1, A3Z2
0.29000V	300 mV	3	1.0315 to 1.1565	A3VR1, A3Z2
2.9000V	3V	4	1.0315 to 1.1565	A3VR1, A3Z2
29.000V	30V	5	1.0340 to 1.1640	A3VR1, A3Z2, A3Z4
290.00V	300V	6	1.0290 to 1.1590	A3VR1, A3Z2, A3Z4
AC VOLTS (1 kHz)				
0.02900V	300 mV	7	-0.001 to 0.001	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
0.29000V	300 mV	8	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
0.2900V	3V	9	-0.01 to 0.01	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
2.9000V	3V	10	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
2.900V	30V	11	-0.1 to 0.1	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
29.000V	30V	12	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
29.00V	300V	13	-1.0 to 1.0	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
290.00V	300V	14	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
OHMS				
290.00Ω	300Ω	15	0.9965 to 1.0115	A3Z2, A3Z4
2.9000 kΩ	3 kΩ	16	0.9975 to 1.0125	A3Z2, A3Z4
29.000 kΩ	30 kΩ	17	1.0015 to 1.0165	A3Z2, A3Z4
290.00 kΩ	300 kΩ	18	0.9965 to 1.0115	A3Z2, A3Z4
2.9000 MΩ	3 MΩ	19	0.9990 to 1.0090	A3Z2, A3Z4
2.9000 MΩ	10 MΩ	20	0.9990 to 1.0090	A3Z2, A3Z4
FREQUENCY				
10.000 kHz 2.9V rms		21	0.9995 to 1.0005	A3Y2

Table 5-10. Calibration Faults (for software versions lower than 5.4)

INPUT	RANGE	CALIBRATION CONSTANT		RELATED COMPONENTS
		NUMBER	ACCEPTABLE VALUES	
DC VOLTS				
0.09000V	100 mV	1	1.0315 to 1.1565	A3VR1, A3Z2
0.9000V	1V	2	1.0340 to 1.1540	A3VR1, A3Z2
0.29000V	300 mV	3	1.0315 to 1.1565	A3VR1, A3Z2
2.9000V	3V	4	1.0315 to 1.1565	A3VR1, A3Z2
29.000V	30V	5	1.0340 to 1.1640	A3VR1, A3Z2, A3Z4
290.00V	300V	6	1.0290 to 1.1590	A3VR1, A3Z2, A3Z4
AC VOLTS (1 kHz)				
0.02900V	300 mV	7	-0.001 to 0.001	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
0.29000V	300 mV	8	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
0.2900V	3V	9	-0.01 to 0.01	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
2.9000V	3V	10	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
29.000V	30V	11	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
290.00V	300V	12	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
OHMS				
290.00Ω	300Ω	13	0.9965 to 1.0115	A3Z2, A3Z4
2.9000 kΩ	3 kΩ	14	0.9975 to 1.0125	A3Z2, A3Z4
29.000 kΩ	30 kΩ	15	1.0015 to 1.0165	A3Z2, A3Z4
290.00 kΩ	300 kΩ	16	0.9965 to 1.0115	A3Z2, A3Z4
2.9000 MΩ	3 MΩ	17	0.9990 to 1.0090	A3Z2, A3Z4
2.9000 MΩ	10 MΩ	18	0.9990 to 1.0090	A3Z2, A3Z4
FREQUENCY				
10.000 kHz 2.9V rms		19	0.9995 to 1.0005	A3Y2

Replacing the EEPROM (A1U1) 5-24.

The EEPROM provides nonvolatile storage for the instrument serial number, some of the instrument configuration, and all calibration information. If the EEPROM is replaced during repair, the new EEPROM can be programmed with the 7-digit serial number found on the rear panel of the instrument or any 7-digit identifier of your choosing. Note that the serial number is not programmed prior to shipment from the factory.

The following command may be used to program the serial number into the EEPROM:

SERIAL XXXXXXX (xxxxxxx denotes the 7-digit number. Leading zeros must be entered. Note: once entered, the number cannot be changed.)

The serial number of the instrument can be accessed by using the "SERIAL?" command. The response will be "0" (if the serial number has not yet been set) or the 7-digit serial number.

IEEE-488 ASSEMBLY (A5) TROUBLESHOOTING 5-25.

Refer to Section 7 for a discussion of troubleshooting the IEEE-488 Assembly.

MEMORY ASSEMBLY (A6) TROUBLESHOOTING 5-26.

Power-Up Problems 5-27.

The following discussion identifies probable fault areas if the installation of a Memory Assembly PCA causes power-up failure for the instrument. The problem is probably a short on A6J1; the Microprocessor on the Main Assembly is prevented from accessing ROM and RAM correctly. Make the following checks:

- First check for a GND-to-VCC short on the Memory Assembly PCA.
- There may also be a short between an interface signal and VCC, GND, or another interface signal. Check signals D0 .. D7, A0 .. A2, RD*, WR*, MEM*, and RESET*.
- The short may be due to a CMOS input that has been damaged due to static discharge; the short is then detectable only when the circuit is powered up. Use an oscilloscope to check activity on each of the interface signals. Verify that signals are able to transition normally between 0 and 5.1V dc (VCC).

FAILURE TO DETECT MEMORY PCA 5-28.

If the PRINT destination cannot be set to “StorE”, Hydra was unable to determine that the Memory PCA was installed at power-up. The PRINT destination selection procedure is described in Section 3 of the User Manual.

If the Memory PCA is not detected by instrument software, there may be a problem with the IRQ2* or OPS* signal. The Memory PCA connects these two signals when it is installed. A fault with A1R2 or the Microprocessor (A1U4) could also result in failure to detect the Memory PCA.

FAILURE TO STORE DATA 5-29.

Configure the instrument to fast reading rate, 3V dc range on channel 1, and scan interval of 0:00:00. Setup storage of all scan data to the Memory PCA: press SHIFT PRINT, select “StorE”, press ENTER, select “ALL”, and press ENTER. Then, if the “PRN” annunciator is not on, enable data storage by pressing PRINT (“PRN” annunciator comes on.) Finally, enable scanning press SCAN.

While the instrument is scanning, check that data is being stored correctly. Use an oscilloscope to monitor activity on the 7 outputs of the Byte Counter (A6U3) and the 11 outputs of the Page Register (A6U1 and A6U4). Since the repetition rate is fairly low, it may be necessary to use a storage oscilloscope to capture the activity. If either of these circuit elements is not functioning, check the Address Decode circuit (A6U2, A6U5, A6U8) for activity at the end of every scan.

If the outputs of the Page Register and the Byte Counter are showing reasonable activity, verify that these signals are also being received by the Nonvolatile Memories (A6U6 and A6U7). Check CS*, WR*, and OE* inputs on A6U6 and A6U7 for proper activity.

There may also be a problem in reading data back from the Memory PCA. After allowing the Memory PCA to fill with scan data (“F” annunciator on the display lit), turn off scanning (press SCAN). Now press the LIST button and select the “StorE” entry in the menu. While the Hydra is formatting and sending the Memory PCA contents to the RS-232 interface, again monitor the circuit areas described above for reasonable voltage levels and activity.

Section 5A

Diagnostic Testing and Troubleshooting (2635A)

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INTRODUCTION 5A-1.

Hydra provides error code information and semi-modular design to aid in troubleshooting. This section explains the error codes and describes procedures needed to isolate a problem to a specific functional area. Finally, troubleshooting hints for each functional area are presented.

But first, if the instrument fails, check the line voltage fuse and replace as needed. If the problem persists, verify that you are operating the instrument correctly by reviewing the operating instructions found in the Hydra Users Manual.

WARNING

OPENING THE CASE MAY EXPOSE HAZARDOUS VOLTAGES. ALWAYS DISCONNECT THE POWER CORD AND MEASURING INPUTS BEFORE OPENING THE CASE. AND REMEMBER THAT REPAIRS OR SERVICING SHOULD BE PERFORMED ONLY BY QUALIFIED PERSONNEL.

Required equipment is listed in Section 4 of this manual.

Signal names followed by a '*' are active (asserted) low. Signal names not so marked are active high.

SERVICING SURFACE-MOUNT ASSEMBLIES 5A-2.

Hydra incorporates Surface-Mount Technology (SMT) for printed circuit assemblies (pca's). Surface-mount components are much smaller than their predecessors, with leads soldered directly to the surface of a circuit board; no plated through-holes are used. Unique servicing, troubleshooting, and repair techniques are required to support this technology. The information offered in the following paragraphs serves only as an introduction to SMT. It is not recommended that repair be attempted based only on the information presented here. Refer to the Fluke "Surface Mount Device Soldering Kit" for a complete demonstration and discussion of these techniques. (In the USA, call 1-800-526-4731 to order.)

Since sockets are seldom used with SMT, "shotgun" troubleshooting cannot be used; a fault should be isolated to the component level before a part is replaced. Surface-mount assemblies are probed from the component side. The probes should make contact only with the pads in front of the component leads. With the close spacing involved, ordinary test probes can easily short two adjacent pins on an SMT IC.

This Service Manual is a vital source for component locations and values. With limited space on the circuit board, chip component locations are seldom labeled. Figures provided in Section 6 of this manual provide this information. Also, remember that chip components are not individually labeled; keep any new or removed component in a labeled package.

Surface-mount components are removed and replaced by reflowing all the solder connections at the same time. Special considerations are required.

- The solder tool uses regulated hot air to melt the solder; there is no direct contact between the tool and the component.
- Surface-mount assemblies require rework with wire solder rather than with solder paste. A 0.025-inch diameter wire solder composed of 63% tin and 37% lead is recommended. A 60/40 solder is also acceptable.
- A good connection with SMT requires only enough solder to make a positive metallic contact. Too much solder causes bridging, while too little solder can cause weak or open solder joints. With SMT, the anchoring effect of the through-holes is missing; solder provides the only means of mechanical fastening. Therefore, the pca must be especially clean to ensure a strong connection. An oxidized pca pad causes the solder to wick up the component lead, leaving little solder on the pad itself.

Refer to the Fluke "Surface Mount Device Soldering Kit" for a complete discussion of these techniques.

ERROR CODES 5A-3.

At reset, the Hydra Data Bucket software performs power-up self-tests and initialization of Flash Memory, NVRAM, Display, Calibration Data, and measurement hardware. Self-test failures are reported on the display with "Error" in the left display and an error code (1-9,A,b,C,d) in the right display.

Several of these error codes might never be displayed. Certainly, errors 4 and 5, which signify a faulty or dead display, could not be reported in the normal (displayed) manner. Other errors might not appear on the display. Therefore, the following additional methods exist for accessing error information:

- If 'boot' is displayed at power-up, it is likely that one of the memory tests failed (Errors 1 through 3). To determine what the error status was, connect a terminal or computer to the RS-232 interface (19200 baud, 8 data bits, no parity). Send a carriage return or line feed character to the instrument and it should send back a prompt that shows a number followed by a '>' character. The number is interpreted in the same way as the responses for the *TST? and POWERUP? commands; refer to *TST? in Section 4 of the Hydra Data Bucket Users Manual. For example, a '4>' prompt indicates that the test of the NVRAM (A1U20 and A1U24) failed and the instrument was not able to safely power-up and operate.
- The computer interfaces can be used to determine self-check status using the *TST? query. Refer to Section 4 of the Hydra Data Bucket Users Manual for a description of the *TST? response. Note that the extent of the error-producing damage could also cause the instrument to halt before the computer interfaces are operational.
- The POWERUP? computer interface command can be used to determine which errors were detected at power-up. POWERUP? uses the same response format as *TST?; refer to *TST? in Section 4 of the Hydra Data Bucket Users Manual.

Table 5A-1 describes the error codes.

NOTE

Each error code is displayed for 2 seconds.

Table 5A-1. Error Codes

ERROR	DESCRIPTION
1	Boot Firmware (A1U14 and A1U16) Checksum Error
2	Instrument Firmware (A1U14 and A1U16) Checksum Error
3	NVRAM (A1U20 and A1U24) Test Failed
4	Display Power-up Test Failure
5	Display Not Responding
6	Instrument Configuration Corrupted
7	Instrument Calibration Data Corrupted
8	Instrument Not Calibrated
9	A/D Converter Not Responding
A	A/D Converter ROM Test Failure (A3U9)
b	A/D Converter RAM Test Failure (A3U9)
C	A/D Converter Self Test Failure
d	Memory Card Interface Not Installed
Refer to Troubleshooting information later in this section.	
Error 1	Boot Firmware (A1U14 and A1U16) Checksum Error All the bytes in the Boot section of Firmware (including a checksum) are summed.
Error 2	Instrument Firmware (A1U14 and A1U16) Checksum Error All the bytes in the Instrument section of Firmware (including a checksum) are summed.
Error 3	NVRAM (A1U20 and A1U24) Test Failed A test pattern of data is written to and then read from the NVRAM locations that are not used for Non-volatile instrument configuration and measurement data. If the pattern read from any RAM location is not the same as the pattern written, the test fails.
Error 4	Display Power-up Test Failure
Error 5	Display Not Responding The display processor automatically performs a self-check on power-up, and the Microprocessor attempts to read the result of this test.
Error 6	Instrument Configuration Corrupted The instrument configuration information stored in nonvolatile RAM (A1U20 and A1U24) has been corrupted. (The Cyclic Redundancy Checksum on this memory is not correct for the information stored there.) The instrument configuration is reset to the default configuration.
Error 7	Instrument Calibration Data Corrupted The Flash Memory (A1U14 and A1U16) is divided into three storage areas: the Boot Firmware, the Calibration Data, and the Instrument Firmware. The Calibration Data uses a Cyclic Redundancy Checksum (CRC) for data security, against which the data is checked on power-up.
Error 8	Instrument Not Calibrated The calibration data includes status information to indicate which of the measurement functions (Volts DC, Volts AC, Ohms, and Frequency) have been calibrated. If any functions have not been calibrated, this error is reported.

NOTE

Errors 7 and 8 should always appear the first time an instrument is powered up with a new, unitialized Flash Memory. Error 8 continues to appear at subsequent power-ups until the instrument is fully calibrated.

Table 5A-1. Error Codes (cont)

ERROR	DESCRIPTION
Error 9	A/D Converter Not Responding This error is displayed if communication cannot be established with the 6301Y Microcomputer (A3U9).
Error A	A/D Converter ROM Test Failure (A3U9) All bytes of internal ROM for the 6301Y Microcomputer (A3U9) (including the checksum byte) are summed.
Error b	A/D Converter RAM Test Failure (A3U9) Complementary patterns are alternately written to and read from each location of the 256 bytes of RAM internal to the 6301Y Microcomputer (A3U9).
Error C	A/D Converter Self Test Failure The Analog Measurement Processor (A3U8) is programmed to do self test measurements.
Error d	Memory Card Interface Not Installed The Microprocessor checks the system at power-up to determine whether the Memory Card Interface is installed.

GENERAL TROUBLESHOOTING PROCEDURES 5A-4.

Hydra allows for some fault isolation using self-diagnostic routines and descriptive error codes. However, these features are somewhat limited and do not provide in-depth troubleshooting tools.

Hydra incorporates a semi-modular design; determining modules not related to a problem constitutes the first step in the troubleshooting process.

As a first step, remove the Memory Card Interface (A6) from the Hydra Databucket (2635A). Refer to Section 3 of this manual for removal procedures. If removal of this assembly results in improved instrument operation, refer to the Memory Card Interface troubleshooting found later in this section.

Measuring the power supplies helps to isolate a problem further. Refer to Table 5A-2 and Figure 5A-1 for test point identification and readings. If power supply loading is suspected, disconnect the Display PCA at A1J2. If this action solves the loading problem, proceed to Display Assembly Troubleshooting elsewhere in this section. Otherwise, refer to Power Supply Troubleshooting.

If the power supplies appear to be good, check the Display Clock signal (DCLK (A1R85) and E clock signal (A2U4-1)). This clock signal is not symmetrical; it should be about +5.0 volts for about 325 nanoseconds and then near 0 volts for about 651 nanoseconds. If it is not correct at either measurement point, remove the Display Assembly and check the Display clock again at A1R85. If it is now correct, the problem is most likely on the Display Assembly. If it is still incorrect, the problem is probably in the Digital Kernel on the Main Assembly.

Refer to the Schematic Diagrams in Section 8 during the following troubleshooting instructions. Also, these diagrams are useful in troubleshooting circuits not specifically covered here.

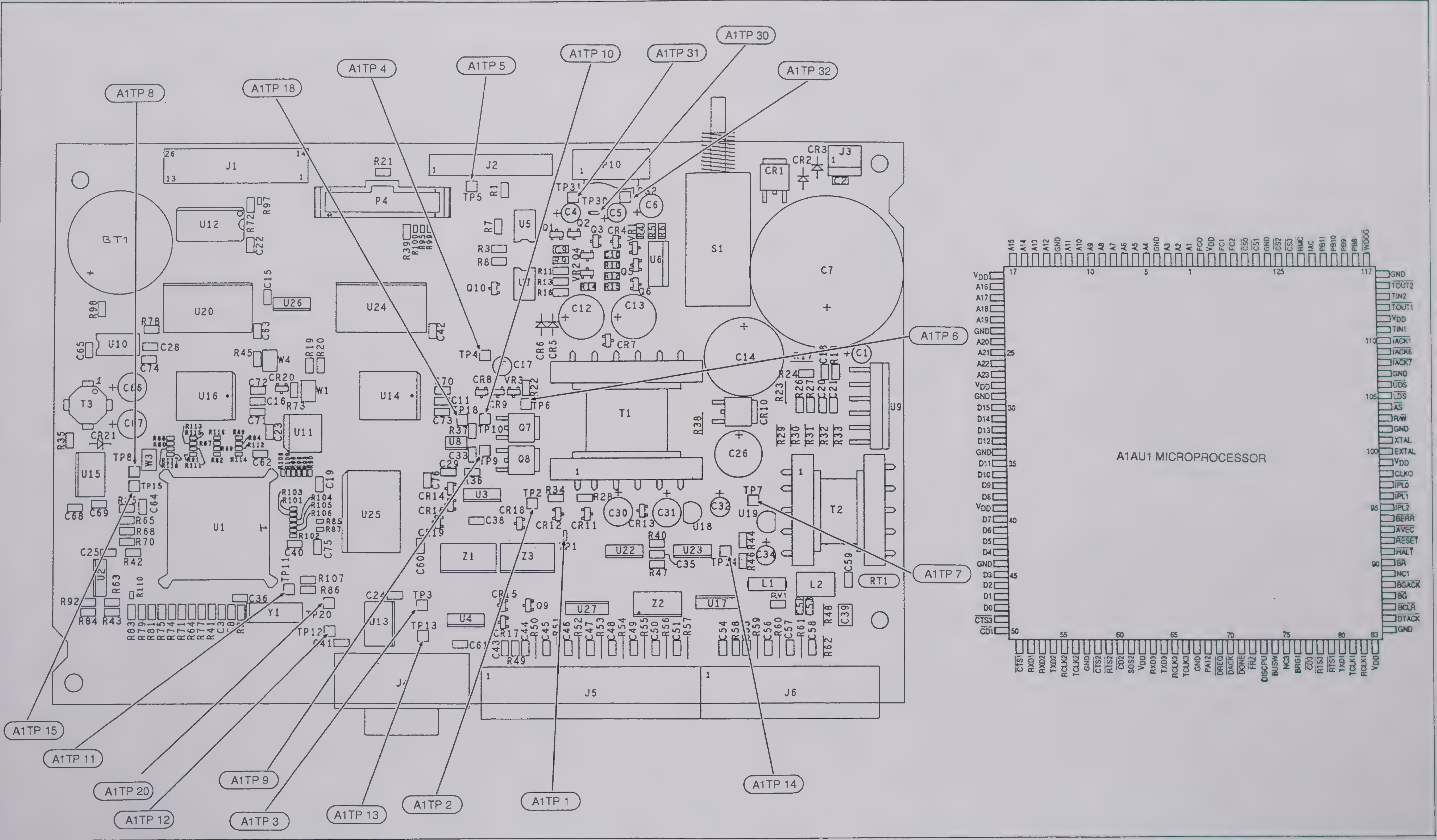

A1TP 8
A1TP 18
A1TP 4
A1TP 5
A1TP 10
A1TP 31
A1TP 30
A1TP 32
A1TP 6
A1TP 7
A1TP 15
A1TP 11
A1TP 20
A1TP 12
A1TP 9
A1TP 3
A1TP 13
A1TP 2
A1TP 1
A1TP 14
A1AU1 MICROPROCESSOR
A15 A14 A13 A12 GND A11 A10 A9 A8 A7 A6 A5 A4 GND A3 A2 A1 FC0 VDD FC1 FC2 CS0 CS1 GND CS2 CS3 RMC IAC PB11 PB10 PB9 PB8 WDOG
GND TOUT2 TIN2 TOUT1 VDD TIN1 IACK1 IACK6 IACK7 GND UDS LDS AS R/W GND XTAL EXTAL VDD CLKO IPL0 IPL1 IPL2 BERR AVEC RESET HALT BR NC1 BGACK BG BCLR DTACK GND
CTS1 RXD1 RXD2 TXD2 RCLK2 TCLK2 GND CTS2 RTS2 CD2 SDS2 VDD RXD3 TXD3 RCLK3 TCLK3 GND PA12 DREQ DACK DONE FRZ DISCPU BUSW NC3 BRG1 CD3 RTS3 RTS1 TXD1 TCLK1 RCLK1 VDD
VDD A16 A17 A18 A19 GND A20 A21 A22 A23 VDD GND D15 D14 D13 D12 GND D11 D10 D9 D8 VDD D7 D6 D5 D4 GND D3 D2 D1 D0 CTS3 CD1
17 10 5 1 125 117 110 105 100 95 90 83 80 75 70 65 60 55 50 45 40 35 30 25

Figure 5A-1. Test Point Locator, Main PCA (A1)

Table 5A-2. Preregulated Power Supplies

PREREGULATED VOLTAGE	MEASUREMENT POINTS	RESULTING SUPPLY
-8.5V	A1CR13-2 to A1TP1	VEE
-29.5V	A1TP4 to A1TP1	VLOAD
+8.9V	A1CR5 cathode to A1TP30	VDD, VDDR
-8.3V	A1CR7 anode and A1TP30	VSS

POWER SUPPLY TROUBLESHOOTING 5A-5.

WARNING

TO AVOID ELECTRIC SHOCK, DISCONNECT ALL CHANNEL INPUTS FROM THE INSTRUMENT BEFORE PERFORMING ANY TROUBLESHOOTING OPERATIONS.

Raw DC Supply 5A-6.

With the instrument connected to line power (120V ac, 60 Hz) and turned ON, check for approximately 14V dc between A1TP1 (GND) and the "+" terminal of capacitor A1C7 (or the cathode of either A1CR2 or A1CR3). (This voltage is approximately 30V dc at 240V ac line.) If no voltage or a very low voltage is present, check for approximately 24V ac across the secondary of the power transformer (or approximately 50V ac at 240V ac line).

The voltage at the output of A1U19 (also A1TP7), should be about +5.3V dc. At 120V ac, 60-Hz line power input, the Hydra Databucket line current is approximately 24 mA. At 50-Hz, 120V ac line power input, there is a 5 to 10% increase in this current figure.

Power Fail Detection 5A-7.

The Power Fail Detection circuit monitors the Raw Supply so that the Microprocessor can be signaled when power is failing. A reference voltage of nominally 1.3 volts dc (internal to A1U10) is compared to the voltage at A1U10-4. If A1U10-4 is less than about 1.3 volts dc, the power fail output (A1U10-5) should be low. This corresponds to a raw supply voltage of about 8 volts dc (A1C7). If the raw supply voltage is greater than 8 volts dc, the power fail output (A1U10-5) should be high. If the power fail output is near 0V dc during normal operation, the Microprocessor will sense that power is failing and will not be able to complete a scan operation.

5-Volt Switching Supply 5A-8.

Use an oscilloscope to troubleshoot the 5-volt switching supply. With the oscilloscope common connected to A1TP1, check the waveform at either A1U9, pin 7 (switch transistor collector) or A1T1, pin 2 to determine the loading on the 5-volt switching supply. The output voltage of the 5-volt switching supply at A1TP2 (VCC) is normally about 5.0V dc with respect to A1TP1 (GND). Note that a fault in the load (high or low resistance) can appear as a faulty output voltage of the 5-volt switching supply.

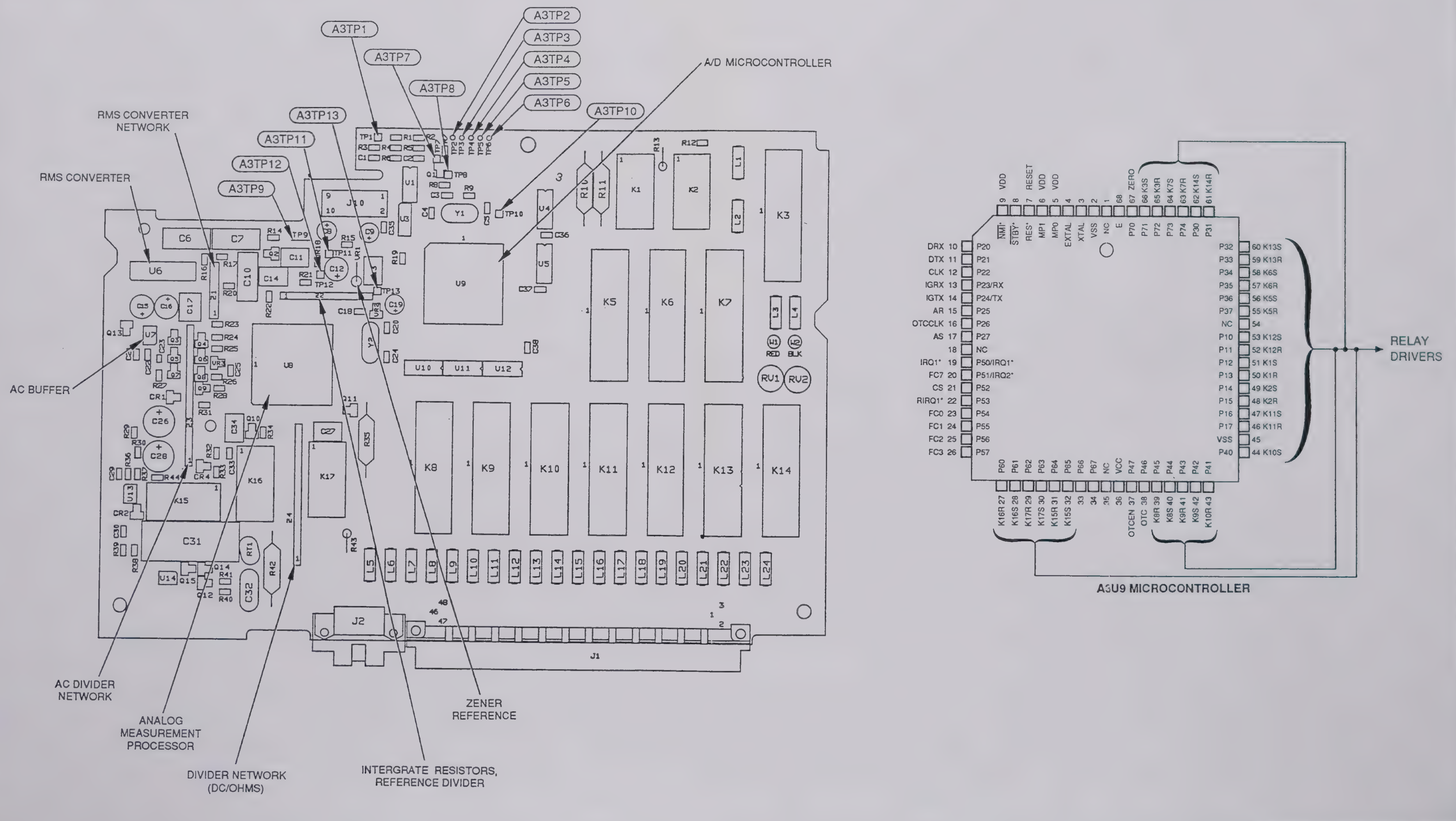

A3TP1
A3TP7
A3TP8
A3TP2
A3TP3
A3TP4
A3TP5
A3TP6
A3TP10
A3TP13
A3TP11
A3TP12
A3TP9
A/D MICROCONTROLLER
RMS CONVERTER NETWORK
RMS CONVERTER
AC BUFFER
AC DIVIDER NETWORK
ANALOG MEASUREMENT PROCESSOR
DIVIDER NETWORK (DC/OHMS)
INTERGRATE RESISTORS, REFERENCE DIVIDER
ZENER REFERENCE
U6
U7
U8
U9
J1
J2
K1
K2
K3
K5
K6
K7
K8
K9
K10
K11
K12
K13
K14
K15
K16
K17
RED
BLK
RV1
RV2
RELAY DRIVERS
A3U9 MICROCONTROLLER
DRX 10 P20
DTX 11 P21
CLK 12 P22
IGRX 13 P23/RX
IGTX 14 P24/TX
AR 15 P25
OTCCLK 16 P26
AS 17 P27
18 NC
IRQ1* 19 P50/IRQ1*
FC7 20 P51/IRQ2*
CS 21 P52
RIRQ1* 22 P53
FC0 23 P54
FC1 24 P55
FC2 25 P56
FC3 26 P57
9 VDD NMI*
8 STBY*
7 RESET RES*
6 VDD MP1
5 VDD MP0
4 EXTAL
3 XTAL
2 VSS
1 NC
68 E
67 ZERO P70
66 K3S P71
65 K3R P72
64 K7S P73
63 K7R P74
62 K14S P30
61 K14R P31
K16R 27 P60
K16S 28 P61
K17R 29 P62
K17S 30 P63
K15R 31 P64
K15S 32 P65
33 P66
34 P67
35 NC
36 VCC
OTCEN 37 P47
OTC 38 P46
K8R 39 P45
K8S 40 P44
K9R 41 P43
K9S 42 P42
K10R 43 P41
P32 60 K13S
P33 59 K13R
P34 58 K6S
P35 57 K6R
P36 56 K5S
P37 55 K5R
NC 54
P10 53 K12S
P11 52 K12R
P12 51 K1S
P13 50 K1R
P14 49 K2S
P15 48 K2R
P16 47 K11S
P17 46 K11R
VSS 45
P40 44 K10S

Figure 5A-4. Test Points, A/D Converter PCA (A3, A3U8)

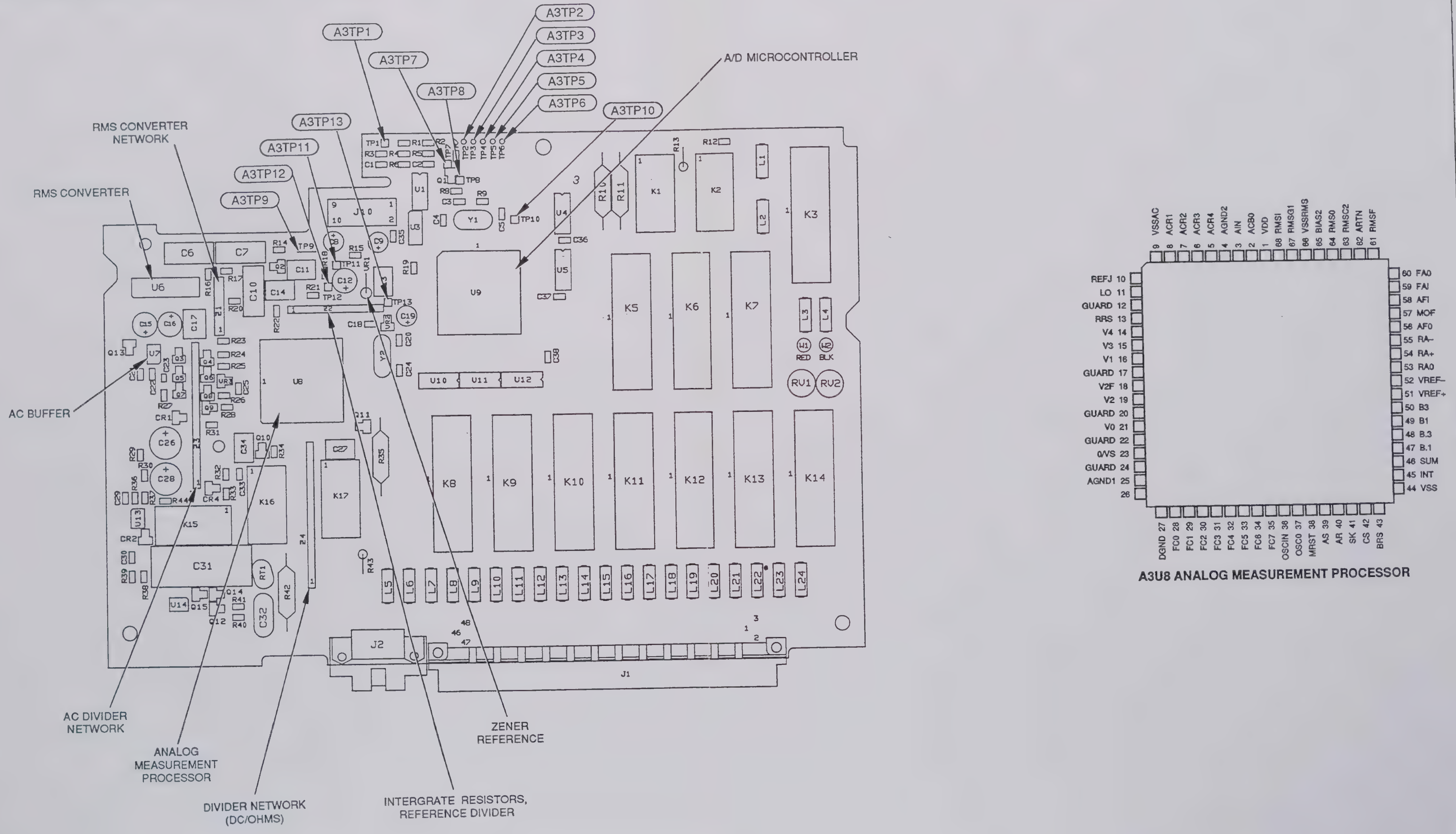

A3TP1
A3TP2
A3TP3
A3TP4
A3TP5
A3TP6
A3TP7
A3TP8
A3TP9
A3TP10
A3TP11
A3TP12
A3TP13
A/D MICROCONTROLLER
RMS CONVERTER NETWORK
RMS CONVERTER
AC BUFFER
AC DIVIDER NETWORK
ANALOG MEASUREMENT PROCESSOR
DIVIDER NETWORK (DC/OHMS)
INTERGRATE RESISTORS, REFERENCE DIVIDER
ZENER REFERENCE
U9
U8
J1
J2
A3U8 ANALOG MEASUREMENT PROCESSOR
9 VSSAC
8 ACR1
7 ACR2
6 ACR3
5 ACR4
4 AGND2
3 AIN
2 ACB0
1 VDD
68 RMSI
67 RMSG1
66 VSSRMS
65 BIAS2
64 RMS0
63 RMSC2
62 ARTN
61 RMSF
REFJ 10
LO 11
GUARD 12
RRS 13
V4 14
V3 15
V1 16
GUARD 17
V2F 18
V2 19
GUARD 20
V0 21
GUARD 22
0/VS 23
GUARD 24
AGND1 25
26
60 FA0
59 FAI
58 AFI
57 MOF
56 AF0
55 RA-
54 RA+
53 RA0
52 VREF-
51 VREF+
50 B3
49 B1
48 B.3
47 B.1
46 SUM
45 INT
44 VSS
DGND 27
FC0 28
FC1 29
FC2 30
FC3 31
FC4 32
FC5 33
FC6 34
FC7 35
OSCIN 36
OSC0 37
MRST 38
AS 39
AR 40
SK 41
CS 42
BRS 43

Figure 5A-5. Test Points, A/D Converter PCA (A3, A3U9)

PCA	TEST POINT	TO	PULSES
A/D Converter	A3TP7	A3TP9	5.55V (VDDR) to 0.7V
Main	A1TP8	A1TP1	5.0V dc (VCC) to 0.0V

Lack of outguard-to-inguard communication activity may be due to improper operation of circuit elements other than A3U9. Using a high input impedance oscilloscope or timer/counter, check for proper Analog Processor (A3U8) crystal oscillator operation. A 3.84-MHz sine wave (260 ns period) should be present at A3U8 pin 37 with respect to A3TP9.

Check the A/D Converter voltage reference:

A3TP12 to A3TP11 (across A3C12) = +1.05V (+0.10V, -0.02V)

Setup the instrument to measure ohms on the 300Ω range. Monitor ohms on a channel with an input of approximately 270Ω. Check that the Analog Processor IC (A3U8) is making A/D conversions. The integrator output waveform at A3TP13 (referenced to A3TP9) should resemble the waveform shown in Figure 5A-6.

Check for channel relay operation by setting up a channel and selecting and de-selecting monitor measurement mode. One or more relays should click each time the monitor button is pressed or channels are changed.

In general, check that the relays are getting the proper drive pulse signals for specific functions and channels and that they are in the correct position.

DC Volts Troubleshooting 5A-11.

Setup the instrument to measure a specific channel on the 300 mV or 3V range, and apply an input to that channel. Then trace the HI signal (referenced to the input channel LO terminal) as described in Table 5A-4.

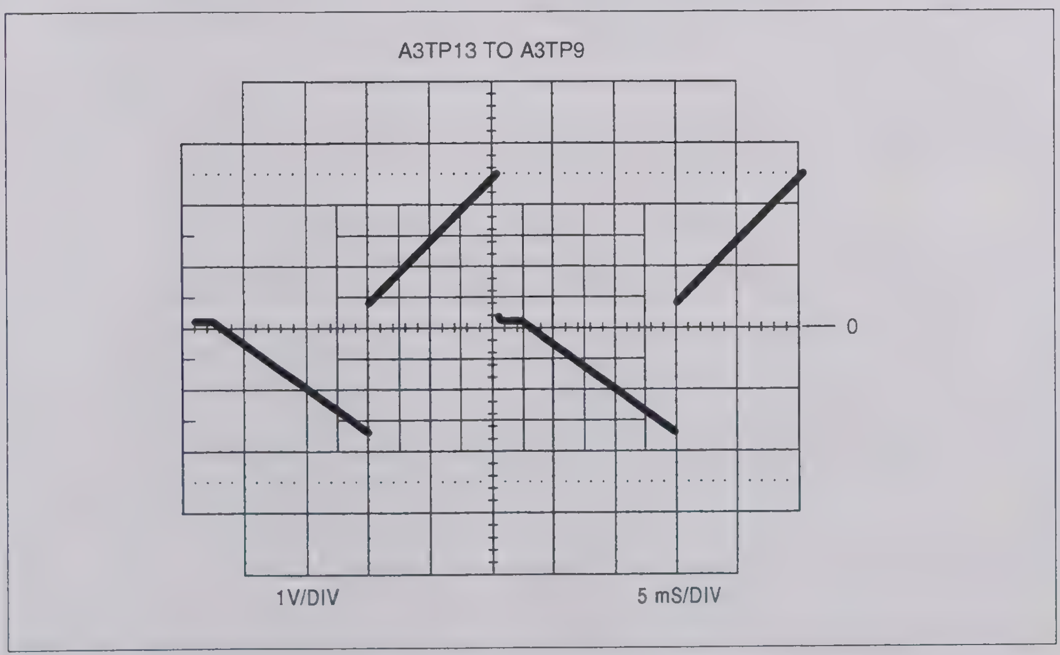


Figure 5A-6. Integrator Output

If the input HI path traces out properly, remove the input from the channel and trace continuity through the LO path. Check among A3L4-A3L24, A3K1-A3K14, A3R35, A3R43, and A3U8 pin 11.

AC Volts Troubleshooting 5A-12.

Setup the instrument to measure a channel on the 300 mV ac range, and apply a signal to that channel. Then trace this HI signal (referenced to the input channel LO terminal) as described in Table 5A-5.

If the input HI path traces out properly, remove the input from the channel, and trace continuity through the LO path. Check among A3L4 through A3L24, A3K1 through A3K14, A3R43, A3R34, A3K16, and A3U8 pin 13.

Ohms Troubleshooting 5A-13.

Setup a channel with an open input for the desired ohms range and place the instrument in monitor mode on that channel. Use a meter with high input impedance to measure the open-circuit voltage at the channel input for the ohms range as listed in Table 5A-6. If a high input impedance meter is not available, only the 30-kΩ and lower ranges can be checked.

If the proper voltage is not measured, setup a channel on the 300Ω range (open input), and have the instrument monitor that channel. Check for 3V dc with respect to A3TP9, and work through the HI SOURCE and HI SENSE paths as described in Table 5A-7.

If the HI path works correctly, trace continuity through the LO path. Check among A3L4 through A3L24, A3K1 through A3K14, A3R35, A3U8 pin 11, A3R43, A3K16, A3R34, and A3U8 pin 13.

Table 5A-4. DC Volts HI Troubleshooting

CHECKPOINT	SIGNAL DESCRIPTION	POSSIBLE FAULT
A3R11 HI	Input	A3K1 through A3K14, A3U4, A3U5, A3U11, A3U12, A3L1, A3L2, A3L3
A3U8 pin 23	Input	A3R11, A3K17, A3R42, A3C32
A3U8 pin 58	Input, DC filter output	A3U8, A3Q2

Table 5A-5. AC Volts HI Troubleshooting

CHECKPOINT	SIGNAL DESCRIPTION	POSSIBLE FAULT
A3R11 HI	Input	A3K1 through A3K14, A3U4, A3U5, A3U11, A3U12 A3L1, A3L2, A3L3
A3Z3 pin 1	Input	A3R11, A3C31, A3K15
A3U6 pin 13	Amplified (X 2.5) input	A3U7, A3Z3, A3Q3 through A3Q9, A3C15, A3C16, A3R24, A3A25, A3R26, A3R27, A3R28, A3C23, A3U6, A3Q13, A3U8
A3Z1 pin 2	DC equivalent of amplified input	A3U6, A3C17
A3U8 pin 61	DC equivalent of original input	A3Z1, A3U8, A3R20, A3C6, A3C7, A3C10, A3R16, A3R17

Table 5A-6. Ohms Open-Circuit Voltages

RANGE	VOLTAGE
300Ω	3V
3 kΩ	1.3V
30 kΩ	1.3V
300 kΩ	3V
3 MΩ	3V
10 MΩ	3V

Table 5A-7. Ohms HI Troubleshooting

CHECKPOINT	SIGNAL DESCRIPTION	POSSIBLE FAULT
A3U8 pin 14	Ohms Source	A3U8
A3R10 HI SRC	Ohms Source	A3R10, A3K16, A3RT1, A3Z4, A3Q10
Channel HI	Ohms Source	A3K1 through A3K14, A3U4, A3U5, A3U11, A3U12, A3L1, A3L2, A3L3
A3U8 pin 23	Ohms Source	A3R11, A3K17, A3R42, A3C32
A3U8 pin 58	Ohms source, filter output	A3U8, A3Q2

DIGITAL KERNEL TROUBLESHOOTING 5A-14.

At power-up, if the display does not light or lights up and fails to report errors or begin operation, use the following troubleshooting procedures.

To determine the relative health of the MC68302 Microprocessor (A1U1), first check for a valid system clock (SCLK) at TP11. Use an oscilloscope to check for the SCLK clock at A1TP11. Look for a 12.288-MHz square wave that transitions from 0 to 5V dc (VCC).

- If this signal is present, check for a similar waveform at pin A1U25-30 of the FPGA. If a 12.288-MHz square wave is not present there, resistor A1R107 is probably bad.
- If the SCLK signal (A1TP11) is something other than a 12.288-MHz square wave, it is most likely that the problem is related to the crystal oscillator circuit (A1U1, A1Y1, A1C3, A1C8, or A1R2).

If the SCLK signal is good, check the Display Clock (DCLK) output from A1U25-19. DCLK should have a frequency of 1.024-MHz (period of 976 nanoseconds). The DCLK signal is not symmetrical; use an oscilloscope to verify that it is high for about 325 nanoseconds and then low for about 651 nanoseconds. The operation of the Display assembly depends on the DCLK signal. Missing segments, intensified digits, a strobing display, or a blank display can be caused by a faulty DCLK clock.

- If the DCLK signal (A1U25-19) is not present but the SCLK signal is correct at A1U25-30, the problem may be that A1U25 was not configured correctly at power-up or A1U25 is defective.
- If the OCLK signal (A1U25-22) is a 3.072-MHz square wave but the DCLK signal is wrong, A1U25 must be defective.

During instrument power-up, the RESET* and HALT* signals are held low for 140 to 280 milliseconds after the VCC power supply is greater than 4.65 volts dc. Before the Microprocessor can begin execution of the firmware stored in the Flash Memory, the reset circuit must release the RESET* and HALT* signals (A1U2-11 and A1U2-8 respectively) and allow them to go high. Verification of the operation of the RESET* and HALT* signals is best done by using a storage oscilloscope.

After the Microprocessor has begun execution of the instructions stored in Flash Memory (A1U14 and A1U16), the Microprocessor may drive the HALT* signal (A1U1-91) low if the instructions executed are not correct. Another sign of incorrect instruction execution is the Bus Error signal (BERR*;A1U1-94) going low to indicate that an access to an unused area of memory space was done. To troubleshoot these problems, use an oscilloscope to check the activity of the address, data, and control signals to the Flash Memory devices (A1U14 and A1U16). It may also be useful to check signal continuity by using a DMM with the instrument power off.

To check the Flash Memory control signals, verify that A1U1-128 is going low and is also appearing on pins A1U14-22 and A1U16-22 of the Flash Memory devices. It may be necessary to continually reset (power on) the instrument to check these lines, since the activity probably halts quickly when the instrument software goes awry. Verify that RDU* (A1U11-14 and A1U14-24) goes low when A1U1-128 is low. Verify that RDL* (A1U11-19 and A1U16-24) goes low when A1U1-128 is low. If all this is true, the problem is with the Flash Memory itself or there is a fault in the address/data lines from the MC68302 Microprocessor.

Verify that the XINIT* output (A1U25-65) goes high after RESET* goes high. Verify that the mode pins and extra chip select input on the FPGA (A1U25) are properly connected to VCC and GND. Pins 6, 29, 54, and 56 must be about 5 volts dc. Pins 52 and 93 must be near 0 volts dc. If the Microprocessor is able to correctly fetch instructions from the Flash Memory, the Microprocessor tries to program the FPGA.

Address decoding for I/O devices like the FPGA is done by A1U11. Verify that the PGA* output (A1U11-12) goes low when the Microprocessor attempts to access the FPGA. Verify the address and I/O* inputs to A1-U11 (pins 2 through 8) according to the decoding shown in the following table.

OUTPUT	A<12>	A<11>	A<10>	A<9>	A<8>	A<7>	I/O*
PGA* (A1U11-12)	0	0	0	0	0	0	0
RTC* (A1U11-16)	0	0	0	0	0	1	0
OPTE* (A1U11-12)	0	0	0	0	1	0	0

Programming of the FPGA is initiated by the Microprocessor by driving the XD/P* (A1U25-80) and RESET* (A1U25-78) signals low simultaneously. RESET* is pulsed low by the Microprocessor for approximately 10 microseconds. The Microprocessor then waits for XINIT* (A1U25-65) to go high; if this doesn't happen, the Watchdog Timer in the Microprocessor will reset the instrument after several seconds by driving POR* (A1U1-117) low. Verify that the Microprocessor waits until XRDY (A1U25-99) is high before writing each byte to the FPGA. (A1U25-88 and A1U25-5 both go low during the write cycle.) Check the XD/P* signal (A1U25-80) at the end of the FPGA programming; if it doesn't go high, the Microprocessor will repeat the FPGA programming sequence until it works correctly or the Watchdog Timer in the Microprocessor resets the instrument by driving POR* (A1U1-117) low. If FPGA programming is failing, check the D<8> through D<15>, PGA*, WRU*, XINIT*, XRDY, XD/P*, and RESET* signals for activity with an oscilloscope. It may also be necessary to check the continuity of these signals with a DMM when the instrument power is off.

If the instrument powers up and displays ‘boot,’ it is likely that one of the memory test errors (Errors 1 through 3) was detected. To determine what the error status was, connect a terminal or computer to the RS-232 interface (19200 baud, 8 data bits, no parity). Assuming that the RS-232 interface is functional, send a carriage return or line feed character to the instrument, and it should send back a prompt that shows a number followed by a ‘>’ character. The number is interpreted in the same way as the responses for the *TST? and POWERUP? commands; refer to *TST? in Section 4 of the Hydra Data Bucket Users Manual. For example, a ‘4>’ prompt indicates that the test of the NVRAM (A1U20 and A1U24) failed and the instrument was not able to safely power-up and operate.

Now send a ‘t’ character followed by a carriage return to the instrument to request a retest of the firmware stored in Flash Memory. If both the boot firmware and the instrument firmware checksums are correct, the response will be as follows:

```
Boot image OK
Hydra image OK
0>
```

If the boot firmware checksum is not correct, the message “Bad boot image -- use at own risk!” might be seen. The code that must be executed to generate this message is part of the boot firmware that is bad, so there is no guarantee that this message will be seen.

If the instrument firmware checksum is not correct, one of the following error messages may be seen:

Bad rom pointer	“Invalid pointer to checksum structure”
Bad checksum pointer	“Invalid pointer to instrument checksum”
Bad checksum	“Incorrect instrument checksum”

Invalid instrument firmware may be corrected by using a personal computer to load new instrument firmware into the Hydra Databucket. To do this see the section entitled “Updating the 2635A Instrument Firmware” in Section 4 of this manual.

If the NVRAM (A1U20 and A1U24) do not operate correctly, the problem must be corrected before new instrument firmware may be loaded or the instrument can power up completely. Use an oscilloscope to check the activity of the address, data, and control signals to the NVRAM devices (A1U14 and A1U16). It may be necessary to continually reset (power on) the instrument to check these lines, since the activity probably halts quickly when the instrument software goes awry. To check the NVRAM control signals, verify that A1U1-127 is going low, propogating through A1U26, and also appearing on pins A1U20-22 and A1U24-22 of the NVRAM devices. Verify that RDU* (A1U11-14 and A1U24-24) goes low when A1U1-127 is low. Verify that RDL* (A1U11-19 and A1U20-24) goes low when A1U1-127 is low. If all this is true, the problem is with the NVRAM itself or there is a fault in the address/data lines from the MC68302 Microprocessor. It may also be useful to check signal continuity by using a DMM with the instrument power off. Verify also that pin 30 on A1U24 and A1U20 is pulled up to approximately 5.0 volts dc by resistor A1R45.

Figure 5A-7 shows the timing relationships of the MC68302 Microprocessor address, data, and memory control signals used for memory read and write cycles. The chip selects from the Microprocessor (FLASH*, SRAM*, MCARD*, and I/O*) are decoded internally from the address bus and the address strobe (AS*) signal. Therefore the AS* waveform is the same as the chip select signal for the device that the Microprocessor is accessing.

If the instrument powers up without any errors, but does not recognize front-panel button presses, the problem may be in the Keyboard Interrupt (KINT*) signal from the FPGA. If the KINT* output (A1U25-62) is low (and never goes high), the Microprocessor (A1U1) is failing to recognize the interrupt, or the microprocessor interface to A1U25 is not working correctly. Verify that the KINT* signal gets to the input pin (A1U1-121) on the Microprocessor.

If the interval time does not count down properly when scanning is enabled, the problem may be in the Real-Time Clock Interrupt (CINT*) signal from the Real-Time Clock (A1U12). If the CINT* output (A1U12-3) is low (and never goes high), the Microprocessor (A1U1) is failing to recognize the interrupt or the microprocessor interface to A1U12 is not working correctly. Verify that the CINT* signal gets to the input pin (A1U1-96) on the Microprocessor. Also verify that the Real-Time Clock is actively keeping time by checking for a 1-Hz square wave output on A1U12-4. Pin A1U12-2 must also be properly connected to GND for the Real-Time Clock to operate. The interface to the Microprocessor operates very much like the interface to NVRAM device A1U20.

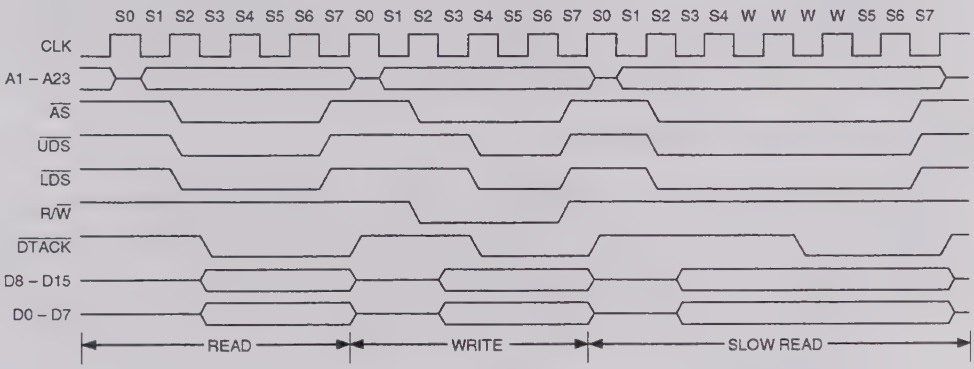
DIGITAL AND ALARM OUTPUT TROUBLESHOOTING 5A-15.

Power up Hydra while holding down the CANCL button to reset the instrument configuration. Since the structure of the eight Digital Outputs and four Alarm Outputs is very similar, the troubleshooting procedure presented here does not refer to specific device and pin numbers. First verify that the input of the Output Driver (A1U17 or A1U27) is low and that the output is near +5V dc. If the input is high, the problem may be in the FPGA (A1U25). If the output is not near +5V dc, use an ohmmeter to check the pull-up resistor in A1Z2.

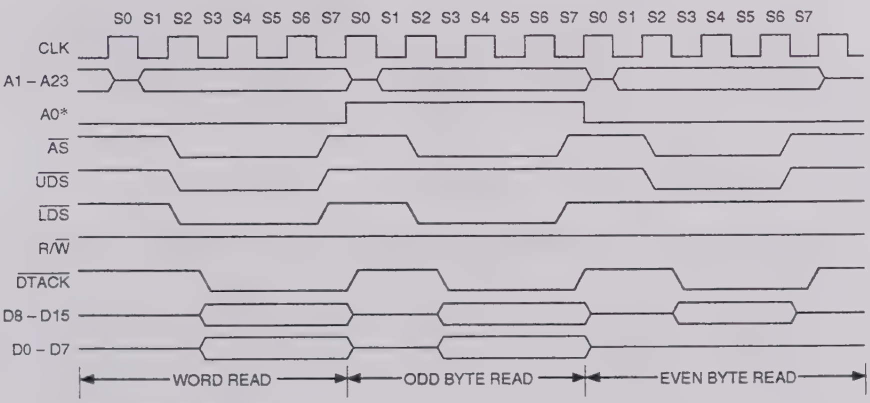
Use the proper computer interface command to change the state of the Digital Output (DO_LEVEL x,1) or Alarm Output (ALARM_DO_LEVEL x,1), where x is the number of the output being checked. Now verify that the input of the Output Driver is high and that the output is near +0.8V dc. If there is no change in the input, check the address signals to the FPGA (A1U25-85, A1U25-90, A1U25-96, A1U25-97) and the behavior of the output pin on the FPGA that goes to the input of the Output Driver (A1U17 or A1U27). If the output of the Output Driver fails to change when the input does, the problem is most likely the inverting output driver (A1U17 or A1U27).

DIGITAL INPUT TROUBLESHOOTING 5A-16.

Power up Hydra while holding down the CANCL button to reset the instrument configuration. Verify that the Input Buffer Threshold circuit generates approximately 1.4V dc at A1TP18. Drive the Digital Input (A1J5) to be checked with a signal generator outputting a 100-Hz square wave that transitions from 0 to +5V dc. The signal generator output common should be connected to Common (A1J5-1). Verify that the output of the Input Buffer is a 100-Hz square wave that is the inverse of the input signal.

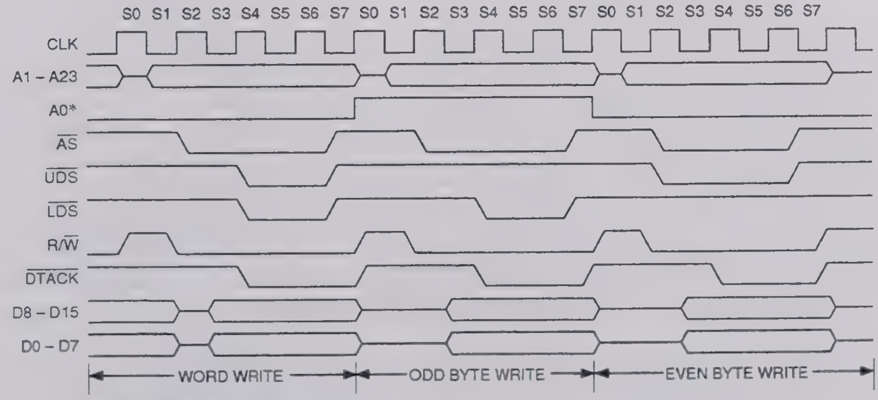

S0 S1 S2 S3 S4 S5 S6 S7 S0 S1 S2 S3 S4 S5 S6 S7 S0 S1 S2 S3 S4 W W W W S5 S6 S7
CLK
A1 – A23
$\overline{AS}$
$\overline{UDS}$
$\overline{LDS}$
R/$\overline{W}$
$\overline{DTACK}$
D8 – D15
D0 – D7
READ
WRITE
SLOW READ

READ AND WRITE CYCLE TIMING DIAGRAM


S0 S1 S2 S3 S4 S5 S6 S7 S0 S1 S2 S3 S4 S5 S6 S7 S0 S1 S2 S3 S4 S5 S6 S7
CLK
A1 – A23
A0*
$\overline{AS}$
$\overline{UDS}$
$\overline{LDS}$
R/$\overline{W}$
$\overline{DTACK}$
D8 – D15
D0 – D7
WORD READ
ODD BYTE READ
EVEN BYTE READ

*INTERNAL SIGNAL ONLY

WORD AND BYTE READ CYCLE TIMING DIAGRAM


S0 S1 S2 S3 S4 S5 S6 S7 S0 S1 S2 S3 S4 S5 S6 S7 S0 S1 S2 S3 S4 S5 S6 S7
CLK
A1 – A23
A0*
$\overline{AS}$
$\overline{UDS}$
$\overline{LDS}$
R/$\overline{W}$
$\overline{DTACK}$
D8 – D15
D0 – D7
WORD WRITE
ODD BYTE WRITE
EVEN BYTE WRITE

*INTERNAL SIGNAL ONLY

WORD AND BYTE WRITE CYCLE TIMING DIAGRAM

Figure 5A-7. Microprocessor Timing

If the Input Buffer does not function correctly, the problem is probably A1Z1, A1Z3, or the associated comparator (A1U3 or A1U4). If the Input Buffer functions correctly, but Hydra is not able to read the state of the Digital Input correctly, the problem is most likely the FPGA (A1U25). If Hydra is not able to read the states of any of the eight Digital Inputs correctly, the problem is most likely in the address signals going to the FPGA (A1U25-85, A1U25-90, A1U25-96, A1U25-97).

TOTALIZER TROUBLESHOOTING 5A-17.

Power up Hydra while holding down the CANCL button to reset the instrument configuration. Verify that the Input Buffer Threshold circuit generates approximately 1.4V dc at A1TP18. Drive the Totalizer Input (A1J5-2) with a signal generator outputting a 100-Hz square wave that transitions from 0 to +5V dc. The signal generator output common should be connected to Common (A1J5-1). Verify that the output of the Input Buffer (A1U8-1) is a 100-Hz square wave that is the inverse of the input signal. Verify also that the input to the totalizer counter (A1TP20) is a buffered form of the signal just verified at the output of the Input Buffer.

Use the following procedure to troubleshoot the totalizer input debouncer, Enable the totalizer debouncer by sending the TOTAL_DBNC 1 Computer Interface command to the instrument. With the signal generator still connected and outputting a 100-Hz square wave, verify that the waveform at the input to the totalizer counter (A1TP20) is delayed by 1.75 milliseconds from the waveform at A1U8-1.

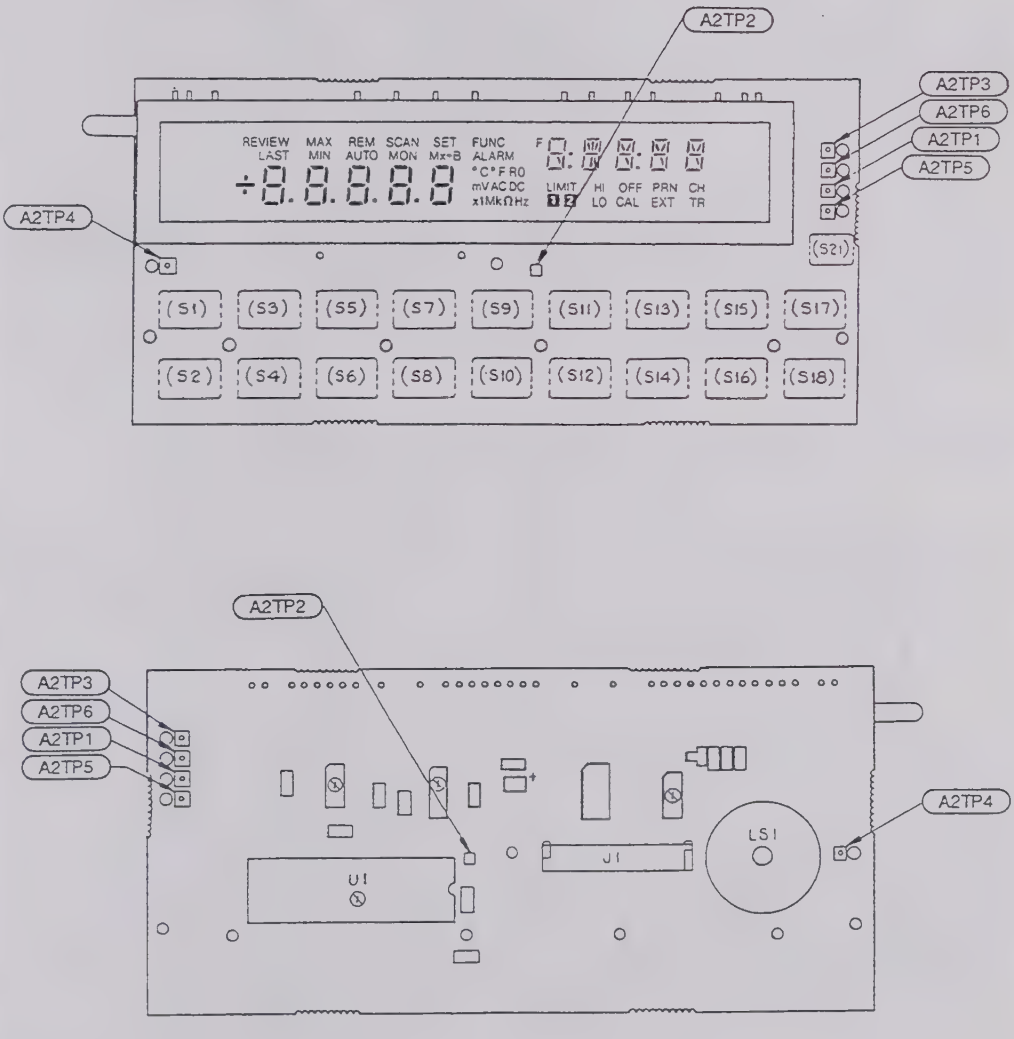
DISPLAY ASSEMBLY TROUBLESHOOTING 5A-18.

The following discussion is helpful if it has been determined that the Display Assembly is faulty. Refer to Figure 5A-8 for Display PCA test points. This initial determination may not be arrived at easily, since an improperly operating display may be the result of a hardware or software problem that is not a direct functional part of the Display Assembly. Consult the General Troubleshooting Procedures found earlier in this section for procedures to isolate the fault to the Display Assembly. Use the following discussion of display software operation when troubleshooting problems within a known faulty Display Assembly. A Display Extender Cable (PN 867952) is available for use during troubleshooting. Note that this cable must be twisted to mate correctly to the connectors on Display and Main PCAs.

The Display Controller reads the DTEST* and LTE* inputs to determine how to initialize the display memory. DTEST* (A2TP4) and LTE* (A2TP5) default to logic 1 and logic 0, respectively, to cause all display segments to be initialized to “on.” Either test point can be jumpered to VCC (A2TP6) or GND (A2TP3) to select other display initialization patterns. Display Test Patterns #1 and #2 are a mixture of “on” and “off” segments with a recognizable pattern to aid in troubleshooting problems involving individual display segments. When either of the special display patterns is selected, the beeper is also sounded for testing without interaction with the Microprocessor. Table 5A-8 indicates the display initialization possibilities.

Figure 5A-9 shows the timing of communications between the Microprocessor and the Display Controller. Figures 5A-10 and 5A-11 show Display Test Patterns #1 and #2, respectively. Refer to the Display Assembly schematic diagram in Section 8 for information on grid and anode assignments.

When a Hydra display is initially powered up, all display segments should come on automatically. If this display does not appear, proceed with the following steps:


A2TP2
A2TP3
A2TP6
A2TP1
A2TP5
A2TP4
REVIEW
LAST
MAX
MIN
REM
AUTO
SCAN
MON
SET
Mx+B
FUNC
ALARM
°C°F RO
mVACDC
x1MkΩHz
LIMIT
1 2
HI
LO
OFF
CAL
PRN
EXT
CH
TR
(S1)
(S2)
(S3)
(S4)
(S5)
(S6)
(S7)
(S8)
(S9)
(S10)
(S11)
(S12)
(S13)
(S14)
(S15)
(S16)
(S17)
(S18)
(S21)
A2TP2
A2TP3
A2TP6
A2TP1
A2TP5
A2TP4
U1
J1
LS1

TEST POINT LOCATIONS
(DISPLAY PCA)

Figure 5A-8. Test Points, Display PCA (A2)

Table 5A-8. Display Initialization

A2TP4 DTEST*	A2TP5 LTE*	POWER-UP DISPLAY INITIALIZATION
1	1	All Segments OFF
1	0	All Segments ON (default)
0	1	Display Test Pattern #1
0	0	Display Test Pattern #2

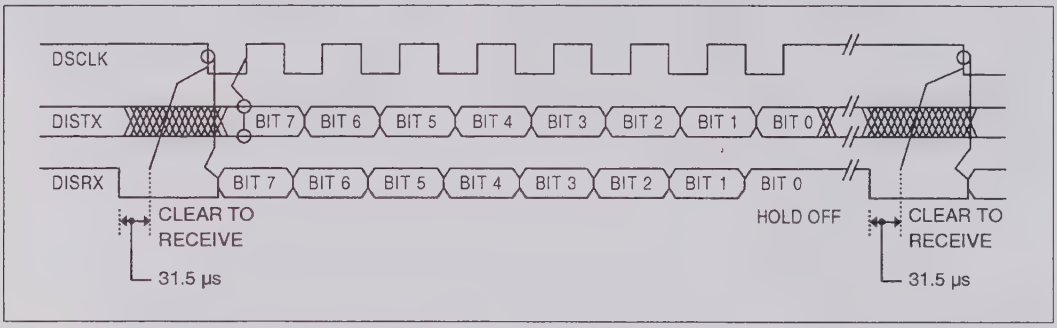

DSCLK
DISTX
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
BIT 0
DISRX
CLEAR TO RECEIVE
31.5 µs
HOLD OFF
CLEAR TO RECEIVE
31.5 µs

Figure 5A-9. Display Controller to Microprocessor Signals

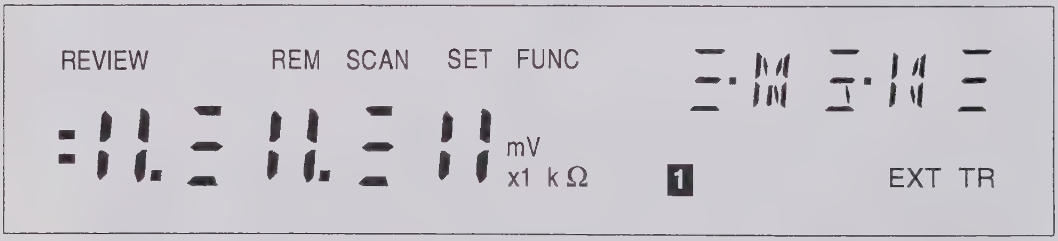

REVIEW
REM
SCAN
SET
FUNC
mV
x1 k Ω
1
EXT TR

Figure 5A-10. Display Test Pattern #1

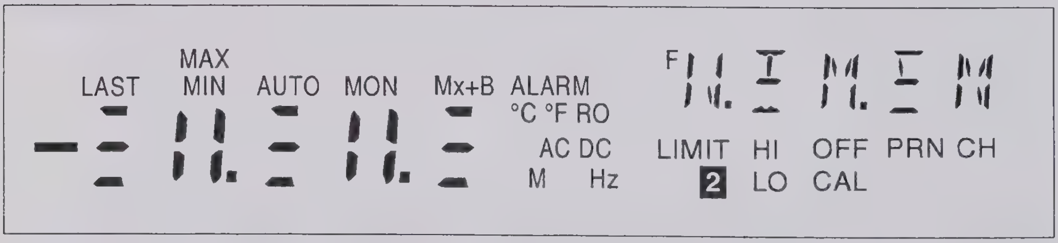

LAST
MAX
MIN
AUTO
MON
Mx+B
ALARM
°C °F RO
AC DC
M Hz
F
LIMIT
HI
OFF
PRN
CH
2
LO
CAL

Figure 5A-11. Display Test Pattern #2

NOTE

If the display is operational but has problems when front-panel buttons are pressed, proceed directly to step 9.

1. Check the three power supplies with respect to GND (A2TP3 or A2U1-42) on the Display Assembly.

VCC (A2U1-21)	4.75 to 5.25V dc
VEE (A2U1-4)	-4.75 to -5.25V dc
VLOAD (A2U1-5)	-28.5 to -32.0V dc

2. Check the filament drive signals FIL1 and FIL2; these connect to the last two pins on each end of A2DS1. These signals should be 5.4V ac with FIL2 biased to be about 6.8V dc higher than the VLOAD supply (nominally a -23.2V dc level). FIL1 and FIL2 should be 180 degrees out of phase. If the dc bias of FIL2 is not at about -23.2V dc, the display segments that should be “off” will show a shadowing (or speckling) effect.
3. Check the clock signal CLK1 at A2TP2, A2U1-2, and A2U4-3. This signal should be a 512-kHz square wave (1.953 microseconds per cycle). This signal depends on an E clock signal (also known as DCLK) of 1.024 MHz from the Main Assembly. If the E clock is not correct, the problem may be in A1U25 or in the ribbon cable system connecting the two assemblies.
4. Check the state of the RESET signal (A2U1-1). This signal should be low once the reset time is completed (after power-up). Also verify that the RESET* signal (A2U6-3) is high after the reset time is completed.
5. Verify that the DISRX signal (A2U1-39) goes low after RESET (A2U1-1) goes low. If this sequence does not occur, communication to the Microprocessor is held off with the DISRX signal high. If DISRX stays high but is not shorted to VCC, A2U1 must be faulty.
6. Verify activity for both the DISTX and DSCLK signals. These signals are driven by the Microprocessor and must be transitioning for the Display Controller to receive commands from the Microprocessor.
7. If all segments of a particular digit do not turn on at power-up, the grid drive from A2U1 may not be connected properly to A2DS1. Grids are numbered from 10 to 0 (left to right as the display is viewed). For a digit to be enabled, the respective grid drive signals (GRID(10:0)) must be at approximately VCC (4.75 to 5.25V dc.) For a digit to be disabled, the drive must be at VLOAD (-28.5 to -32.0V dc.)
8. If a segment under each of several (or all) grids fails to be turned on (or off) properly, one of the anode drive signals may not be connected properly from A2U1 to A2DS1. When an anode signal is at VCC, and a grid signal is at VCC, the corresponding segment on the display is illuminated.
9. If the Microprocessor has difficulty recognizing front-panel button presses, the switch scanning signals SWR1 through SWR6 should be checked (A1U25-67, A1U25-68, A1U25-71, A1U25-73, A1U25-70, and A1U25-69 respectively). When no switch contacts are being closed, the switch scanning lines should have about 20-kΩ of resistance between each other (through two 10-kΩ pullup resistors to VCC). Unless one of the switches is closed, none of the switch scanning lines should be shorted directly to GND at any time.

VARIATIONS IN THE DISPLAY 5A-19.

Under normal operation, the display presents various combinations of brightly and dimly lit annunciators and digits. However, you may encounter other, random irregularities across different areas of the display under the following circumstances:

- After prolonged periods of displaying the same information.
- If the display has not been used for a prolonged period.

This phenomenon can be cleared by activating the entire display and leaving it on overnight (or at least for several hours). Use the following procedure to keep the display fully lit:

1. With power OFF, press and hold SHIFT, then press power ON.
2. Wait a moment for the instrument to beep, then release SHIFT. The entire display will now stay on until you are ready to deactivate it.
3. At the end of the activation period, press any button on the front panel; the instrument resumes the mode in effect prior to the power interruption (Active or Inactive.)

CALIBRATION FAILURES 5A-20.

Introduction 5A-21.

Calibration of Hydra through the computer interface is described in Section 4 of this manual. Generally, a calibration failure is indicated by a Device Dependent Error and a "!>" prompt after a CAL_STEP? command if the RS-232 interface is being used. This occurs if the analog input varies from what the instrument expects to see by more than ±5% or ±15%, depending on the calibration step.

Before suspecting a fault with Hydra, verify that the calibration is being conducted properly.

- Check the connections between the source and the instrument. Are all the connections in place?
- Check the output of the calibration source. Does it equal the value called for by this calibration step?
- Check the calibration source. Is it in operate mode? Has it reverted to standby?

If a calibration step has failed, Hydra remains on that step so that the output from the calibration source may be corrected or the calibration reference value (CAL_REF) being used by Hydra may be changed if it was improperly entered. The calibration step may be repeated by sending the CAL_STEP? command to Hydra again.

Calibration of Hydra utilizes a simple "calibration by function" approach. If you suspect calibration errors, but the instrument does not exhibit the symptoms mentioned above, verify that you are observing the following calibration rules:

- Independent calibration of any function results in the storage of calibration constants for that function only.
- Once calibration is begun, all steps for that function must be completed before the calibration constants are stored. If all steps are not completed and the procedure is terminated, no constants for that function are stored; only calibration constants for previously completed functions are stored.

Calibration-Related Components 5A-22.

If the calibration setup is correct, a faulty component within Hydra may be causing the failure. Each measurement function depends on a combination of components in and around the Analog Measurement Processor (A3U8).

RMS Converter	A3U6
AC Buffer	A3U7
Zener Reference	A3VR1
Divider Network (DC/Ohms)	A3Z4

Integrate Resistors, Reference Divider	A3Z2
AC Divider Network	A3Z3
RMS Converter Network	A3Z1

Basic dc measurements depend on the zener reference (A3VR1), reference divider network (A3Z2), and integrate resistors (A3Z2). Resistance measurements and dc measurements above three volts additionally depend on the resistors in the dc divider network (A3Z4). AC measurements depend on the ac divider network (A3Z3), ac buffer (A3U7), and RMS converter (A3U6), as well as the basic dc measurement components.

NOTE

During calibration, the measurement rate is selected automatically as required by the calibration step.

Table 5A-9 may be useful in isolating a calibration problem to specific components.

Table 5A-9. Calibration Faults (for software versions 5.4 and above)

INPUT	RANGE	CALIBRATION CONSTANT		RELATED COMPONENTS
		NUMBER	ACCEPTABLE VALUES	
DC VOLTS				
0.09000V	100 mV	1	1.0315 to 1.1565	A3VR1, A3Z2
0.9000V	1V	2	1.0340 to 1.1540	A3VR1, A3Z2
0.29000V	300 mV	3	1.0315 to 1.1565	A3VR1, A3Z2
2.9000V	3V	4	1.0315 to 1.1565	A3VR1, A3Z2
29.000V	30V	5	1.0340 to 1.1640	A3VR1, A3Z2, A3Z4
290.00V	300V	6	1.0290 to 1.1590	A3VR1, A3Z2, A3Z4
AC VOLTS (1 kHz)				
0.02900V	300 mV	7	-0.001 to 0.001	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
0.29000V	300 mV	8	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
0.2900V	3V	9	-0.01 to 0.01	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
2.9000V	3V	10	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
2.900V	30V	11	-0.1 to 0.1	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
29.000V	30V	12	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
29.00V	300V	13	-1.0 to 1.0	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
290.00V	300V	14	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
OHMS				
290.00Ω	300Ω	15	0.9965 to 1.0115	A3Z2, A3Z4
2.9000 kΩ	3 kΩ	16	0.9975 to 1.0125	A3Z2, A3Z4
29.000 kΩ	30 kΩ	17	1.0015 to 1.0165	A3Z2, A3Z4
290.00 kΩ	300 kΩ	18	0.9965 to 1.0115	A3Z2, A3Z4
2.9000 MΩ	3 MΩ	19	0.9990 to 1.0090	A3Z2, A3Z4
2.9000 MΩ	10 MΩ	20	0.9990 to 1.0090	A3Z2, A3Z4
FREQUENCY				
10.000 kHz 2.9V rms		21	0.9995 to 1.0005	A3Y2

Retrieving Calibration Constants 5A-23.

If a calibration error is suspected, the stored constant can be retrieved and verified over the computer interface. Acceptable calibration constants for each function and range are listed in Table 5A-9. Retrieve the constant with the following command:

CAL_CONST? xx (where xx denotes the calibration constant number)

The entire calibration of the Hydra Databucket can be retrieved from the instrument in tabular form by using the following command:

EEM_LIST?

The instrument response from this command shows the currently used FLASH memory block and page numbers, and each calibration constant in hexadecimal and floating point with a description of what function and range each calibration constant is used on. The following is a sample of a typical EEM_LIST? response:

```
Page 10 of Parameter Block 1 is currently in use.
Register    Hex Value     F.P. Value      Description
---------------------------------------------------------------
  0-1       0x3F8A847A    1.0821679    100 Millivolt DC Gain
  2-3       0x3F8A5D75    1.0809771    1 Volt DC Gain
  4-5       0x3F8A6357    1.0811566    300 Millivolt DC Gain
  6-7       0x3F8A5BC0    1.0809250    3 Volt DC Gain
  8-9       0x3F8B4F57    1.0883588    30 Volt DC Gain
 10-11      0x3F8A7C8A    1.0819256    150/300 Volt DC Gain
 12-13      0xB8F20A00   -0.0001154    300 Millivolt AC Offset
 14-15      0x3F8A5119    1.0805999    300 Millivolt AC Gain
 16-17      0xBA974800   -0.0011542    3 Volt AC Offset
 18-19      0x3F8A7F29    1.0820056    3 Volt AC Gain
 20-21      0xBC3A6C00   -0.0113783    30 Volt AC Offset
 22-23      0x3F8A863A    1.0822213    30 Volt AC Gain
 24-25      0xBDE81400   -0.1133194    150/300 Volt AC Offset
 26-27      0x3F8AC886    1.0842445    150/300 Volt AC Gain
 28-29      0x3F808EAB    1.0043539    300 Ohm Gain
 30-31      0x3F809759    1.0046188    3 Kilo Ohm Gain
 32-33      0x3F80FD78    1.0077353    30 Kilo Ohm Gain
 34-35      0x3F7FF46C    0.9998233    300 Kilo Ohm Gain
 36-37      0x3F7FFDD0    0.9999666    3 Mega Ohm Gain
 38-39      0x3F7FFDD0    0.9999666    10/30 Mega Ohm Gain
 40-41      0x3F80073D    1.0002209    Frequency Gain
 42         0x000F                     Calibration Status
 43-44      0xAAAAAAAA                 Product Serial Number
 45         0xFFFF                     Unused EEM Register #1
 46         0xFFFF                     Unused EEM Register #2
 47         0xFFFF                     Unused EEM Register #3
 48         0x62F4                     CRC of EEM Data (0x62F4)
```

Replacing the FLASH Memory (A1U14 and A1U16) 5A-24.

The FLASH Memory provides nonvolatile storage for the instrument serial number, the instrument firmware, and all calibration information. If the “boot” firmware in FLASH memory has been determined to be faulty, A1U14 and A1U16 must both be replaced. Many other problems may be corrected by loading new instrument firmware in the instrument (see the section entitled “Updating the 2635A Instrument Firmware” in Section 4 of this manual), or recalibrating the instrument.

If the FLASH Memories must be replaced during repair, the instrument must be recalibrated. The new FLASH Memory can be programmed with the 7-digit serial number found on the rear panel of the instrument or any 7-digit identifier of your choosing. Note that the serial number is not programmed prior to shipment from the factory.

The following command may be used to program the serial number into the FLASH Memory:

SERIAL XXXXXXX (xxxxxxx denotes the 7-digit number. Leading zeros must be entered. Note: once entered, the number cannot be changed.)

The serial number of the instrument can be accessed by using the "SERIAL?" command. The response will be "0" (if the serial number has not yet been set) or the 7-digit serial number.

MEMORY CARD INTERFACE ASSEMBLY (A6) TROUBLESHOOTING 5A-25.

Power-Up Problems 5A-26.

The following discussion identifies probable fault areas if the installation of a Memory Card Interface Assembly PCA causes power-up failure for the instrument. The problem is probably a short on A6P2; the Microprocessor on the Main Assembly is prevented from accessing Flash Memory and NVRAM correctly. Make the following checks:

- First check for a GND-to-VCC short on the Memory Card Interface Assembly PCA.
- There may also be a short between an interface signal and VCC, GND, or another interface signal. Check signals D8 .. D15, A1 .. A4, XRDU*, XWRU*, XMCARD*, XSCLK, DTACK*, MCINT*, and RESET*.
- The short may be due to a CMOS input that has been damaged due to static discharge; the short is then detectable only when the circuit is powered up. Use an oscilloscope to check activity on each of the interface signals. Verify that signals are able to transition normally between 0 and 5.0V dc (VCC).

FAILURE TO DETECT MEMORY CARD INTERFACE PCA 5A-27.

If the Memory Card Interface is not installed properly, an "ERROR d" is displayed during power-up. The Microprocessor checks for the presence of the Memory Card Interface by attempting to read one of the registers in the Memory Card Controller (A6U1). If A6U3-19 fails to drive the DTACK* signal low during the read access, the Microprocessor will abort the memory cycle and report the Memory Card Interface as being not installed.

Verify the RESET*, XMCARD*, XRDU*, XSCLK, DTACK* and WAIT* signals on the Memory Card Interface. RESET* (A6U1-33) must be high and WAIT* (A6U3-5) must be high. Using a storage oscilloscope, verify that DTACK* (A6U3-19) goes low while MCARD* (A6U3-3) is low for the first read memory cycle to the Memory Card Controller (A6U1) during instrument power-up. It may be necessary to cycle the power on the instrument several times to verify this operation.

FAILURE TO DETECT INSERTION OF MEMORY CARD 5A-28.

When a Memory Card is inserted into the Memory Card Interface, the card detect signals (CD1 and CD2; A6U1-40 and A6U1-38) are driven low. Verify that the Memory Card Controller detects this and interrupts the Microprocessor (A1U1) by driving the MCINT* signal (A6U1-112) low. Failure to generate the interrupt may be due to problems with the data bus (D8..D15), the address bus (A1..A4), or one of the control signals (XSCLK, XMCARD*, XWRU*, XRDU*, and RESET*). Consult the schematics found in Section 8 of this manual and verify these interconnections. Consider the ribbon cable that connects the Main Assembly (A1) to the Memory Card Interface Assembly (A6) as a possible source of the problem as well. It may be necessary to repeatedly insert and remove the card to observe the behavior of these signals.

FAILURE TO POWER CARD / ILLUMINATE THE BUSY LED 5A-29.

When a Memory Card is properly inserted and then detected by the Microprocessor (A1U1), the Memory Card should be powered up and the BUSY LED should be illuminated for a short period of time. If the BUSY LED is not visibly illuminated when the card is inserted, verify the following things using a storage oscilloscope. Verify that the gate of transistor A6Q1 is driven low by A6U1-102 (check both ends of resistor A6R13). When the gate of A6Q1 is near 0 volts dc, the drain of transistor (A6Q1-5 through A6Q1-8) should be near 5 volts dc.

Approximately 50 milliseconds after transistor drain (A6Q1-5 through A6Q1-8) goes to about 5 volts dc, the BUSY LED should be turned on by A6U1-119 going low to sink current through the LED (A6DS1) and current-limiting resistor (A6R10). When the Microprocessor (A1U1) is done accessing data on the memory card, A6U1-119 and A6U1-102 will both go high again to turn off the BUSY LED and the card power supply. If the 50-millisecond delay between the memory card power being turned on and the BUSY LED being turned on may be extended up to a total of 250 milliseconds if the RDY/BSY signal (A6U1-66) is being held low by the memory card.

FAILURE TO ILLUMINATE THE BATTERY LED 5A-30.

The yellow BATTERY LED is controlled by a Memory Card Controller output (A6U1-18). The Microprocessor checks the BVD1 and BVD2 outputs (A6U1-96 and A6U1-95 respectively) from the memory card about 50 milliseconds after it is powered up. The BATTERY LED is turned on by A6U1-118 going low to sink current through the LED (A6DS2) and current-limiting resistor (A6R11). Verify that the BATTERY LED state matches the state of the BVD1 and BVD2 signals as shown in the following table (H = 5 volts dc, L = 0 volts dc).

BATTERY LED	BVD1	BVD2
OFF	H	H
ON	H	L
ON	L	H
ON	L	L

FAILURE TO WRITE TO MEMORY CARD 5A-31.

The installed memory card controls the state of the write protect (WP) signal that is an input to the Memory Card Controller (A6U1-97). This signal must be near 0 volts dc when the memory card is powered up and any operation requiring write access to the memory card is done. Verify that the state of the WP signal (A6U1-97) correctly follows the state of the write protect switch on the memory card as indicated in the following table (H = 5 volts dc, L = 0 volts dc).

WRITE PROTECT	WP (A6U1-97)
Enabled	H
Disabled	L

If the problem with the interface has not been isolated yet, the problem is probably in the card address (CA<0> .. CA<25>, REG*), card data (CD<0> .. CD<15>), and control signals (CE1*, CE2*, CRD*, CWR*). The card data (CD<0> .. CD<15>) signals each go through a series termination resistor (A6R8, A6R9, A6Z2, A6Z3) so verify these series resistances. The control signals (CE1*, CE2*, CRD*, CWR*) each go from the Memory Card Controller (A6U1) through an analog switch (A6U2) as they go to the Memory Card Connector (A6P1), so verify that each control signal functions properly. There are two card enable signals (CE1* and CE2*): one for even numbered bytes and the other for odd numbered bytes. The card read (CRD*) and card write (CWR*) signals must go low for read and write cycles respectively. The following table describes the memory card access modes to “attribute” memory (only read accesses are done by the instrument).

“Attribute” Memory Card Access Modes

FUNCTION MODE	REG*	CE2*	CE1*	CA0	CRD*	CWR*	D15-D8	D7-D0
Even Byte Read	L	H	L	L	L	H	xxx	Even
Odd Byte Read	L	H	L	H	L	H	xxx	Odd
Word Read	L	L	L	x	L	H	Odd	Even
Odd Byte Read	L	L	H	x	L	H	Odd	xxx

The following table describes the memory card access modes to “common” memory (Static RAM memory on the type of memory cards used by this instrument).

“Common” Memory Card Access Modes

FUNCTION MODE	REG*	CE2*	CE1*	CA0	CRD*	CWR*	D15-D8	D7-D0
Even Byte Read	H	H	L	L	L	H	xxx	Even
Odd Byte Read	H	H	L	H	L	H	xxx	Odd
Word Read	H	L	L	x	L	H	Odd	Even
Odd Byte Read	H	L	H	x	L	H	Odd	xxx
Even Byte Write	H	H	L	L	H	L	xxx	Even
Odd Byte Write	H	H	L	H	H	L	xxx	Odd
Word Write	H	L	L	x	H	L	Odd	Even
Odd Byte Write	H	L	H	x	H	L	Odd	xxx

WRITE / READ MEMORY CARD TEST (DESTRUCTIVE) 5A-32.

The instrument has a special computer interface command that may be used gain diagnostic information about what is failing to function correctly in the Memory Card Interface.

WARNING

USE OF THE FOLLOWING COMMAND WILL DESTROY ANY DATA STORED ON THE MEMORY CARD THAT IS INSTALLED IN THE INSTRUMENT. AFTER COMPLETION OF THE TROUBLESHOOTING AND REPAIR OF THE MEMORY CARD INTERFACE, THE MEMORY CARD USED MUST BE FORMATTED AGAIN BEFORE IT CAN BE USED AGAIN FOR DATA STORAGE.

To make use of this command, connect a terminal or computer to the RS-232 interface and set the instrument communication parameters as follows:

- Press SHIFT - LIST.
- With ‘BAUd’ displayed, use the UP or DOWN arrow key to select the desired baud rate. Then press ENTER.
- With ‘PAR’ (parity) displayed, use the UP or DOWN arrow key to select the parity. Then press ENTER.
- With ‘CtS’ (Clear to Send) displayed, use the UP or DOWN arrow key to select ‘OFF’. Then press ENTER.
- With ‘ECHO’ displayed, use the UP or DOWN arrow key to select ‘ON’. Then press ENTER. Communications setup for Hydra is now complete.

Assuming that the RS-232 interface is functional, send a carriage return or line feed character to the instrument and it should send back a prompt. With a Static RAM memory card installed in the instrument, send the following command followed by a carriage return or line feed:

MCARD_DESTRUCTIVE_TEST? <size>	where the <size> parameter is the number of kbytes (1024 bytes) of the card to test. Use <size> = 256 for a 256 kbyte card and <size> = 1024 for a 1 Mbyte card.

This command writes data to the memory card and then reads and compares the data to the pattern that was written. A maximum of 20 lines of output will be generated, but all locations on the card are sequentially written and then read. The messages output by this command are summarized below:

```
MEMORY CARD IS NOT INSERTED!
```

The Memory Card Controller doesn’t recognize that the memory card is inserted in connector A6P1. Verify that A6U1-38 and A6U1-40 are both near 0 volts dc.

```
MEMORY CARD IS WRITE PROTECTED!
```

The Memory Card Controller is indicating that the memory card is write protected. Verify that the switch on the rear edge of the memory card is in the proper position and that A6U1-97 is near 0 volts dc when the memory card is powered up.

```
MEMORY CARD TEST PASSED.
```

The memory card test passed without detecting any errors.

```
ADDRESS 0x000000: DATA WAS 0x14, EXPECTED 0xC9
ADDRESS 0x000001: DATA WAS 0x3D, EXPECTED 0x2D
ADDRESS 0x000002: DATA WAS 0xAB, EXPECTED 0xBD
```

These are typical errors indicating in hexadecimal the address, the data that was read from the card and the data that was expected. It may be possible to get some indication of which address or data signals to probe with an oscilloscope to determine where the fault is.

When probing signals to detect activity, it may be useful to change the <size> parameter to be 16384 so that it will attempt to test the card as if it is a 16-Mbyte memory card. This guarantees that error messages will be output, but it will take longer to complete the test, thus allowing more time to probe signals before having to send the memory card test command again.

Section 6

List of Replaceable Parts

TABLE OF CONTENTS

ASSEMBLY NAME	DRAWING NO.	TABLE		FIGURE	
		NO.	PAGE	NO.	PAGE
2620A/2625A Final Assembly	2620A/2625A	6-1	6-6	6-1	6-8
2635A Final Assembly	2635A	6-2	6-12	6-2	6-13
2620A/2625A A1 Main PCA	2620A-4001	6-3	6-17	6-3	6-20
2635A A1 Main PCA	2635A-4001	6-4	6-21	6-4	6-24
A2 Display PCA	2620A-4002	6-5	6-25	6-5	6-26
A3 A/D Converter PCA	2620A-4003	6-6	6-27	6-6	6-29
A4 Analog Input PCA	2620A-4004	6-7	6-30	6-7	6-31
A5 (Option -05) IEEE-488 Interface PCA	2620A-4005	6-8	6-32	6-8	6-33
2625A A6 Memory PCA	2625A-4006	6-9	6-34	6-9	6-35
2635A A6 Memory Card I/F PCA	2635A-4006	6-9	6-36	6-9	6-37

INTRODUCTION 6-1.

This section contains an illustrated list of replaceable parts for the 2620A, 2625A, and 2635A. Parts are listed by assembly; alphabetized by reference designator. Each assembly is accompanied by an illustration showing the location of each part and its reference designator. The parts lists give the following information:

- Reference designator
- An indication if the part is subject to damage by static discharge
- Description
- Fluke stock number
- Manufacturers supply code (code-to-name list at the end of this section)
- Manufacturers part number or generic type
- Total quantity
- Any special notes (i.e., factory-selected part)

CAUTION

A ϟ symbol indicates a device that may be damaged by static discharge.

HOW TO OBTAIN PARTS 6-2.

Electrical components may be ordered directly from the manufacturer by using the manufacturers part number, or from the Fluke Corporation and its authorized representatives by using the part number under the heading FLUKE STOCK NO. In the U.S., order directly from the Fluke Parts Dept. by calling 1-800-526-4731. Parts price information is available from the Fluke Corporation or its representatives. Prices are also available in a Fluke Replacement Parts Catalog which is available on request.

In the event that the part ordered has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions, if necessary.

To ensure prompt delivery of the correct part, include the following information when you place an order:

- Part number and revision level of the pca containing the part.
- Reference designator
- Fluke stock number
- Description (as given under the DESCRIPTION heading)
- Quantity
- Instrument Model, Serial Number, and Firmware Numbers

NOTE

*Instrument Firmware Numbers can be retrieved over the computer interface using the *IDN? query. Refer to Section 4 of the Hydra Users Manual for more information.*

MANUAL STATUS INFORMATION 6-3.

The Manual Status Information table that precedes the parts list defines the assembly revision levels that are documented in the manual. Revision levels are printed on the component side of each pca.

NEWER INSTRUMENTS 6-4.

Changes and improvements made to the instrument are identified by incrementing the revision letter marked on the affected pca. These changes are documented on a supplemental change/errata sheet which, when applicable, is included with the manual.

SERVICE CENTERS 6-5.

A list of service centers is located at the end of this section.

NOTE

This instrument may contain a Nickel-Cadmium battery. Do not mix with the solid waste stream. Spent batteries should be disposed of by a qualified recycler or hazardous materials handler. Contact your authorized Fluke service center for recycling information.

WARNING

THIS INSTRUMENT CONTAINS TWO FUSIBLE RESISTORS (PN 650085). TO ENSURE SAFETY, USE EXACT REPLACEMENT ONLY.

Manual Status Information

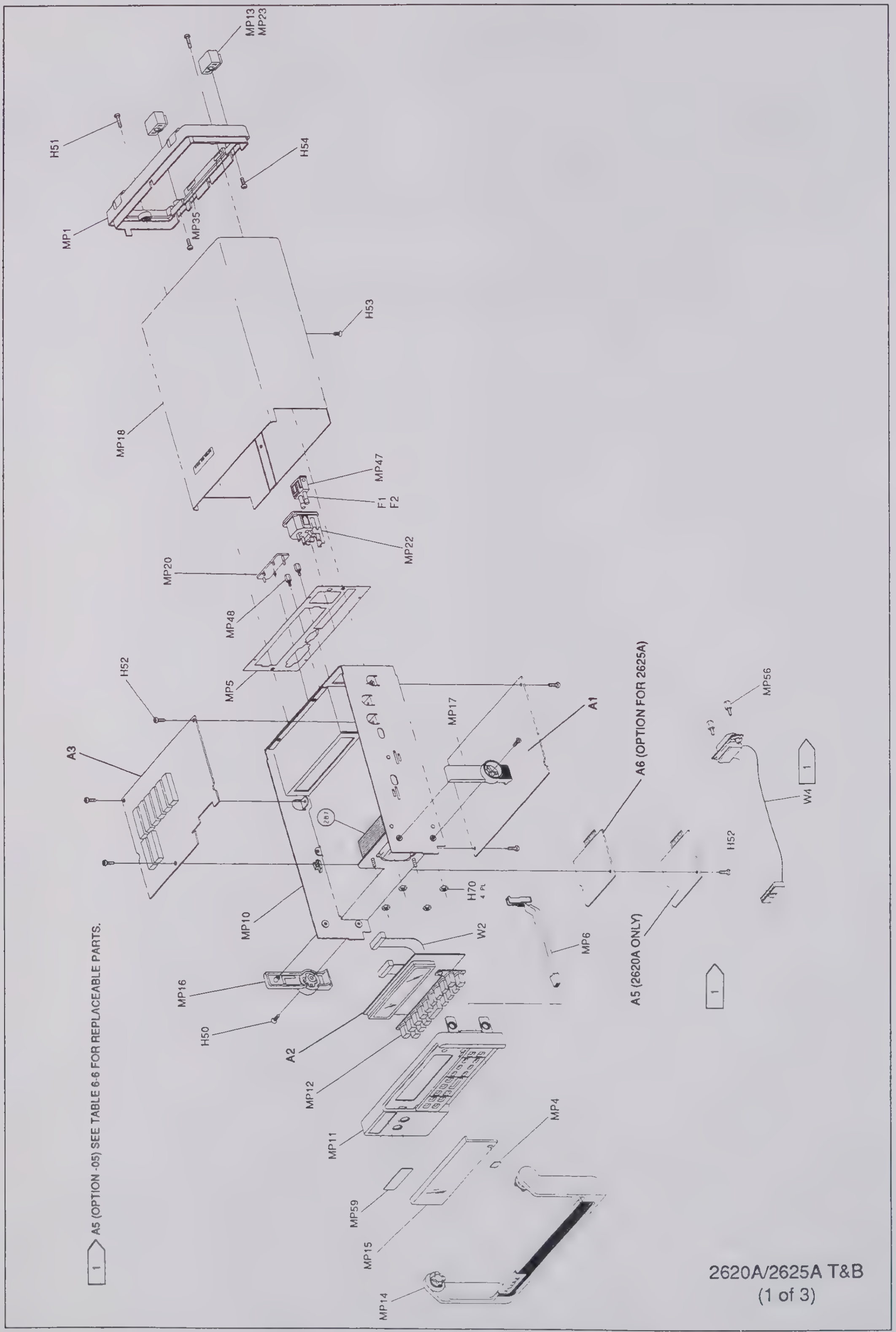
REF. OR OPTION NO.	ASSEMBLY NAME	FLUKE PART NO.	REVISION
A1	2620A/2625A Main PCA	814186	D
A1	2635A Main PCA	925669	A
A2	Display PCA	814194	-
A3	A/D Converter PCA	814202	E
A4	Analog Input PCA	814210	B
A5	IEEE-488 Interface PCA	872593	A
A6	2625A Memory PCA	886135	A
A6	2635A Memory Card I/F PCA	931977	A

Table 6-1. 2620A/2625A Final Assembly

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
A 1	MAIN PCA	814186	89536	814186	1	
A 2	DISPLAY PCA	814194	89536	814194	1	
A 3	A/D CONVERTER PCA	814202	89536	814202	1	
A 4	ANALOG INPUT PCA	814210	89536	814210	1	
A 5	IEEE-488 INTERFACE PCA	872593	89536	872593	1	3
A 6	MEMORY PCA	886135	89536	886135	1	1
F 1, 2	FUSE,5X20MM,0.125A,250V,SLOW	822254	71400	GDC-125MA	2	
H 50	SCREW,FH,P,LOCK,STL,8-32,.375	114116		COMMERCIAL	2	
H 51	SCREW,PH,P,LOCK,SS,6-32,.375	334458		COMMERCIAL	2	
H 52	SCREW,PH,P,LOCK,STL,6-32,.250	152140		COMMERCIAL	6	
H 53	SCREW,FHU,P,LOCK,SS,6-32,.250	769893		COMMERCIAL	1	
H 54	SCREW,TH,P,SS,4-40,.187	721118		COMMERCIAL	2	
H 65	SCREW,KNURL,SL,CAPT,STL,6-32,.500	876479		COMMERCIAL	2	
H 70	NUT,HEX,STL,6-32	110551		COMMERCIAL	4	
MP 1	BEZEL,REAR	874081	89536	874081	1	
MP 2	ISOTHERMAL CASE,BOTTOM	874107	89536	874107	1	
MP 3	ISOTHERMAL CASE,TOP	874110	89536	874110	1	
MP 5	DECAL,REAR PANEL	874128	89536	874128	1	
MP 6	ROD,POWER SWITCH	784827	89536	784827	1	
MP 10	CHASSIS ASSY	871561	89536	871561	1	
MP 11	FRONT PANEL	795062	89536	795062	1	
MP 12	ELASTOMERIC KEYPAD	795070	89536	795070	1	
MP 13, 23	CASE,FOOT, BLACK	824433	89536	824433	2	
MP 14	HANDLE,PAINTED	949511	89536	949511	1	
MP 15	LENS, FRONT PANEL	784777	89536	784777	1	
MP 16	MOUNTING PLATE,HANDLE (LEFT)	884267	89536	884267	1	
MP 17	MOUNTING PLATE,HANDLE (RIGHT)	884270	89536	884270	1	
MP 18	CASE,OUTER	884262	89536	884262	1	
MP 20	COVER,IEEE	885983	89536	885983	1	
MP 22	PWR PLUG,PANEL,6.3A,250V,3 WIRE	780817	61935	KEA4301.0523	1	
MP 25	DECAL,ISOTHERMAL CASE	874131	89536	874131	1	
MP 26	NAMEPLATE	877845	89536	877845	1	2
MP 26	NAMEPLATE	784736	89536	784736	1	1
MP 38	INSERT,SHIPPING CONTAINER	848221	89536	848221	2	
MP 39	CONTAINER,SHIPPING	852384	89536	852384	1	
MP 43	TEST LEAD ASSY, TL70A	855820	89536	855820	1	
MP 47	PWR PLUG PART,FUSE HOLDER	780825	61935	KEA4301.1405	1	
MP 48	CONN ACC,D-SUB,FEMALE SCREWLOCK,.250	844704	55566	4750-2-28	2	
MP 66	TERM STRIP,SOCKET,.197CTR,8 POS	875877	06229	99.241.0401.1	1	
MP 67	TERM STRIP,SOCKET,.197CTR,10 POS	875880	06229	99.240.0401.1	1	
MP 80	HYDRA STARTER SOFTWARE	890645	89536	890645	1	
MP 90	BAG,STATIC SHIELDING,6"X10"	680918	89536	680918	1	
MP 91	BAG,STATIC SHIELDING,3"X5"	680868	89536	680868	1	
MP 99	T/C CABLE,ASSY	871512	89536	871512	1	
MP 101	LABEL,ADHES,VINYL,BAR CODE,1.500,.312	844712	89536	844712	4	
T 1	TRANSFORMER,POWER	931105	89536	931105	1	
TM 1	2620A/2625A MANUAL SET (ENGLISH)	886015	89536	886015	1	5
TM 2	HYDRA STARTER & LABTECH ACQUIRE MAN	890632	89536	890632	1	
TM 3	HYDRA SERVICE MANUAL (WITH DISKS)	889589	89536	889589	0	4
TM 4	HYDRA DATA LOGGER MANUAL	891457	89536	891457	0	4
TM 5	2620A/2625A USER MANUAL (GERMAN)	919220	89536	919220	0	4
TM 6	2620A/2025A USER MANUAL (FRENCH)	885991	89536	885991	0	4
W 1	WIRE ASSY,GROUND	874099	89536	874099	1	

Table 6-1. 2620A/2625A Final Assembly (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
W 1	WIRE ASSY,GROUND	874099	89536	874099	1	
W 2	CABLE ASSY,FLAT,20 COND,MMOD,FERRITE	876185	47001	MICA 20-5.75IN	1	
W 3	CORD,LINE,5-15/IEC,3-18AWG,SVT,5.5 FT	343723	70903	17237	1	
NOTES:	ϟ Static sensitive part. 1. Used on 2625A only. 2. Used on 2620A only. 3. This is an option only. Not available for the 2625A. 4. Available through parts department. 5. Includes: Hydra User Manual (885988), and Hydra Quick Setup Card (895883)					


MP13
MP23
H51
H54
MP1
MP35
H53
MP18
MP47
F1
F2
MP22
MP20
MP48
H52
MP5
A3
MP17
A1
A6 (OPTION FOR 2625A)
MP56
W4
1
261
MP10
H70
4 PL
W2
MP6
A5 (2620A ONLY)
H52
1
MP16
H50
A2
MP12
MP11
MP4
MP59
MP15
MP14
1

A5 (OPTION -05) SEE TABLE 6-6 FOR REPLACEABLE PARTS.

2620A/2625A T&B
(1 of 3)

Figure 6-1. 2620A/2625A Final Assembly

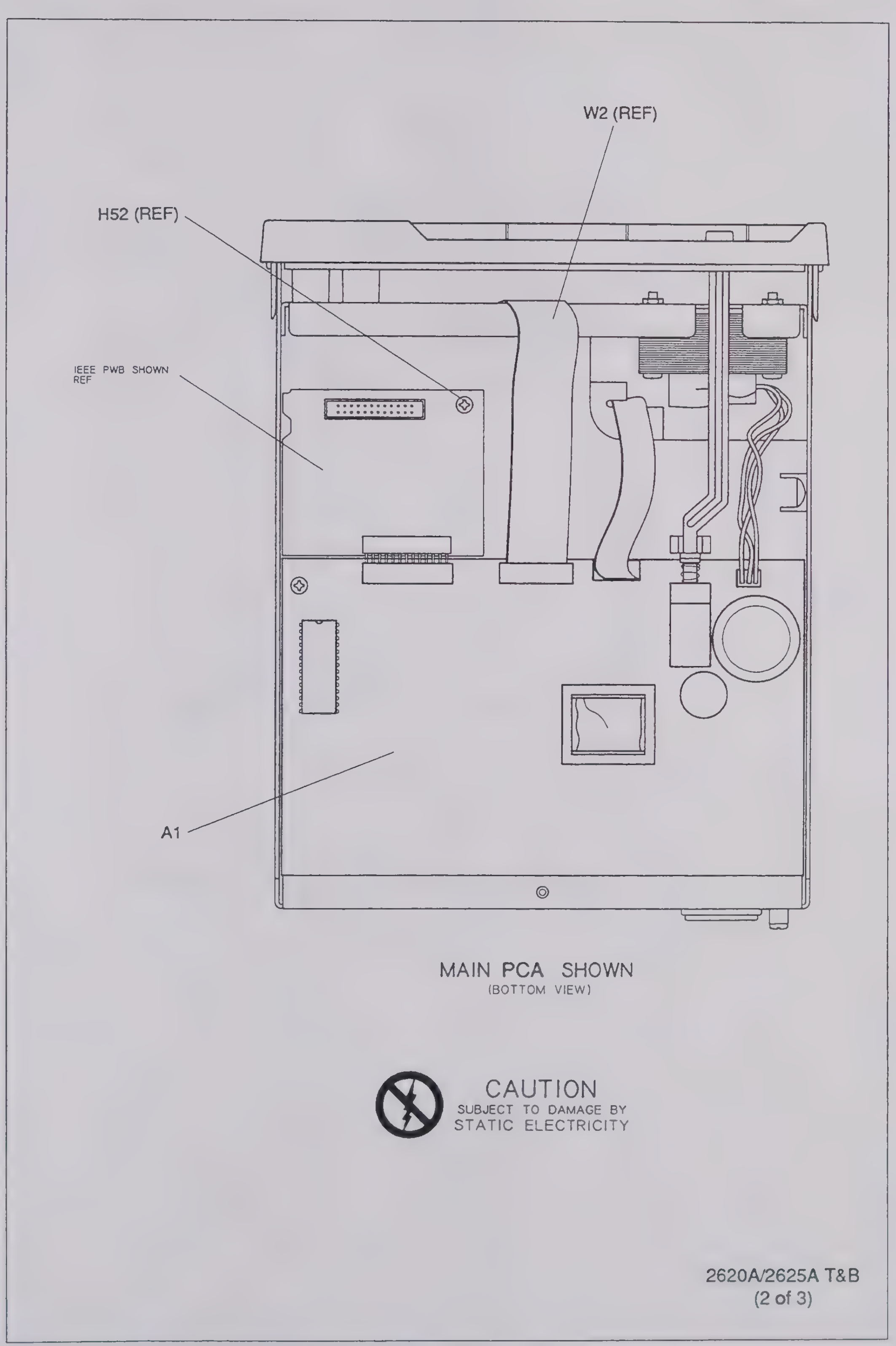
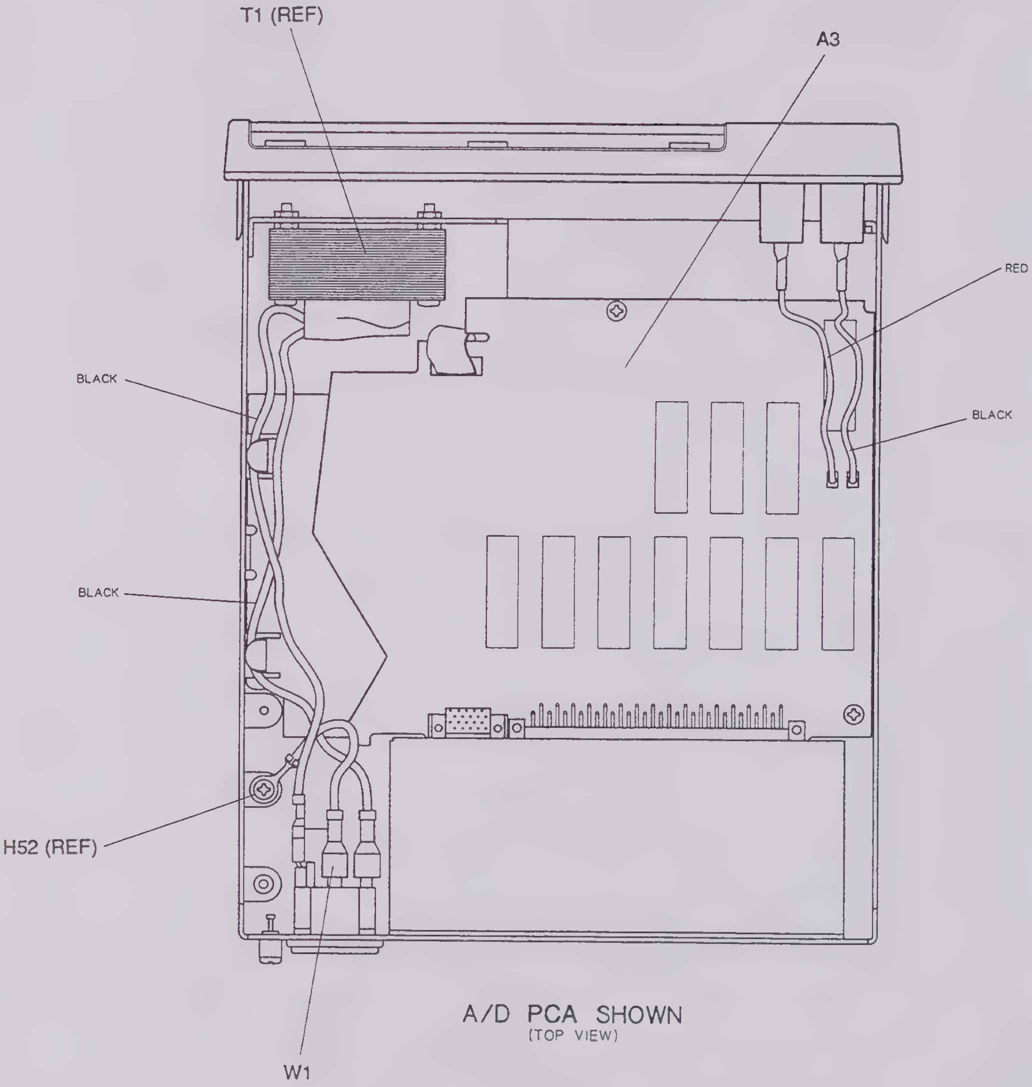

W2 (REF)
H52 (REF)
IEEE PWB SHOWN REF
A1
MAIN PCA SHOWN
(BOTTOM VIEW)
CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY
2620A/2625A T&B
(2 of 3)

Figure 6-1. 2620A/2625A Final Assembly (cont)


T1 (REF)
A3
RED
BLACK
BLACK
BLACK
H52 (REF)
A/D PCA SHOWN
(TOP VIEW)
W1

CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY

2620A/2625A T&B
(3 of 3)

Figure 6-1. 2620A/2625A Final Assembly (cont)

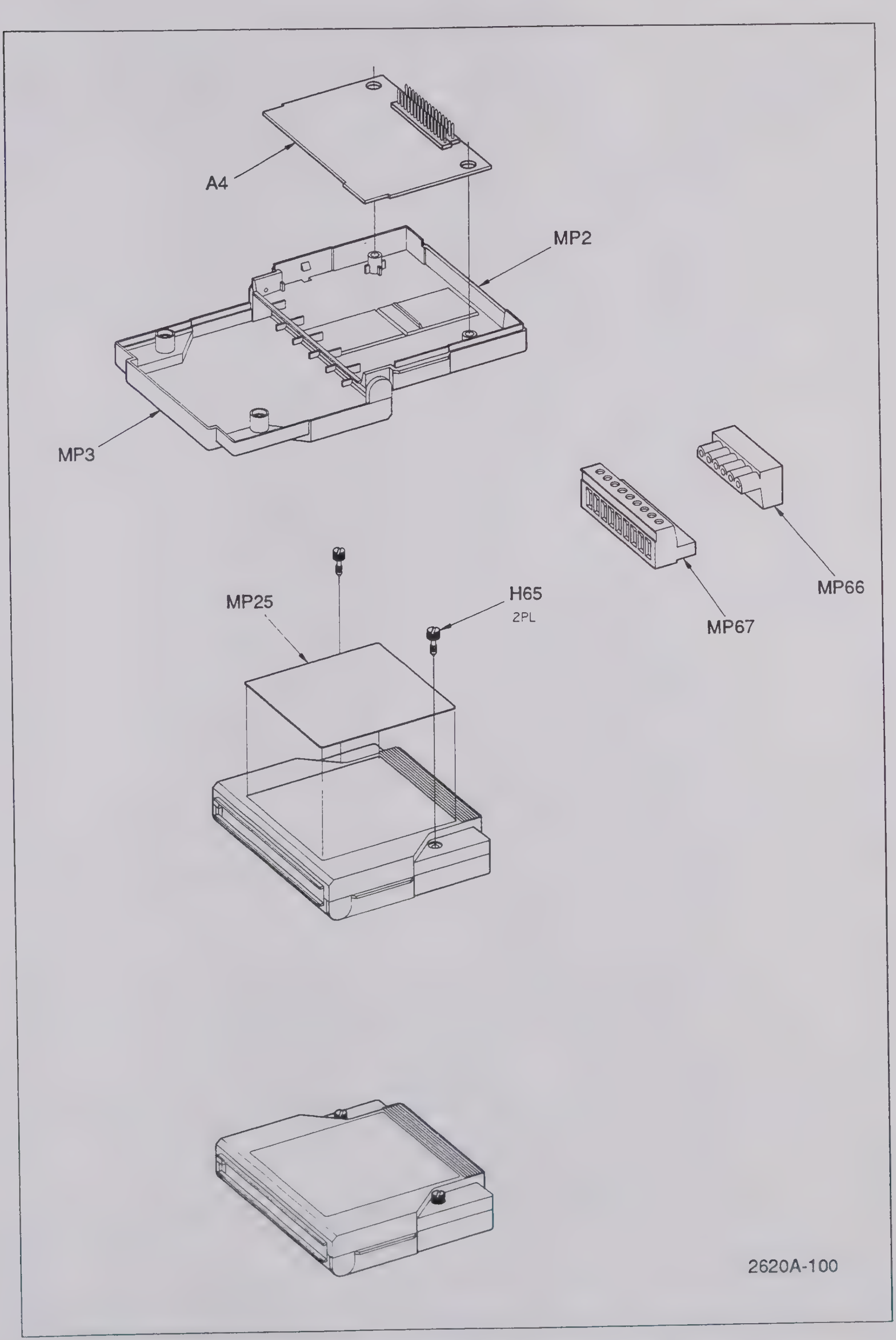

A4
MP2
MP3
MP66
MP67
MP25
H65
2PL
2620A-100

Figure 6-1. 2620A/2625A Final Assembly (cont)

Table 6-2. 2635A Final Assembly

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
A 1	MAIN PCA	925669	89536	925669	1	
A 2	DISPLAY PCA	814194	89536	814194	1	
A 3	A/D CONVERTER PCA	814202	89536	814202	1	
A 4	ANALOG INPUT PCA	814210	89536	814210	1	
A 6	MEMORY CARD I/F PCA	931977	89536	931977	1	
H 50	SCREW,FH,P,LOCK,STL,8-32,.375	114116	74594	114116	2	
H 51	SCREW,PH,P,LOCK,SS,6-32,.500	320051	2M530	320051	2	
H 52	SCREW,PH,P,LOCK,STL,6-32,.250	152140	74594	152140	8	
H 53	SCREW,FHU,P,LOCK,SS,6-32,.250	769893	73734	6-32X1/4FHUCPS2A	1	
H 54	SCREW,TH,P,SS,4-40,.187	721118	89536	721118	2	
H 65	SCREW,KNURL,SL,CAPT,STL,6-32,.500	876479	89536	876479	2	
H 70	NUT,HEX,STL,6-32	110551	73734	70253	4	
H 140	SCREW,PH,P,THD CUT,SS,4-24,.250	309948	89536	309948	1	
F 1, 2	FUSE,5X20MM,0.125A,250V,SLOW	822254	71400	GDC-125MA	2	
MP 1	BEZEL,REAR	874081	89536	874081	1	
MP 2	ISOTHERMAL CASE,BOTTOM	874107	89536	874107	1	
MP 3	ISOTHERMAL CASE,TOP	874110	89536	874110	1	
MP 5	DECAL,REAR PANEL	874128	89536	874128	1	
MP 6	ROD,POWER SWITCH	784827	89536	784827	1	
MP 10	CHASSIS ASSY	871561	89536	871561	1	
MP 11	PANEL,FRONT	932058	89536	932058	1	
MP 12	KEYPAD,ELASTOMERIC	932066	89536	932066	1	
MP 13, 23	CASE,FOOT, BLACK	824433	89536	824433	2	
MP 14	HANDLE,PAINTED	848205	89536	848205	1	
MP 15	LENS, FRONT PANEL	784777	89536	784777	1	
MP 16	MOUNTING PLATE,HANDLE (LEFT)	884267	89536	884267	1	
MP 17	MOUNTING PLATE,HANDLE (RIGHT)	884270	89536	884270	1	
MP 18	CASE,OUTER	884262	89536	884262	1	
MP 22	PWR PLUG,PANEL,6.3A,250V,3 WIRE	780817	61935	KEA4301.0523	1	
MP 25	DECAL,ISOTHERMAL CASE	874131	89536	874131	1	
MP 35	DECAL, CSA	864470	89536	864470	1	
MP 43	TEST LEAD ASSY, TL70A	855820	89536	855820	1	
MP 47	PWR PLUG PART,FUSE HOLDER	780825	61935	KEA4301.1405	1	
MP 48	CONN ACC,D-SUB,FEMALE SCREWLOCK,.250	844704	55566	4750-2-28	2	
MP 59	NAMEPLATE	931873	89536	931873	1	
MP 66	TERM STRIP,SOCKET,.197CTR,8 POS	875877	06229	99.241.0401.1	1	
MP 67	TERM STRIP,SOCKET,.197CTR,10 POS	875880	06229	99.240.0401.1	1	
MP 80	HYDRA STARTER SOFTWARE	890645	89536	890645	1	
MP 99	T/C CABLE,ASSY	871512	89536	871512	1	
MP 101	LABEL,ADHES,VINYL,BAR CODE,1.500,.312	844712	89536	844712	4	
MP 102	GROUND STRIP,BECU,SPRING,1.08,.60	927561	52814	187RF8C070-1.08-L-02	2	
MP 112	ϟ CARD,MEMORY,SRAM,BATTERY,68 PIN				1	3
MP 998	COVER,IEEE	885983	89536	885983	1	
T 1	TRANSFORMER,POWER	931105	89536	931105	1	
TM 1	2635A MANUAL SET (ENGLISH)	932160	89536	932160	1	1
TM 2	HYDRA STARTER & LABTECH ACQUIRE MAN	890632	89536	890632	1	
TM 3	HYDRA SERVICE MANUAL	889589	89536	889589	0	2
TM 4	2635A USER MANUAL (FRENCH)	931902	89536	931902	0	2
TM 5	2635A USER MANUAL (GERMAN)	931907	89536	931907	0	2
W 1	WIRE ASSY,GROUND	874099	89536	874099	1	
W 2	CABLE ASSY,FLAT,20 COND,MMOD,FERRITE	876185	47001	MICA 20-5.75IN	1	
W 3	CABLE,MEMORY	931113	89536	931113	1	
W 4	CORD,LINE,5-15/IEC,3-18AWG,SVT,5.5 FT	343723	70903	17237	1	

NOTES:

ϟ Static sensitive part.
1. Includes: Hydra Data Bucket User Manual (931894), and Hydra Quick Setup Card (895883
21 Available through parts department.
3. For 256KB Memory Card order Fluke PN 927512.
For 1 MB Memory Card order Fluke PN 927517.
For 2 MB Memory Card order Fluke PN 944314.

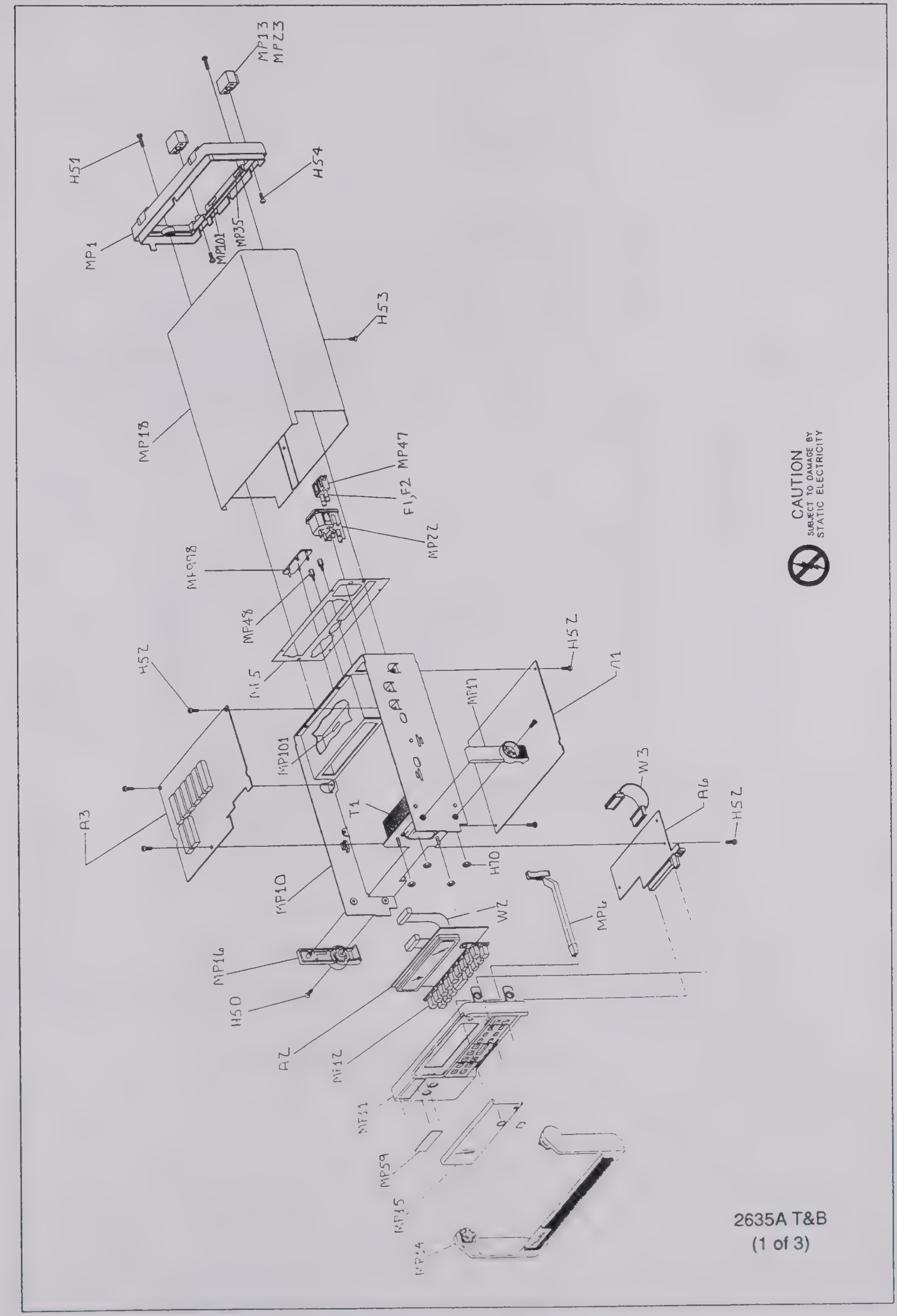

MP13
MP23
H51
H54
MP1
MP101
MP35
H53
MP18
F1,F2
MP47
MP22
MP98
MP48
H52
MP15
MP101
MP17
H52
A1
W3
A6
H52
A3
T1
H70
MP10
W2
MP6
MP16
H50
A2
MP12
MP11
MP59
MP15
MP24
CAUTION
SUBJECT TO DAMAGE BY STATIC ELECTRICITY
2635A T&B
(1 of 3)

Figure 6-2. 2635A Final Assembly

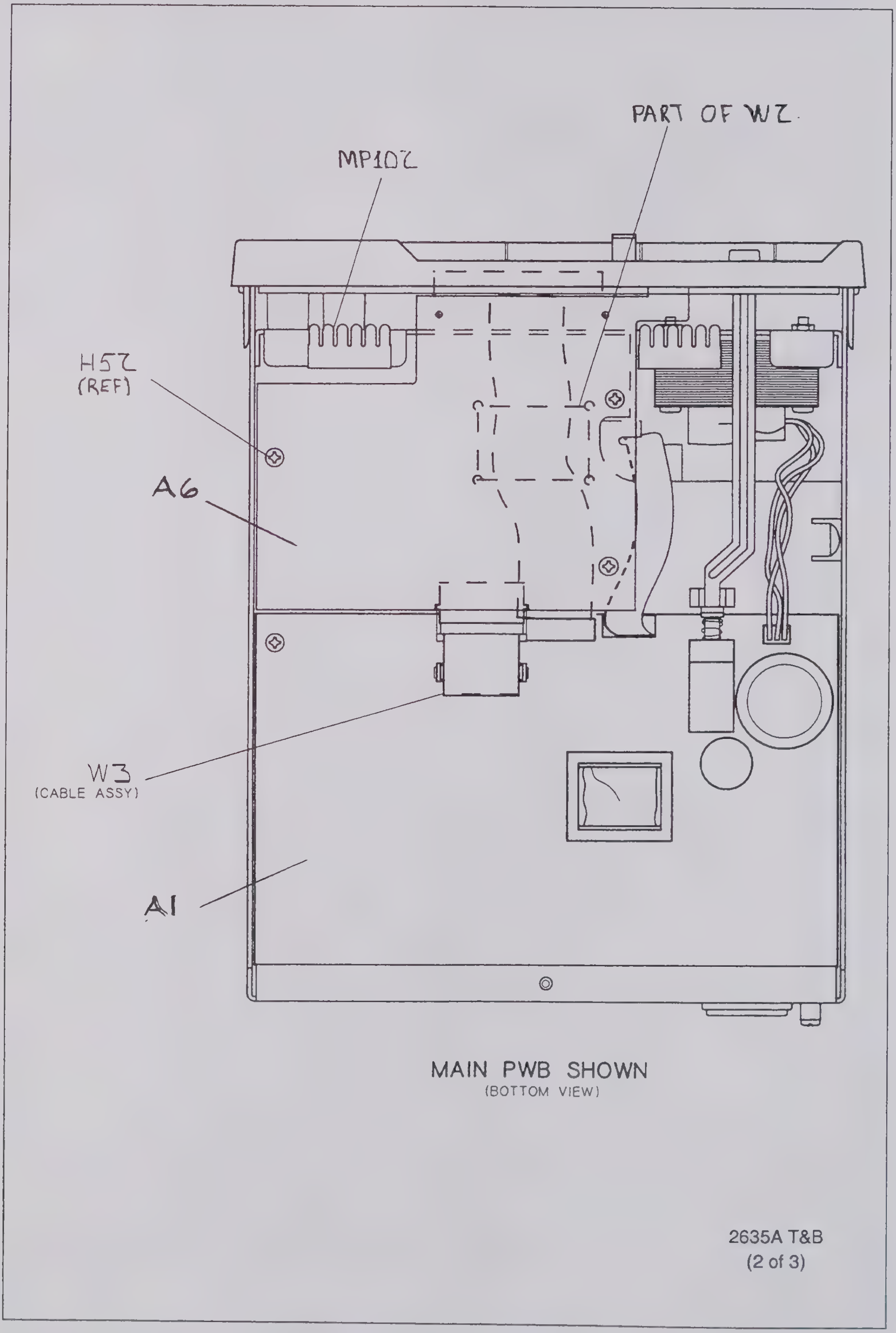

PART OF W2
MP102
H52
(REF)
A6
W3
(CABLE ASSY)
A1
MAIN PWB SHOWN
(BOTTOM VIEW)
2635A T&B
(2 of 3)

Figure 6-2. 2635A Final Assembly (cont)

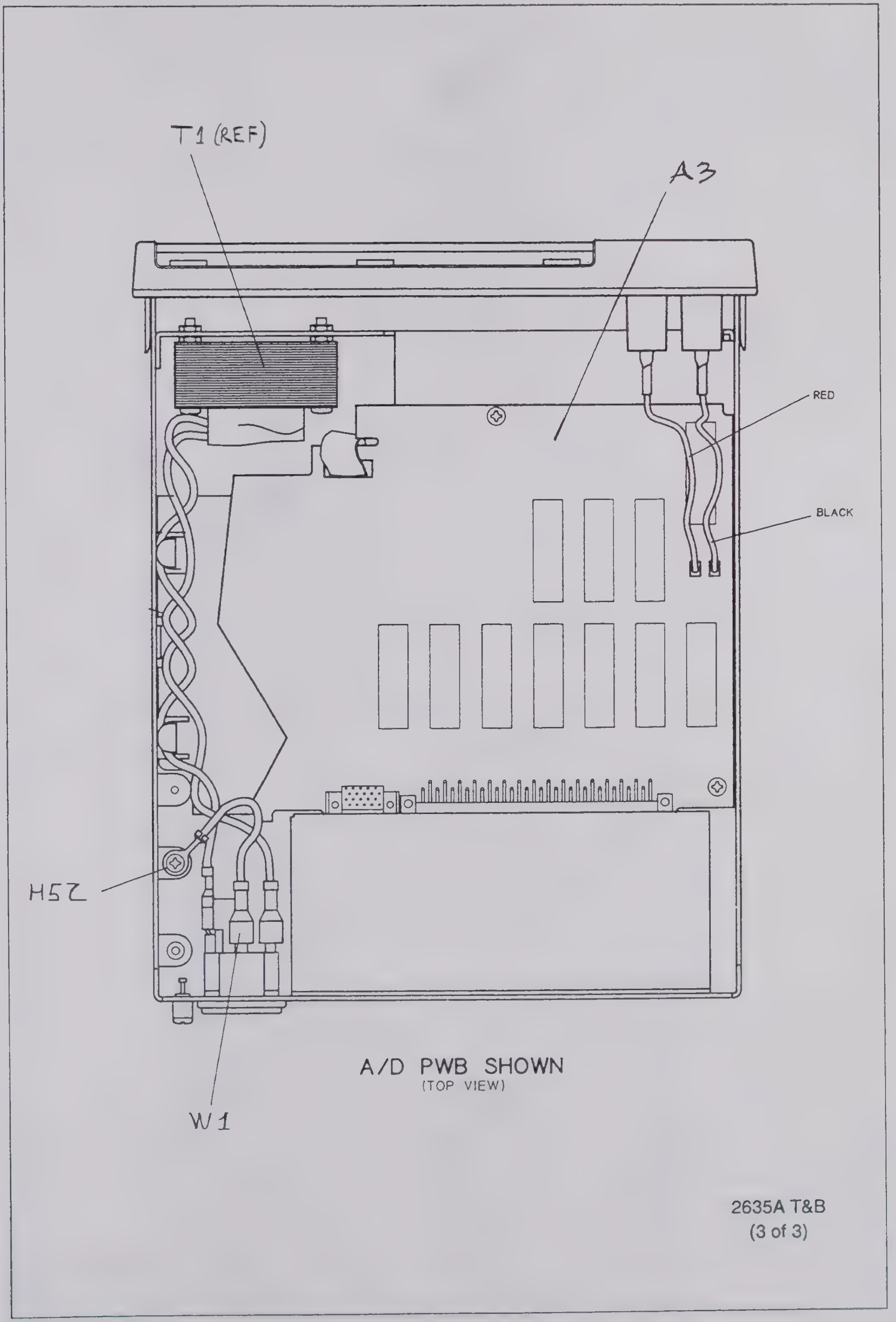

T1 (REF)
A3
RED
BLACK
H52
W1
A/D PWB SHOWN
(TOP VIEW)
2635A T&B
(3 of 3)

Figure 6-2. 2635A Final Assembly (cont)

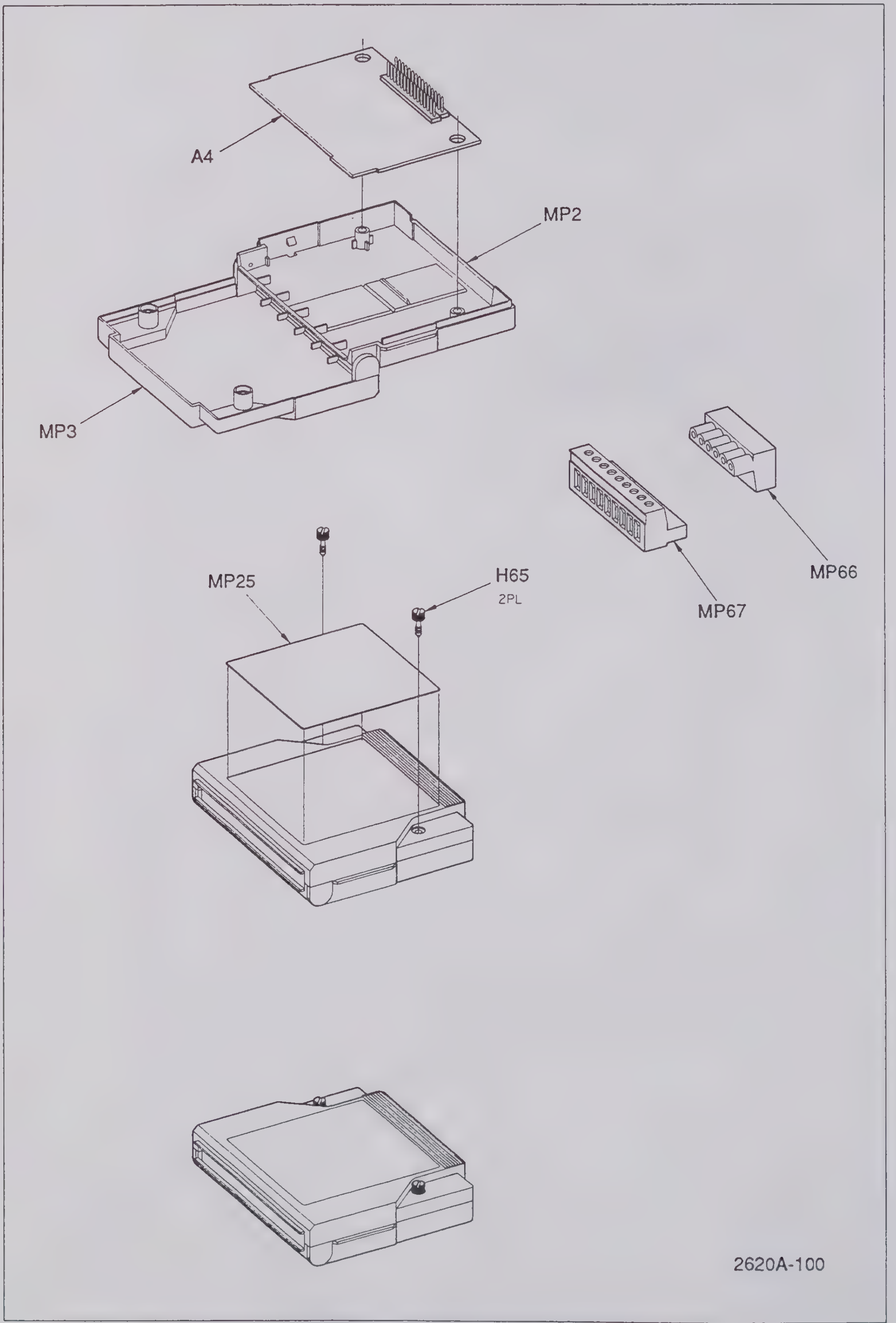

A4
MP2
MP3
MP66
MP67
MP25
H65
2PL
2620A-100

Figure 6-2. 2635A Final Assembly (cont)

Table 6-3. 2620A/2625A A1 Main PCA

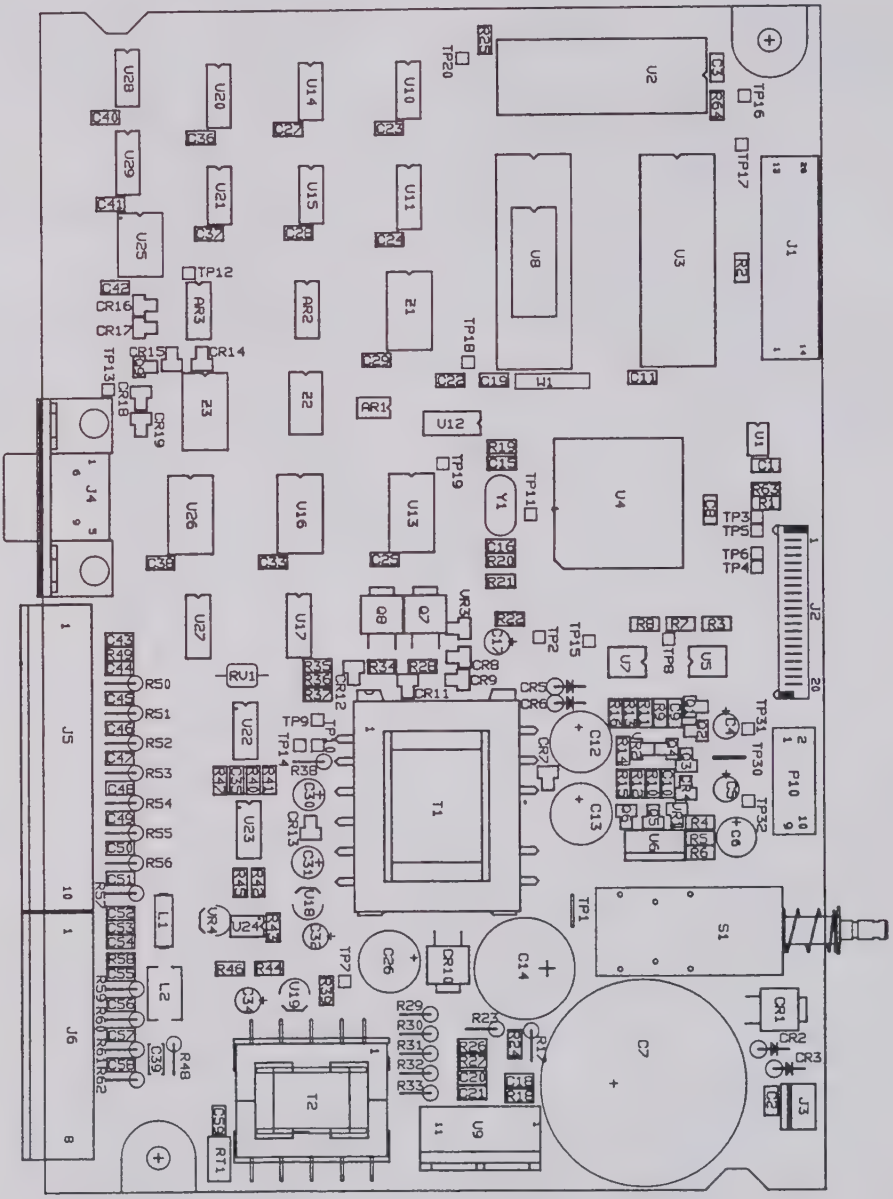
REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
AR 1	ϟ IC,OP AMP,DUAL,LOW POWER,SOIC	867932	6E570	LM358D	1	
AR 2, 3	ϟ IC,OP AMP,QUAD,LOW POWER,SOIC	742569	6E570	LM324D	2	
C 1, 3, 8, C 11, 19, 22- C 25, 27- 29, C 33, 36- 38, C 40- 42	CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287 747287 747287 747287 747287	04222	12065C104KATBA	19	
C 2	CAP,CER,0.033UF,+-20%,100V,X7R,1206	886655	04222	12061C333MATMA	1	
C 4, 5, 32, C 34	CAP,AL,1UF,+-20%,50V,SOLV PROOF	782805 782805	62643	KMA50105M4X7LL	4	
C 6	CAP,AL,10UF,+-20%,63V,SOLV PROOF	816843	62643	KME63T10RM5X11RP	1	
C 7	CAP,AL,10000UF,+-20%,35V,SOLV PROOF	875203	62643	SMH35VN103M35X25LLV	1	
C 9, 10, 43- C 52, 54- 59	CAP,CER,180PF,+-10%,50V,C0G,1206	769778 769778	04222	12065A181KATBA	18	
C 12, 13	CAP,AL,470UF,+-20%,16V,SOLV PROOF	772855	62643	KME16T471M10X12.5MC	2	
C 14	CAP,AL,2200UF,+-20%,10V,SOLV PROOF	875208	62643	LXE10VB222M18X15MC	1	
C 15, 16, 18	CAP,CER,33PF,+-10%,50V,C0G,1206	769240	04222	12065A330KATBA	3	
C 17	CAP,AL,2.2UF,+-20%,50V,SOLV PROOF	769687	62643	KMA50T2R2M45X85LL	1	
C 20	CAP,CER,1800PF,+-10%,50V,C0G,1206	769786	04222	12065A182KATBA	1	
C 21	CAP,CER,820PF,+-5%,50V,C0G,1206	867403	04222	12065A821JATBA	1	
C 26	CAP,AL,47UF,+-20%,100V,SOLV PROOF	837492	62643	KMF100VB47RM10X16MX	1	
C 30, 31	CAP,AL,47UF,+-20%,50V,SOLV PROOF	822403	62643	KME50T47RM6X11RP	2	
C 35, 53	CAP,CER,1000PF,+-5%,50V,C0G,1206	867408	04222	12065A102JATBA	2	
C 39	CAP,CER,0.047UF,+-10%,100V,X7R	844733	04222	SR591C473KAA	1	
CR 1, 10	DIODE,SI,100 PIV,3.3 AMPS,SCHOTTKY	837740	59993	30WQ10F	2	
CR 2, 3	DIODE,SI,600 PIV,1.5 AMP	112383	55464	1N5397	2	
CR 4, 11, 12	ϟ DIODE,SI,BV=75V,IO=250MA,SOT23	830489	25403	BAS16	3	
CR 5, 6	ϟ DIODE,SI,SCHOTTKY BARRIER,40V,1A	837732	04713	MBR140P	2	
CR 7, 14- 16, CR 18, 19	ϟ DIODE,SI,BV=70.0V,IO=50MA,DUAL,SOT23 ϟ	742544 742544	25403	BAW56	6	
CR 8, 9, 13, CR 17	ϟ DIODE,SI,BV=100,IO=100MA,SOT23 ϟ	821116 821116	04713	MMBD7000L	4	
J 1	SOCKET,2 ROW,PWB,0.100C,RT ANG,26 POS	543512	00779	2-535512-0	1	
J 2	HEADER,1 ROW,.050CTR,20 PIN	831529	47001	MICS20	1	
J 3	HEADER,1 ROW,.100CTR,3 PIN	845334	00779	640456-3	1	
J 4	CONN,D-SUB,PWB,RT ANG,9 PIN	855221	00779	747840-4	1	
J 5	HEADER,1 ROW,.197CTR,RT ANG,10 PIN	875695	06229	25.332.4053.1	1	
J 6	HEADER,1 ROW,.197CTR,RT ANG,8 PIN	875690	06229	25.332.3853.1	1	
L 1	CORE,BEAD,FERRITE,.335X.120	867734	34899	2743021447	1	
L 2	CHOKE,6TURN	320911	89536	320911	1	
P 10	CABLE ASSY,FLAT,10 CONDUCT,6.0"	714022	28213	1002645-C	1	
Q 1- 3	ϟ TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT-23	742684	04713	MMBT3906L	3	
Q 4- 6	ϟ TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	742676	04713	MMBT3904L	3	
Q 7, 8	ϟ TRANSISTOR,SI,N-MOS,50W,DPAK	927806	17856	SMD25N05-45L	2	
Q [illegible]	ϟ TRANSISTOR,SI,NPN,25V,SOT-23	820902	04713	MMBT5089L	1	
R 1, 2, 11, R 12, 22	ϟ RES,CERM,47K,+-5%,.125W,200PPM,1206 ϟ	746685 746685	91637	CRCW1206-4702JB02	5	
R 3, 4, 14, R 20, 21, 25, R 42, 47, 64	ϟ RES,CERM,10K,+-5%,.125W,200PPM,1206 ϟ ϟ	746610 746610 746610	91637	CRCW1206-1002JB02	9	
R 5	ϟ RES,CERM,1K,+-1%,.125W,100PPM,1206	783241	91637	CRCW1206-1001FB02	1	
R 6	ϟ RES,CERM,3.32K,+-1%,.125W,100PPM,1206	810788	91637	CRCW1206-3321FB02	1	
R 7, 16	ϟ RES,CERM,100K,+-5%,.125W,200PPM,1206	740548	91637	CRCW1206-1003JB02	2	
R 8, 63	ϟ RES,CERM,270,+-5%,.125W,200PPM,1206	746354	91637	CRCW1206-2700JB02	2	
R 9, 10, 35	ϟ RES,CERM,4.7K,+-5%,.125W,200PPM,1206	740522	91637	CRCW1206-4701JB02	3	
R 13	ϟ RES,CERM,20,+-5%,.125W,200PPM,1206	746222	91637	CRCW1206-20R0JB02	1	

Table 6-3. 2620A/2625A A1 Main PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
R 15	ϟ RES,CERM,33,+-5%,.125W,200PPM,1206	746248	91637	CRCW1206-33R0JB02	1	
R 17	RES,CF,1M,+-5%,0.25W	649970	59124	CF1/4 105J	1	
R 18	ϟ RES,CERM,10M,+-5%,.125W,300PPM,1206	783274	91637	CRCW1206-1005JB02	1	
R 19, 28, 34, R 49, 58	ϟ RES,CERM,470,+-5%,.125W,200PPM,1206 ϟ	740506 740506	91637	CRCW1206-4700JB02	5	
R 23	RES,CF,220K,+-5%,0.25W	851837	59124	CF1/4 224J	1	
R 24	ϟ RES,CERM,64.9K,+-1%,.125W,100PPM,1206	876086	91637	CRCW1206-6492FB	1	
R 26	ϟ RES,CERM,10.5K,+-1%,.125W,100PPM,1206	851852	91637	CRCW1206-1052FB	1	
R 27	ϟ RES,CERM,220K,+-5%,.125W,200PPM,1206	746750	91637	CRCW1206-2203JB02	1	
R 29- 31	RES,CF,0.50,+-5%,0.25W	830646	59124	CF1/4 R50J	3	
R 32, 33	RES,CF,1,+-5%,0.25W	867866	59124	CF1/4 1R0J	2	
R 36, 37	ϟ RES,CERM,15K,+-5%,.125W,200PPM,1206	746628	91637	CRCW1206-1502JB02	2	
R 38	RES JUMPER,0.02,0.25W	682575	91637	FRJ-55	1	
R 39	ϟ RES,CERM,63.4K,+-1%,.125W,100PPM,1206	836627	91637	CRCW1206-6342FB	1	
R 40	ϟ RES,CERM,5.1K,+-5%,.125W,200PPM,1206	746560	91637	CRCW1206-5101JB02	1	
R 41	ϟ RES,CERM,11K,+-1%,.125W,100PPM,1206	867291	91637	CRCW1206-1102FB	1	
R 43	ϟ RES,CERM,39K,+-5%,.125W,200PPM,1206	746677	91637	CRCW1206-3902JB02	1	
R 44	ϟ RES,CERM,1.30K,+-1%,.125W,100PPM,1206	780999	91637	CRCW1206-132FB02	1	
R 45	ϟ RES,CERM,1M,+-1%,.125W,100PPM,1206	836387	91637	CRCW1206-1004FB02	1	
R 46	ϟ RES,CERM,4.02K,+-1%,.125W,100PPM,1206	783266	91637	CRCW1206-4021FB02	1	
R 48	RES,CF,10K,+-5%,0.25W	697102	59124	CF1/4 103J	1	
R 50- 57, 59- R 62	RES,CF,47,+-5%,0.25W	822189 822189	59124	CF1/4 470J	12	
RT 1	THERMISTOR,DISC,0.46,25 C	875240	4Z785	RXE065	1	
RV 1	VARISTOR,39V,+-20%,1.0MA	831735	34371	V39MA2A	1	
S 1	SWITCH,PUSHBUTTON,DPDT,PUSH-PUSH	836361	31918	NE182UEESP	1	
T 1	TRANSFORMER,INVERTER	873968	89536	873968	1	
T 2	INDUCTOR,FXD,DUAL,EE24-25,0.4MH,1.2A	817379	89536	817379	1	
TP 1, 30	JUMPER,WIRE,NONINSUL,0.200CTR	816090	91984	150T1	2	
U 1	IC,CMOS,64 X 16 BIT EEPROM,SERIAL,SO8	876789	27014	NM93C46M8	1	
U 2	ϟ IC,CMOS,TRIPLE PROGRAMMABLE TIMER	866991	62786	293D105XHD63A40RP	1	
U 3	ϟ MODULE,8KX8 SRAM,ZERO PWR,TIMEKEEPER	867945	50088	MK48T08B20	1	
U 4	ϟ IC,CMOS,8-BIT MPU,1.5MHZ,256BYT,PLCC	876896	62786	HD63A03YCP	1	
U 5, 7	ϟ ISOLATOR,OPTO,LED TO TRANSISTOR	851790	25088	4N28-584	2	
U 6	ϟ IC,VOLT REG,ADJ,1.2 TO 37 V,1.5 AMPS	460410	27014	LM317T	1	
U 8	ϟ 2620A-PROGRAMMED EPROM	894555	89536	894555	1	
U 9	ϟ IC,VOLT REG,ADJ,SWITCHING REGULATOR	867135	27014	LM2579T	1	
U 10	ϟ IC,CMOS,TRIPLE 3 INPUT NOR GATE,SOIC	867981	6E570	74HC27D	1	
U 11	ϟ IC,CMOS,3-8 LINE DCDR W ENABLE,SOIC	783019	6E570	74HC138D	1	
U 12, 28	ϟ IC,CMOS,QUAD INPUT NAND GATE,SOIC	830703	6E570	74HC00D	2	
U 13	ϟ IC,CMOS,OCTL LINE DRVR,SOIC	801043	04713	MC74HC244AD	1	
U 14	ϟ IC,CMOS,QUAD 2 INPUT XOR GATE,SOIC	867973	6E570	74HC86D	1	
U 15	ϟ IC,CMOS,QUAD INPUT NOR GATE,SOIC	830711	6E570	74HC02D	1	
U 16, 26	ϟ IC,CMOS,OCTAL D F/F,+EDG TRG,SOIC	838029	6E570	74HC273D	2	
U 17, 27	ϟ IC,ARRAY,7 NPN DARLINGTON PAIRS,SOIC	821009	31019	ULN-2004L	2	
U 18	ϟ IC,VOLT REG,FIXED,-5.0 VOLTS,0.1 AMPS	454793	27014	79L05A	1	
U 19	ϟ IC,VOLT REG,ADJ,1.2 TO 32 V,0.1 A	810242	01295	TL317CLP	1	
U 20	ϟ IC,CMOS,12 STAGE BIN RIPPLE CNTR,SOIC	831636	6E570	74HC4040D	1	
U 21	ϟ IC,CMOS,TRIPLE 3 INPUT NAND GATE,SOIC	867978	01295	SN74HC10D	1	
U 22	ϟ IC,CMOS,DUAL D F/F,+EDG TRG,SOIC	782995	6E570	74HC74D	1	
U 23	ϟ IC,CMOS,HEX INVERTER,UNBUFFERED,SOIC	806893	6E570	74HCU04D	1	
U 24	ϟ IC,COMPARATOR,DUAL,LOW PWR,SOIC	837211	6E570	LM393D	1	
U 25	ϟ IC,CMOS,RS232 DRIVER/RECEIVER,SOIC	821538	04713	MC145406DW	1	

Table 6-3. 2620A/2625A A1 Main PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
U 29	⚡ IC,CMOS,8 BIT P/S-IN,S-OUT SHFT,SOIC	782904	6E570	74HCT165D	1	
VR 1	⚡ ZENER,UNCOMP,5.6V,5%,20MA,0.2W,SOT-23	875604	04713	MMBZ5232BL	1	
VR 2	⚡ ZENER,UNCOMP,6.0V,5%,20MA,0.2W,SOT-23	837161	04713	MMBZ5233BT1	1	
VR 3	⚡ ZENER,UNCOMP,6.8V,5%,20MA,0.2W,SOT-23	837195	04713	MMBZ5235BL	1	
VR 4	⚡ IC, 1.23V,150 PPM T.C.,BANDGAP V. REF	634451	27014	LM385Z-1.2D26Z	1	
Y 1	CRYSTAL,4.9152 MHZ,± 0.005%,HC-18/U	800367	75378	MP042	1	
Z 1	RES,CERM,NET,CUSTOM	821157	91637	SOGC-2000-S4	1	
Z 2	RES,CERM,SOIC,16 PIN,15 RES,22K,+-2%	867841	91637	SOMC-1601-223G	1	
Z 3	RES,CERM,SOIC,20 PIN,10 RES,47K,+-2%,	867846	80294	4420P-001-473	1	
NOTES:	⚡ Static sensitive part.					


U28
U20
U14
U10
TP20
R25
U2
C3
R64
TP16
C40
C36
C27
C23
U29
U21
U15
U11
TP17
U8
U3
J1
C41
C37
C28
C24
U25
R2
TP12
C42
CR16
CR17
AR3
AR2
Z1
TP18
C29
CR15
CR14
TP13
CR18
CR19
Z3
Z2
C22
C19
W1
C11
AR1
U12
J4
R19
C15
U1
C1
TP19
U26
U16
U13
Y1
TP11
U4
C8
R63
R1
TP3
TP5
TP6
TP4
C38
C33
C25
C16
R20
R21
J2
U27
U17
Q8
Q7
VR3
R22
TP2
TP15
R8
R7
R3
TP8
U7
U5
J5
C43
R49
C44
R50
RV1
R35
R36
R37
R34
R28
CR8
CR9
CR12
CR11
CR5
CR6
C45
R51
C46
R52
C47
R53
C48
R54
C49
R55
C50
R56
C51
R57
U22
TP9
TP14
TP10
R38
C30
CR13
C31
U23
R47
C35
R40
R41
R45
R42
T1
C12
C13
CR7
C4
C5
C6
TP31
TP30
TP32
P10
R4
R5
R6
U6
U18
VR4
U24
R43
C32
L1
C52
C53
C54
R58
C55
C56
C57
C58
R59
R60
R61
R62
L2
J6
R46
R44
C34
U19
R39
TP7
C26
CR10
C14
TP1
S1
C7
CR1
CR2
CR3
C2
J3
R29
R30
R31
R32
R33
R23
R26
R27
C20
C21
R24
R17
C18
R18
U9
T2
C39
R48
C59
RT1

NOTE: TP2-TP20,TP31,TP32,W1 ARE NOT COMPONENTS.

2620A-1601

Figure 6-3. 2620A/2625A A1 Main PCA

Table 6-4. 2635A A1 Main PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
BT 1	BATTERY,LITHIUM,3.0V,0.500AH	821439	7X302	ES954-03	1	
C 1, 4, 5, C 32, 34	CAP,AL,1UF,+-20%,50V,SOLV PROOF	782805 782805	62643	KMA50105M4X7LL	5	
C 2	CAP,CER,0.033UF,+-20%,100V,X7R,1206	886655	04222	12061C333MATMA	1	
C 3, 8	CAP,CER,27PF,+-10%,50V,C0G,1206	800508	04222	12065A270KATBA	2	
C 6	CAP,AL,10UF,+-20%,63V,SOLV PROOF	816843	62643	KME63T10RM5X11RP	1	
C 7	CAP,AL,10000UF,+-20%,35V,SOLV PROOF	875203	62643	SMH35VN103M35X25LLV	1	
C 9, 10, 43- C 52, 54- 59	CAP,CER,180PF,+-10%,50V,C0G,1206	769778 769778	04222	12065A181KATBA	18	
C 11, 15, 16, C 19, 22- 25, C 28, 29, 33, C 36, 38, 40- C 42, 60- 65, C 68, 70- 73, C 75, 76	CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287 747287 747287 747287 747287 747287 747287	04222	12065C104KATBA	29	
C 12, 13	CAP,AL,470UF,+-20%,16V,SOLV PROOF	772855	62643	KME16T471M10X12.5MC	2	
C 14	CAP,AL,2200UF,+-20%,10V,SOLV PROOF	875208	62643	LXE10VB222M18X15MC	1	
C 17	CAP,AL,2.2UF,+-20%,50V,SOLV PROOF	769687	62643	KMA50T2R2M45X85LL	1	
C 18	CAP,CER,33PF,+-10%,50V,C0G,1206	769240	04222	12065A330KATBA	1	
C 20	CAP,CER,1800PF,+-10%,50V,C0G,1206	769786	04222	12065A182KATBA	1	
C 21	CAP,CER,820PF,+-5%,50V,C0G,1206	867403	04222	12065A821JATBA	1	
C 26	CAP,AL,47UF,+-20%,100V,SOLV PROOF	837492	62643	KMF100VB47RM10X16MX	1	
C 30, 31, 66, C 67	CAP,AL,47UF,+-20%,50V,SOLV PROOF	822403 822403	62643	KME50T47RM6X11RP	4	
C 35, 53, 74	CAP,CER,1000PF,+-5%,50V,C0G,1206	867408	04222	12065A102JATBA	3	
C 39	CAP,CER,0.047UF,+-10%,100V,X7R	844733	04222	SR591C473KAA	1	
C 69	CAP,CER,4700PF,+-10%,50V,X7R,1206	832279	04222	12061C472KATBA	1	
CR 1, 10	DIODE,SI,100 PIV,3.3 AMPS,SCHOTTKY	837740	59993	30WQ10F	2	
CR 2, 3	DIODE,SI,600 PIV,1.5 AMP	112383	55464	1N5397	2	
CR 4, 11, 12, CR 20	ϟ DIODE,SI,BV=75V,IO=250MA,SOT23 ϟ	830489 830489	25403	BAS16	4	
CR 5, 6, 21	ϟ DIODE,SI,SCHOTTKY BARRIER,40V,1A	837732	04713	MBR140P	3	
CR 7, 14- 16, CR 18, 19	ϟ DIODE,SI,BV=70.0V,IO=50MA,DUAL,SOT23 ϟ	742544 742544	25403	BAW56	6	
CR 8, 9, 13, CR 17	ϟ DIODE,SI,BV=100,IO=100MA,SOT23 ϟ	821116 821116	04713	MMBD7000L	4	
J 1	SOCKET,2 ROW,PWB,0.100C,RT ANG,26 POS	543512	00779	2-535512-0	1	
J 2	HEADER,1 ROW,.050CTR,20 PIN	831529	47001	MICS20	1	
J 3	HEADER,1 ROW,.100CTR,3 PIN	845334	00779	640456-3	1	
J 4	CONN,D-SUB,PWB,RT ANG,9 PIN	855221	00779	747840-4	1	
J 5	HEADER,1 ROW,.197CTR,RT ANG,10 PIN	875695	06229	25.332.4053.1	1	
J 6	HEADER,1 ROW,.197CTR,RT ANG,8 PIN	875690	06229	25.332.3853.1	1	
L 1	CORE,BEAD,FERRITE,.335X.120	867734	34899	2743021447	1	
L 2	CHOKE,6TURN	320911	89536	320911	1	
MP 32[illegible]	JUMPER,REC,2 POS,.100CTR,.025 SQ POST	757294	00779	850108-1	1	
P 4	HEADER,2 ROW,.050CTR,40 PIN	838573	00779	104068-4	1	
P 10	CABLE ASSY,FLAT,10 CONDUCT,6.0"	714022	28213	1002645-C	1	
Q 1- 3, 10	ϟ TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT-23	742684	04713	MMBT3906L	4	
Q 4- 6	ϟ TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	742676	04713	MMBT3904L	3	
Q 7, 8	ϟ TRANSISTOR,SI,N-MOS,50W,DPAK	927806	17856	SMD25N05-45L	2	
Q 9	ϟ TRANSISTOR,SI,NPN,25V,SOT-23	820902	04713	MMBT5089L	1	
R 1, 11, 12, R 22, 25, 45	ϟ RES,CERM,47K,+-5%,.125W,200PPM,1206 ϟ	746685 746685	91637	CRCW1206-4702JB02	6	
R 2	ϟ RES,CERM,698K,+-1%,.125W,100PPM,1206	867296	91637	CRCW1206-6983FB	1	

Table 6-4. 2635A A1 Main PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
R 3, 4, 14, R 42, 47, 64, R 65, 68, 70, R 72- 75, 78, R 79, 81	ϟ RES,CERM,10K,+-5%,.125W,200PPM,1206 ϟ ϟ ϟ ϟ	746610 746610 746610 746610 746610	91637	CRCW1206-1002JB02	16	
R 5, 98	ϟ RES,CERM,1K,+-1%,.125W,100PPM,1206	783241	91637	CRCW1206-1001FB02	2	
R 6	ϟ RES,CERM,3.32K,+-1%,.125W,100PPM,1206	810788	91637	CRCW1206-3321FB02	1	
R 7, 16, 35	ϟ RES,CERM,100K,+-5%,.125W,200PPM,1206	740548	91637	CRCW1206-1003JB02	3	
R 8, 21	ϟ RES,CERM,270,+-5%,.125W,200PPM,1206	746354	91637	CRCW1206-2700JB02	2	
R 9, 10, 39, R 41, 71, 77, R 83	ϟ RES,CERM,4.7K,+-5%,.125W,200PPM,1206 ϟ ϟ	740522 740522 740522	91637	CRCW1206-4701JB02	7	
R 13	ϟ RES,CERM,20,+-5%,.125W,200PPM,1206	746222	91637	CRCW1206-20R0JB02	1	
R 15, 86,107	ϟ RES,CERM,33,+-5%,.125W,200PPM,1206	746248	91637	CRCW1206-33R0JB02	3	
R 17	RES,CF,1M,+-5%,0.25W	649970	59124	CF1/4 105J	1	
R 18	ϟ RES,CERM,10M,+-5%,.125W,300PPM,1206	783274	91637	CRCW1206-1005JB02	1	
R 19	ϟ RES,CERM,11K,+-1%,.125W,100PPM,1206	867291	91637	CRCW1206-1102FB	1	
R 20	ϟ RES,CERM,59K,+-1%,.125W,100PPM,1206	851803	91637	CRCW1206-593FB	1	
R 23	RES,CF,220K,+-5%,0.25W	851837	59124	CF1/4 224J	1	
R 24	ϟ RES,CERM,64.9K,+-1%,.125W,100PPM,1206	876086	91637	CRCW1206-6492FB	1	
R 26	ϟ RES,CERM,10.5K,+-1%,.125W,100PPM,1206	851852	91637	CRCW1206-1052FB	1	
R 27	ϟ RES,CERM,220K,+-5%,.125W,200PPM,1206	746750	91637	CRCW1206-2203JB02	1	
R 28, 34, 49, R 58	ϟ RES,CERM,470,+-5%,.125W,200PPM,1206 ϟ	740506 740506	91637	CRCW1206-4700JB02	4	
R 29- 31	RES,CF,0.50,+-5%,0.25W	830646	59124	CF1/4 R50J	3	
R 32, 33	RES,CF,1,+-5%,0.25W	867866	59124	CF1/4 1R0J	2	
R 36	ϟ RES,CERM,3.6K,+-5%,.125W,200PPM,1206	746537	91637	CRCW1206-3601JB02	1	
R 37	ϟ RES,CERM,9.1K,+-5%,.125W,200PPM,1206	746602	91637	CRCW1206-9103JB02	1	
R 38	RES JUMPER,0.02,0.25W	682575	91637	FRJ-55	1	
R 40	ϟ RES,CERM,5.1K,+-5%,.125W,200PPM,1206	746560	91637	CRCW1206-5101JB02	1	
R 43, 63, 84, R 92	ϟ RES,CERM,1.5K,+-5%,.125W,200PPM,1206 ϟ	746438 746438	91637	CRCW1206-1501JB02	4	
R 44	ϟ RES,CERM,1.30K,+-1%,.125W,100PPM,1206	780999	91637	CRCW1206-132FB02	1	
R 46	ϟ RES,CERM,4.02K,+-1%,.125W,100PPM,1206	783266	91637	CRCW1206-4021FB02	1	
R 48	RES,CF,10K,+-5%,0.25W	697102	59124	CF1/4 103J	1	
R 50- 57, 59- R 62	RES,CF,47,+-5%,0.25W	822189 822189	59124	CF1/4 470J	12	
R 66, 67, 69, R 80, 82, 85, R 87- 91, 93- R 97, 99-106, R 108-118	ϟ RES,CERM,47,+-5%,.0625W,200PPM,0603 ϟ ϟ ϟ ϟ	927707 927707 927707 927707 927707	91637	CRCW0603-470JRT1	35	
RT 1	THERMISTOR,DISC,0.46,25 C	875240	4Z785	RXE065	1	
RV 1	VARISTOR,41.5V,+-9%,1.0MA,1206	914114	4B792	V33MLA1206H23	1	
S 1	SWITCH,PUSHBUTTON,DPDT,PUSH-PUSH	836361	31918	NE182UEESP	1	
T 1	TRANSFORMER,INVERTER	873968	89536	873968	1	
T 2	INDUCTOR,FXD,DUAL,EE24-25,0.4MH,1.2A	817379	89536	817379	1	
T 3	INDUCTOR,20UH,1.15ADC	914007	0NFL0	CTX20-1	1	
TP 1, 30	TERM,UNINSUL,WIRE FORM,TEST POINT	781237	27918	TP102-01	2	
U 1	ϟ IC,INTEGR MLTIPROTOCOL MPU,16 MHZ,QFP	910831	04713	MC68302FC16	1	
U 2	ϟ IC,CMOS,QUAD BUS BUFFER W/3-ST,SOIC	866801	27014	MM74HC125M FLOW 63	1	
U 3, [illegible]	ϟ IC,OP AMP,QUAD,LOW POWER,SOIC	742569	6E570	LM324D	2	
U 5, 7	ϟ ISOLATOR,OPTO,LED TO TRANSISTOR	851790	25088	4N28-584	2	
U 6	ϟ IC,VOLT REG,ADJ,1.2 TO 37 V,1.5 AMPS	460410	27014	LM317T	1	
U 8	ϟ IC,OP AMP,DUAL,LOW POWER,SOIC	867932	6E570	LM358D	1	
U 9	ϟ IC,VOLT REG,ADJ,SWITCHING REGULATOR	867135	27014	LM2579T	1	
U 10	ϟ IC,CMOS,MICROPROCESSOR SUPERVISOR,DIP	913975	39003	MAX694CPA	1	

Table 6-4. 2635A A1 Main PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
U 11	⚡ GAL,PROGRAMMED,I/O DECODER	931910	89536	931910	1	
U 12	⚡ IC,CMOS,PARALLEL I/O CAL/CLCK W/CRYST	914036	61722	RTC64613	1	
U 13	⚡ IC,CMOS,RS232 DRIVER/RECEIVER,SOIC	821538	04713	MC145406DW	1	
U 14, 16	2635A PROGRAMMED ROM SET	932129	89536	932129	1	
U 15	⚡ IC,CMOS,REGULATOR,STEP-UP,PWM,SO16	914080	39003	MAX732CWE	1	
U 17, 27	⚡ IC,ARRAY,7 NPN DARLINGTON PAIRS,SOIC	821009	31019	ULN-2004L	2	
U 18	⚡ IC,VOLT REG,FIXED,-5.0 VOLTS,0.1 AMPS	454793	27014	79L05A	1	
U 19	⚡ IC,VOLT REG,ADJ,1.2 TO 32 V,0.1 A	810242	01295	TL317CLP	1	
U 20, 24	⚡ IC,CMOS,SRAM,128K X 8,120 NS,SO32	914101	62786	HM628128LFP-8SLT	2	
U 22	⚡ IC,CMOS,DUAL D F/F,+EDG TRG,SOIC	782995	6E570	74HC74D	1	
U 23	⚡ IC,CMOS,HEX INVERTER,UNBUFFERED,SOIC	806893	6E570	74HCU04D	1	
U 25	⚡ IC,PROG GATE ARRAY,3000 G,70 MHZ,PQFP	887138	68994	XC3030-70PQ100C	1	
U 26	⚡ IC,CMOS,QUAD INPUT NAND GATE,SOIC	830703	6E570	74HC00D	1	
VR 1	⚡ ZENER,UNCOMP,5.6V,5%,20MA,0.2W,SOT-23	875604	04713	MMBZ5232BL	1	
VR 2	⚡ ZENER,UNCOMP,6.0V,5%,20MA,0.2W,SOT-23	837161	04713	MMBZ5233BT1	1	
VR 3	⚡ ZENER,UNCOMP,6.8V,5%,20MA,0.2W,SOT-23	837195	04713	MMBZ5235BL	1	
W 3	HEADER,1 ROW,.100CTR,2 PIN	643916	00779	103747-2	1	
Y 1	CRYSTAL,12.288MHZ,50PPM,SURFACE MT	913942	61429	FPX128-20	1	
Z 1	RES,CERM,NET,CUSTOM	821157	91637	SOGC-2000-S4	1	
Z 2	RES,CERM,SOIC,16 PIN,15 RES,22K,+-2%	867841	91637	SOMC-1601-223G	1	
Z 3	RES,CERM,SOIC,20 PIN,10 RES,47K,+-2%,	867846	80294	4420P-001-473	1	
NOTES:	⚡ Static sensitive part.					

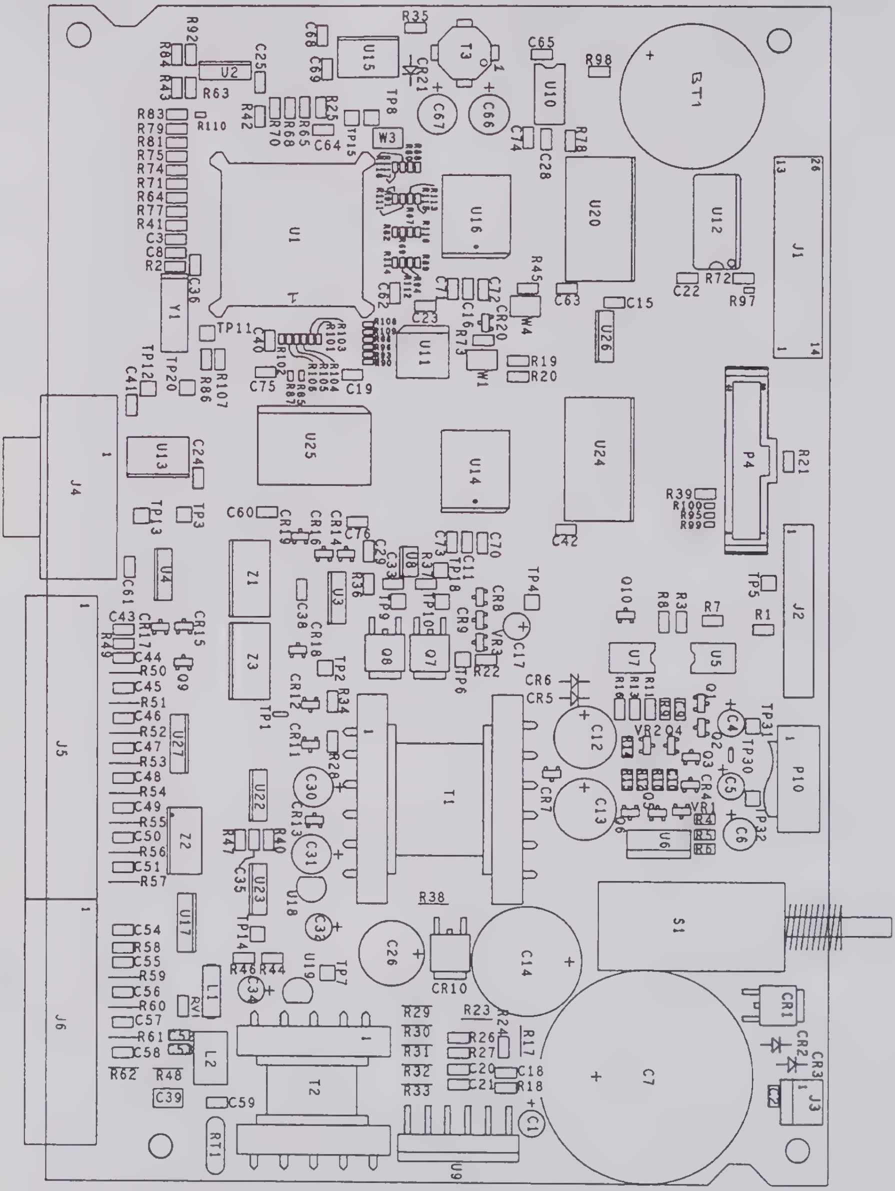

R92
R84
R43
U2
R63
C25
C68
C69
U15
R35
T3
CR21
C67
C66
C65
U10
R98
BT1
R42
R70
R68
R65
R25
C64
TP8
TP15
W3
C74
C28
R78
R83
R79
R81
R75
R74
R71
R64
R77
R41
C3
C8
R2
R110
U1
U16
U20
U12
J1
R45
C63
C15
R72
C22
R97
Y1
C36
C62
C71
C12
C16
CR20
W4
U26
C23
TP11
C40
R103
R101
R102
R104
R106
R105
R87
U11
R73
W1
R19
R20
TP12
TP20
R86
R107
C41
C75
C19
U13
C24
U25
U14
U24
P4
R21
R39
R100
R95
R99
C42
J4
TP13
TP3
C60
CR19
CR16
CR14
C76
C29
C33
U8
R37
TP18
C73
C11
C70
U4
Z1
U3
R36
TP9
TP10
CR8
TP4
Q10
R8
R3
R7
R1
TP5
J2
C61
C38
CR18
Q8
Q7
CR9
VR3
C17
TP6
R22
U7
U5
C43
CR17
CR15
R49
C44
Q9
R50
C45
R51
C46
R52
C47
R53
C48
R54
C49
R55
C50
R56
C51
R57
Z3
TP2
CR12
R34
TP1
CR11
CR6
CR5
C12
VR2
Q4
Q1
C4
TP31
P10
TP30
Q3
CR4
C5
Q2
U27
J5
U22
R28
C30
T1
CR7
C13
VR1
R4
R5
R6
U6
C6
TP32
CR13
Z2
R47
R40
C31
C35
U23
U18
U17
R38
S1
C54
R58
C55
R59
C56
R60
C57
R61
C58
C3
C26
CR10
C14
TP14
R46
R44
U19
TP7
C34
L1
RV1
CR1
CR2
CR3
J6
R29
R23
R30
R24
R17
R26
R31
R27
R32
C20
C18
R33
C21
R18
C1
C7
L2
T2
J3
R62
R48
C39
C59
RT1
U9
2635A-1601

Figure 6-4. 2635A A1 Main PCA

Table 6-5. A2 Display PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1, 3- 6	CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	04222	12065C104KATBA	5	
C 2	CAP,TA,4.7UF,+-20%,15V	745976	56289	195D475X0015V2B	1	
CR 3	ϟ DIODE,SI,BV=75V,IO=250MA,SOT23	830489	25403	BAS16	1	
DS 1	TUBE,DISPLAY,VAC FLUOR,7 SEG,10 CHAR	783522	0BW21	CPF2397A	1	
J 1	HEADER,1 ROW,.050CTR,20 PIN	831529	47001	MICS20	1	
LS 1	AF TRANSD,PIEZO,22 MM	602490	51406	PKM24-4A1	1	
MP 69	LABEL,ADHESIVE,IC,HIGH TEMPERATURE	720904	85480	DAT-1-637-10	1	
R 1, 10, 12	ϟ RES,CERM,10K,+-5%,.125W,200PPM,1206	746610	91637	CRCW1206-1002JB02	3	
R 2	ϟ RES,CERM,2.2M,+-5%,.125W,200PPM,1206	811778	91637	CRCW1206-2204JB02	1	
R 3	ϟ RES,CERM,1.2M,+-5%,.125W,200PPM,1206	806240	91637	CRCW1206-1204JB02	1	
R 11	ϟ RES,CERM,1K,+-5%,.125W,200PPM,1206	745992	91637	CRCW1206-1001JB02	1	
U 1	ϟ IC,CMOS,4-BIT MPU,FLUKE 45-90002	820993	33297	UPD7527ACU	1	
U 4	ϟ IC,CMOS,DUAL DIV BY 16 BIN CNTR,SOIC	837054	6E570	74HC393D	1	
U 5	ϟ IC,CMOS,DUAL MONOSTB MULTIVBRTR,SOIC	806620	6E570	74HC423D	1	
U 6	ϟ IC,CMOS,QUAD 2 IN NAND W/SCHMT,SOIC	837245	04713	MC74HC132D	1	
Z 1	RES,CERM,SOIC,16 PIN,15 RES,10K,+-5%	836296	91637	SOMC-1601-103G	1	
NOTES:	ϟ Static sensitive part.					

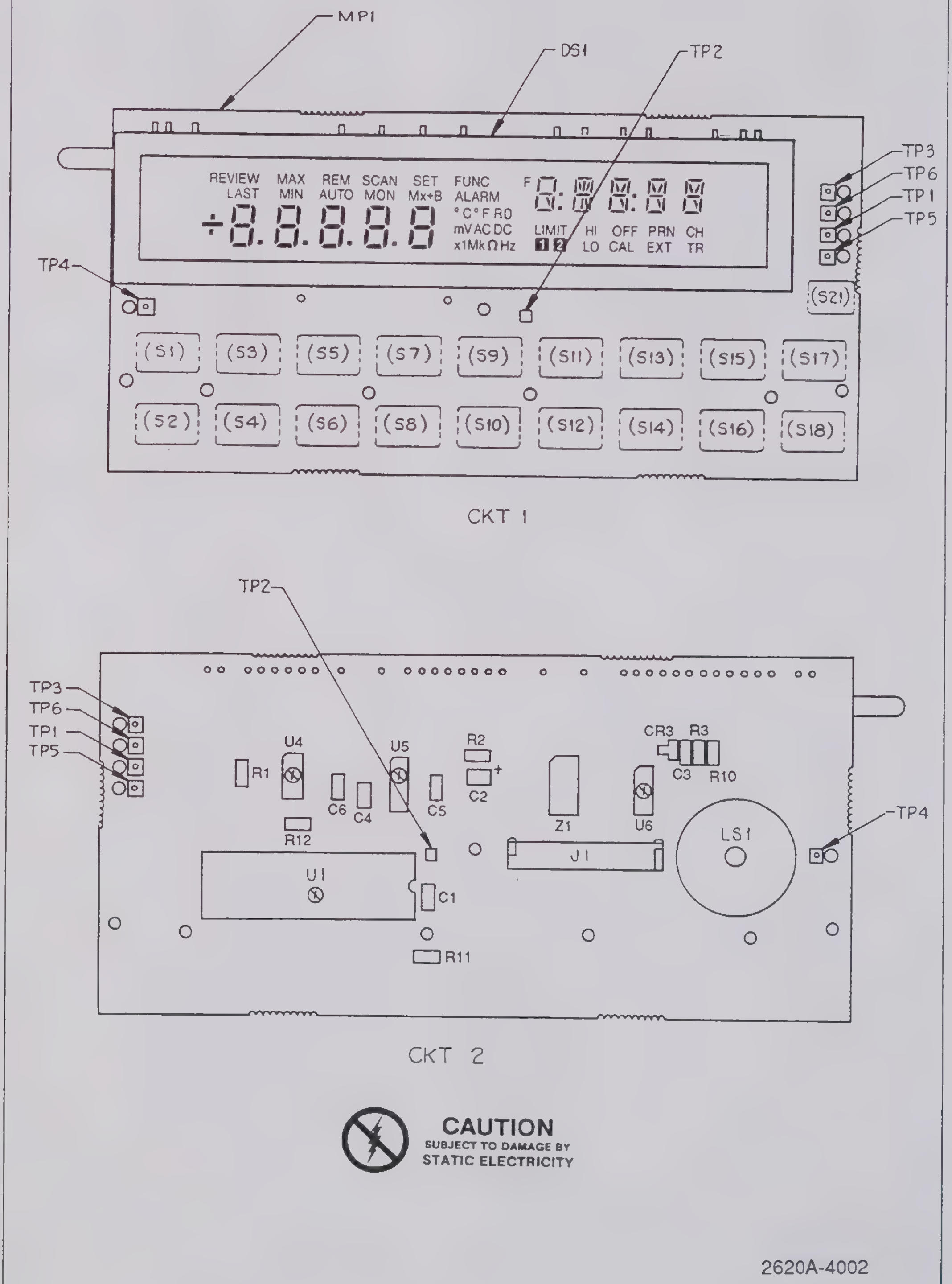

MP1
DS1
TP2
TP3
TP6
TP1
TP5
TP4
REVIEW LAST
MAX MIN
REM AUTO
SCAN MON
SET Mx+B
FUNC ALARM
°C°F RO
mV AC DC
x1MkΩHz
LIMIT 1 2
HI LO
OFF CAL
PRN EXT
CH TR
(S1)
(S2)
(S3)
(S4)
(S5)
(S6)
(S7)
(S8)
(S9)
(S10)
(S11)
(S12)
(S13)
(S14)
(S15)
(S16)
(S17)
(S18)
(S21)
CKT 1
TP2
TP3
TP6
TP1
TP5
U4
U5
R1
R2
C2
CR3
R3
C3
R10
C6
C4
C5
R12
Z1
U6
TP4
LS1
J1
U1
C1
R11
CKT 2
CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY
2620A-4002

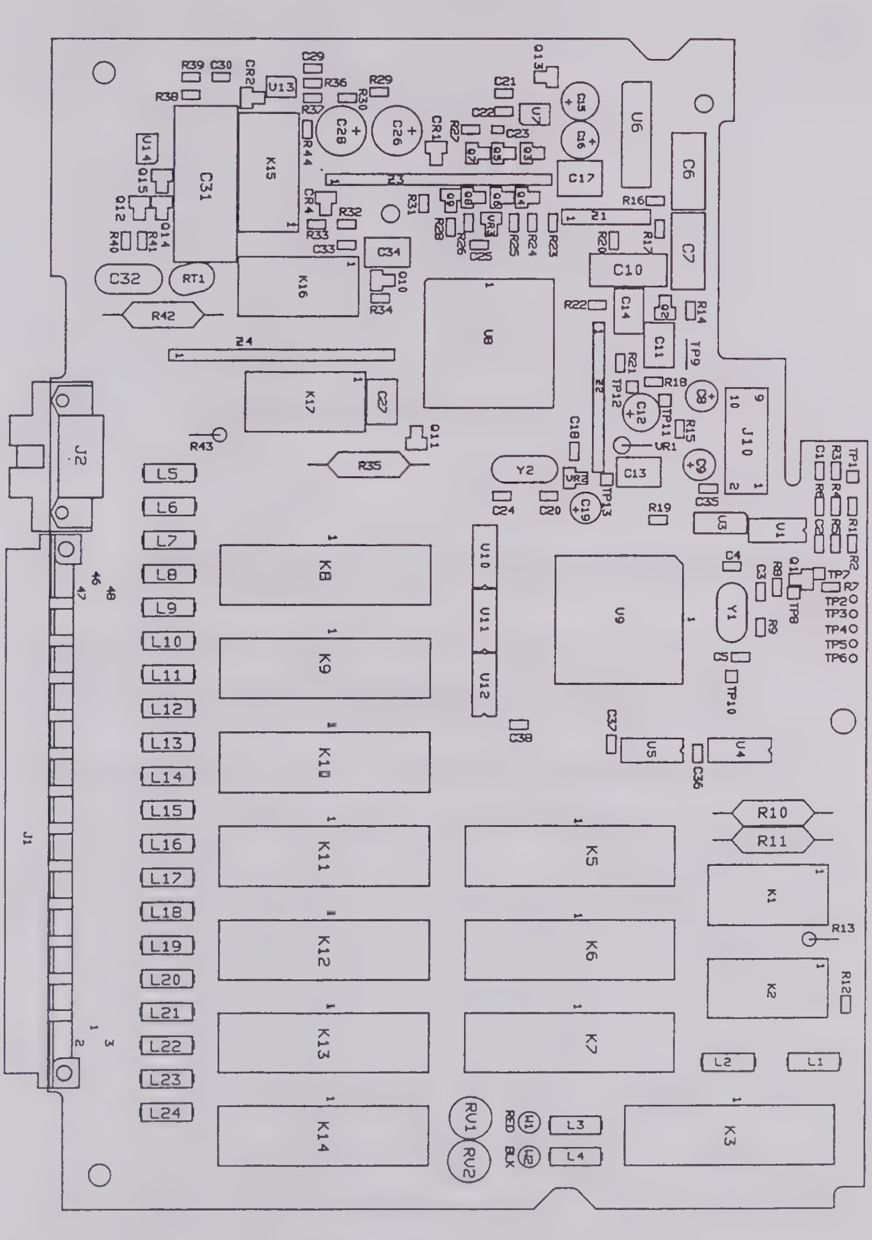
Figure 6-5. A2 Display PCA

Table 6-6. A3 A/D Converter PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1- 3, 18, C 21, 22, 25, C 29, 33	CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287 747287 747287	04222	12065C104KATBA	9	
C 4, 5	CAP,CER,15PF,+-10%,50V,C0G,1206	837393	04222	12065A150KATBA	2	
C 6, 7, 10	CAP,POLYPR,0.1UF,+-10%,160V	446781	68919	MKP4104K160B	3	
C 8, 9, 19	CAP,TA,10UF,+-20%,10V	714766	56289	199D106X0010BE2	3	
C 11	CAP,POLYPR,2200PF,+-5%,100V	854505	68919	FKP2222J100V	1	
C 12	CAP,TA,2.2UF,+-10%,35V	697433	56289	199D225X9035BG2	1	
C 13	CAP,POLYPR,0.033UF,+-10%,63V	721050	68919	MKP20333K63	1	
C 14, 34	CAP,POLYPR,1000PF,+-1%,100V	844816	68919	FKP2102F100V	2	
C 15, 16	CAP,TA,33UF,+-10%,6V	866897	56289	199D336X9006CG2	2	
C 17	CAP,POLYES,1UF,+-10%,50V	733089	68919	MKS2105K50	1	
C 20, 24	CAP,CER,4.3PF,+-10%,50V,C0G,1206	844738	04222	12061A4R3KATBA	2	
C 23	CAP,CER,4.3PF,+-0.5PF,50V,C0G,0805	514216	51406	GRH708C0G4R3D200AL	1	
C 26, 28	CAP,AL,470UF,+-20%,10V,SOLV PROOF	822387	62643	KME10VB471M8X11FTV	2	
C 27	CAP,POLYPR,100PF,+-1%,100V	844803	68919	FKP2101F100V	1	
C 30	CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	04222	12061C103KATBA	1	
C 31	CAP,POLYES,0.1UF,+-10%,1000V	837518	68919	MKS4223K1000	1	
C 32	CAP,CER,2500PF,+-20%,250V,X7R	485680	4U402	WY9-2500PF/250V 20%-1	1	
C 35- 38	CAP,CER,180PF,+-10%,50V,C0G,1206	769778	04222	12065A181KATBA	4	
CR 1, 2, 4	⚡ DIODE,SI,BV=70.0V,IO=50MA,DUAL,SOT23	742320	25403	BAV99	3	
J 1	CONN,DIN41612,TYPE C,RT ANG,48 PIN	867333	0G8R9	73-03-148-6999	1	
J 2	CONN,MICRO-RIBBON,PLUG,RT ANG,20 POS	876107	83486	10-5061-020-101-688	1	
J 10	HEADER,2 ROW,.100CTR,10 PIN	756858	00779	102977-5	1	
K 1, 2, 15- K 17	RELAY,ARMATURE,2 FORM C,5VDC,LATCH	836486 836486	61529	DS2ESL2DC5VCH245	5	
K 3, 5- 14	RELAY,ARMATURE,4 FORM C,5 V,LATCH	867882	61529	DS4E-SL2-DC5V-H285	11	
L 1- 24	CORE,BEAD,FERRITE,.335X.120	867734	34899	2743021447	24	
Q 1	⚡ TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT-23	742684	04713	MMBT3906L	1	
Q 2, 12, 13	⚡ TRANSISTOR,SI,N-JFET,SOT-23	876263	27014	SB90041	3	
Q 3- 9	⚡ TRANSISTOR,SI,N-JFET,SOT-23	820860	17856	SSTH17	7	
Q 10, 11, 14, Q 15	⚡ TRANSISTOR,SI,NPN,SELECT IEBO,SOT-23 ⚡	821637 821637	04713	SMBT1388L	4	
R 1	⚡ RES,CERM,10K,+-1%,.125W,100PPM,1206	769794	91637	CRCW1206-1002FB02	1	
R 2, 36, 40	⚡ RES,CERM,30.1K,+-1%,.125W,100PPM,1206	801258	91637	CRCW1206-3012FB02	3	
R 3, 4	⚡ RES,CERM,470K,+-5%,.125W,200PPM,1206	746792	91637	CRCW1206-4703JB02	2	
R 5	⚡ RES,CERM,100K,+-1%,.125W,100PPM,1206	769802	91637	CRCW1206-1003FB02	1	
R 6, 8, 9, R 19, 23, 34	⚡ RES,CERM,10K,+-5%,.125W,200PPM,1206 ⚡	746610 746610	91637	CRCW1206-1002JB02	6	
R 7	⚡ RES,CERM,360,+-5%,.125W,200PPM,1206	783290	91637	CRCW1206-3600JB02	1	
R 10, 11	RES,MF,1K,+-1%,100PPM,FLMPRF,FUSIBLE	650085	91637	CMF-65-69 1001F T-1	2	1
R 12, 33, 39, R 44	⚡ RES,CERM,1K,+-5%,.125W,200PPM,1206 ⚡	745992 745992	91637	CRCW1206-1001JB02	4	
R 13, 43	RES,CF,270,+-5%,0.25W	810424	59124	CF1/4 271J	2	
R 14, 24- 28	⚡ RES,CERM,47K,+-5%,.125W,200PPM,1206	746685	91637	CRCW1206-4702JB02	6	
R 15	⚡ RES,CERM,61.9K,+-1%,.125W,100PPM,1206	821330	91637	CRCW1206-6192FB02	1	
R 16, 17, 20	⚡ RES,CERM,200K,+-5%,.125W,200PPM,1206	746743	91637	CRCW1206-2003JB02	3	
R 18	⚡ RES,CERM,16.9K,+-1%,.125W,100PPM,1206	836635	91637	CRCW1206-1692FB	1	
R 21	⚡ RES,CERM,845,+-1%,.125W,100PPM,1206	821322	91637	CRCW1206-8450FB02	1	
R 22	⚡ RES,CERM,91K,+-5%,.125W,200PPM,1206	811828	91637	CRCW1206-9102JB02	1	
R 29, 30	⚡ RES,CERM,22,+-5%,.125W,200PPM,1206	746230	91637	CRCW1206-22R0JB02	2	
R 31, 32, 38	⚡ RES,CERM,100K,+-5%,.125W,200PPM,1206	740548	91637	CRCW1206-1003JB02	3	
R 35, 42	⚡ RES,CERM,100K,+-5%,3W	820811	59124	SPR3-104J	2	
R 37	⚡ RES,CERM,24.9K,+-1%,.125W,100PPM,1206	867689	89536	867689	1	
R 41	⚡ RES,CERM,30.1K,+-1%,.125W,100PPM,1206	801258	89536	801258	1	

Table 6-6. A3 A/D Converter PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
RT 1	THERMISTOR,DISC,POS,1K,+-40%,25 C	820878	54583	911P87E102YU07	1	
RV 1, 2	VARISTOR,910,+-10%,1.0MA	876193	34371	V910LSX1399	2	
TP 9	JUMPER,WIRE,NONINSUL,0.200CTR	816090	91984	150T1	1	
U 1	ϟ IC,COMPARATOR,QUAD,14 PIN,SOIC	741561	6E570	LM339D	1	
U 3	ϟ IC,CMOS,DUAL D F/F,+EDG TRG,SOIC	782995	6E570	74HC74D	1	
U 4, 5, 10- U 12	ϟ IC,ARRAY,7 NPN DARLINGTON PAIRS,SOIC ϟ	821009 821009	31019	ULN-2004L	5	
U 6	ϟ IC,BPLR,TRUE RMS TO DC CONVERTER	707653	24355	AD637JD	1	
U 7	ϟ IC,OP AMP,JFET INPUT,DECOMP,SOIC	837237	27014	LF357M	1	
U 8	MERCURY/SATURN, ASSY TESTED PLASTIC	776195	89536	776195	1	
U 9	ϟ 2620A PROGRAMMED MICROPROCESSOR	886986	62786	886986	1	
U 13	ϟ IC,OP AMP,DUAL,LOW POWER,SOIC	929075	89536	929075	1	
U 14	ϟ IC,COMPARATOR,DUAL,LOW PWR,SOIC	837211	6E570	LM393D	1	
VR 1	ϟ STABILITY TESTED ZENER	387217	89536	387217	1	
VR 2, 3	ϟ ZENER,UNCOMP,6.0V,5%,20MA,0.2W,SOT-23	837161	04713	MMBZ5233BT1	2	
W 1	WIRE ASSY,(H)	834929	89536	834929	1	
W 2	WIRE ASSY,INPUT (L)	874086	89536	874086	1	
Y 1	CRYSTAL,3.6864MHZ,+-0.005%,HC-18U	570606	61429	HC-18/U-3.6864MHZ	1	
Y 2	CRYSTAL,3.84MHZ,+-0.05%,HC-18/U	650390	61429	HC-18/U-384MHZ	1	
Z 1	RES NET THK FILM TESTED	849984	89536	849984	1	
Z 2	RES NET THN FILM TESTED	884544	89536	884544	1	
Z 3	RES NET THK FILM TESTED	847363	89536	847363	1	
Z 4	RES NET THN F TESTED	851100	89536	851100	1	
NOTES:	ϟ Static sensitive part. 1. R10 and R11 are fusible resistors. To ensure safety, use exact replacement only.					


R39
C30
CR2
C29
R38
U13
R36
R29
R30
R37
C28
C26
CR1
R27
C21
C22
C23
U7
Q13
C15
C16
U6
Q7
Q5
Q3
U14
C31
K15
R44
Q15
Z3
C17
C6
CR4
R32
Q9
Q8
Q6
Q4
R16
Q12
Q14
R31
R28
VR3
R26
R25
R24
R23
Z1
R40
R41
R33
C33
C34
R20
R17
C7
C32
RT1
K16
Q10
C10
R34
U8
R22
C14
Q2
R14
R42
C11
Z4
TP9
R21
Z2
TP12
R18
K17
C27
C12
C8
TP11
J10
9
10
1
2
J2
R43
C18
R15
Q11
VR1
C9
R35
Y2
C13
TP1
R3
C1
L5
L6
VR2
TP13
C19
R24
R20
R19
C35
R6
R4
R1
U3
U1
C2
R5
R2
L7
K8
U10
C4
C3
Q1
R8
TP7
R7
TP2
TP3
TP4
TP5
TP6
L8
46
47
48
L9
L10
K9
U11
U9
Y1
TP8
R9
L11
C5
L12
U12
TP10
L13
C37
C38
K10
U5
U4
C36
L14
L15
R10
J1
L16
K11
K5
R11
L17
K1
L18
R13
L19
K12
K6
L20
K2
R12
L21
1
2
3
L22
K13
K7
L2
L1
L23
L24
K14
RU1
RED
W1
L3
K3
RU2
BLK
W2
L4

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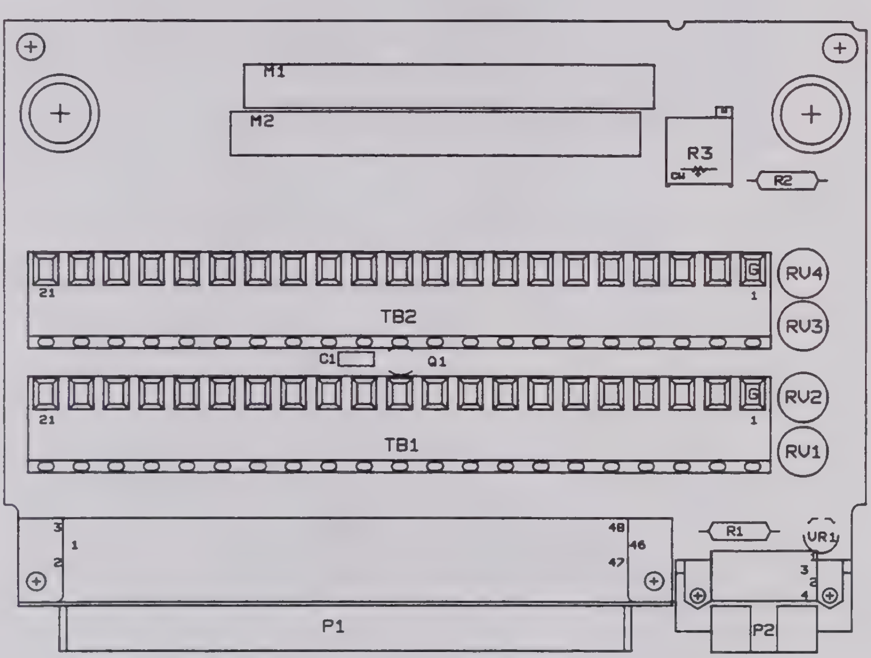
2620A-1603

Figure 6-6. A3 A/D Converter PCA

Table 6-7. A4 Analog Input PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1	CAP,CER,0.047UF,+-10%,50V,X7R	572263	04222	SR215C473KAA	1	
H 55	SCREW,PH,P,THD CUT,SS,4-24,.375	183574	89536	183574	2	
M 1, 2	HEADER,1 ROW,.156CTR,15 PIN	414458	27264	26-60-0150	2	
P 1	CONN,DIN41612,TYPE R,RT ANG,48 SCKT	867338	0G8R9	73-73-148-6899	1	
P 2	CONN,MICRO-RIBBON,REC,RT ANG,20 POS	876102	83486	20-5061-020-101-688	1	
Q 1	ϟ TRANSISTOR,SI,NPN,TEMP SENSOR TO-92	741538	04713	MTS103	1	
R 1	RES,MF,5.49K,+-1%,0.125W,100PPM	334565	91637	CMF-55 5491F T-1	1	
R 2	RES,MF,10K,+-1%,0.125W,25PPM	328120	91637	CMF-55 1002F T-9	1	
R 3	RES,VAR,CERM,50K,+-10%,0.5W	876573	80294	3296P-1-503	1	
RV 1- 4	VARISTOR,910,+-10%,1.0MA	876193	34371	V910LSX1399	4	
TB 1, 2	TERM STRIP,PWB,45 ANG,.197CTR,20 POS	875195	06229	99.204.0400	2	
VR 1	ϟ IC, 2.5V,100 PPM T.C.,BANDGAP REF	723478	27014	LM285BYZ-2.5	1	
NOTES:	ϟ Static sensitive part.					


M1
M2
R3
CW
R2
RV4
RV3
RV2
RV1
TB2
TB1
21
1
C1
Q1
R1
VR1
3
1
2
48
46
47
P1
P2
4

2620A-1604

Figure 6-7. A4 Analog Input PCA

Table 6-8. A5 (Option -05) IEEE-488 Interface PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1- 3	CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	04222	12065C104KATBA	3	
J 1	HEADER,2 ROW,.100CTR,RT ANG,26 PIN	512590	00779	1-87230-3	1	
J 2	HEADER,2 ROW,.100CTR,24 PIN	831834	0JNR4	66506-218	1	
R 1	ϟ RES,CERM,5.1K,+-5%,.125W,200PPM,1206	746560	91637	CRCW1206-5101JB02	1	
TP 1	TERM,UNINSUL,WIRE FORM,TEST POINT	781237	27918	TP102-01	1	
U 1	ϟ IC,NMOS,GPIB CONTROLLER,PLCC	887190	01295	TMS9914AFNL	1	
U 2	ϟ IC,LSTTL,OCTAL GPIB XCVR,SOIC	831651	01295	SN75160BDW	1	
U 3	ϟ IC,LSTTL,OCTAL GPIB XCVR,SOIC	831669	01295	SN75161BDW	1	
U 4	ϟ IC,CMOS,QUAD INPUT NAND GATE,SOIC	830703	6E570	74HC00D	1	
NOTES:	ϟ Static sensitive part. Attaching hardware and cable are listed below: H52 SCREW, PH,PSTL,LOCK,6-32 ,250 152140 MP56 CONN ACC,MICRO-RIBBON,SCREW LOCK KIT 836585 W4 IEEE,CABLE ASSY 874094					

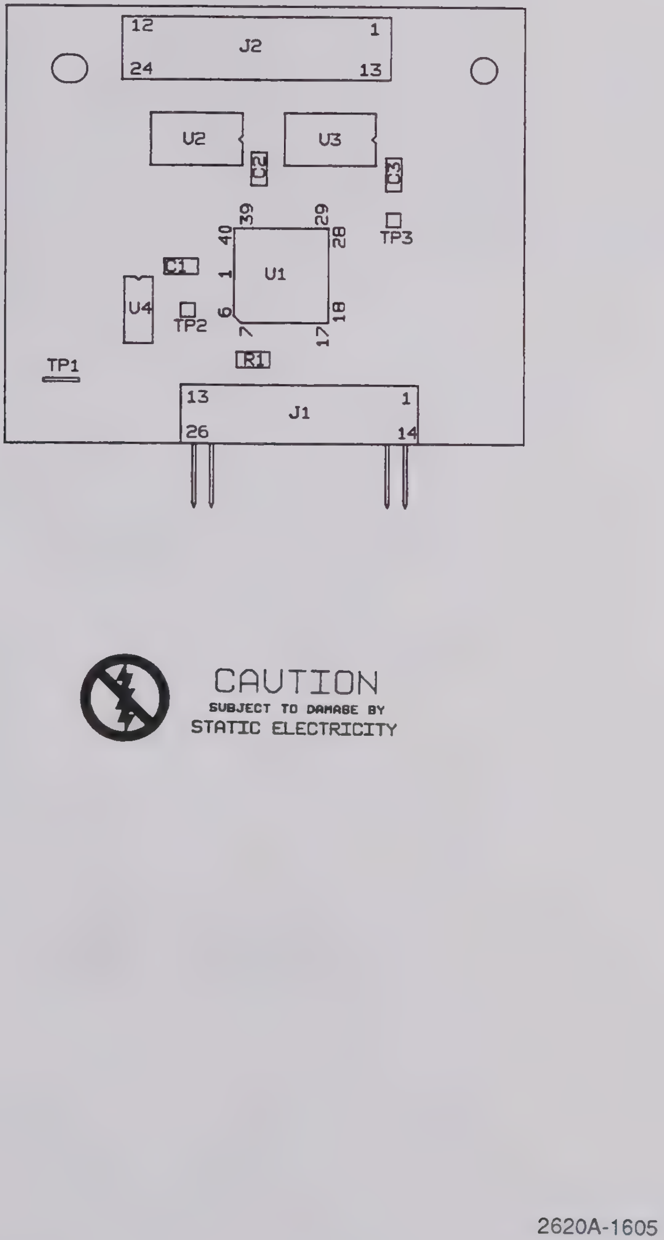

12
1
J2
24
13
U2
U3
C2
C3
39
29
40
28
TP3
C1
1
U1
U4
TP2
9
18
7
17
R1
TP1
13
1
J1
26
14
CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY
2620A-1605

Figure 6-8. A5 IEEE-488 Interface PCA (Option -05)

Table 6-9. 2625A A6 Memory PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1- 8	CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	04222	12065C104KATBA	8	
J 1	HEADER,2 ROW,.100CTR,RT ANG,26 PIN	512590	00779	1-87230-3	1	
TP 1, 2	TERM,UNINSUL,WIRE FORM,TEST POINT	781237	27918	TP102-01	2	
U 1	ϟ IC,CMOS,OCTAL D TRANSPARNT LATCH,SOIC	876235	6E570	74HC373D	1	
U 2	ϟ IC,CMOS,QUAD 2 INPUT AND GATE,SOIC	853317	6E570	74HC08D	1	
U 3	ϟ IC,CMOS,DUAL DIV BY 16 BIN CNTR,SOIC	837054	6E570	74HC393D	1	
U 4	ϟ IC,CMOS,4BIT BISTBL LTCH W/ENABL,SOIC	876243	6E570	74HC75D	1	
U 5	ϟ IC,CMOS,QUAD INPUT NAND GATE,SOIC	830703	6E570	74HC00D	1	
U 6, 7	ϟ IC,CMOS,128K X 8 SRAM,120 NSEC,NVM	876250	0B0A9	DS1245Y-100	2	
U 8	ϟ IC,CMOS,3-8 LINE DCDR W/ENABLE,SOIC	867726	6E570	74HC238D	1	
NOTES:	ϟ Static sensitive part.					

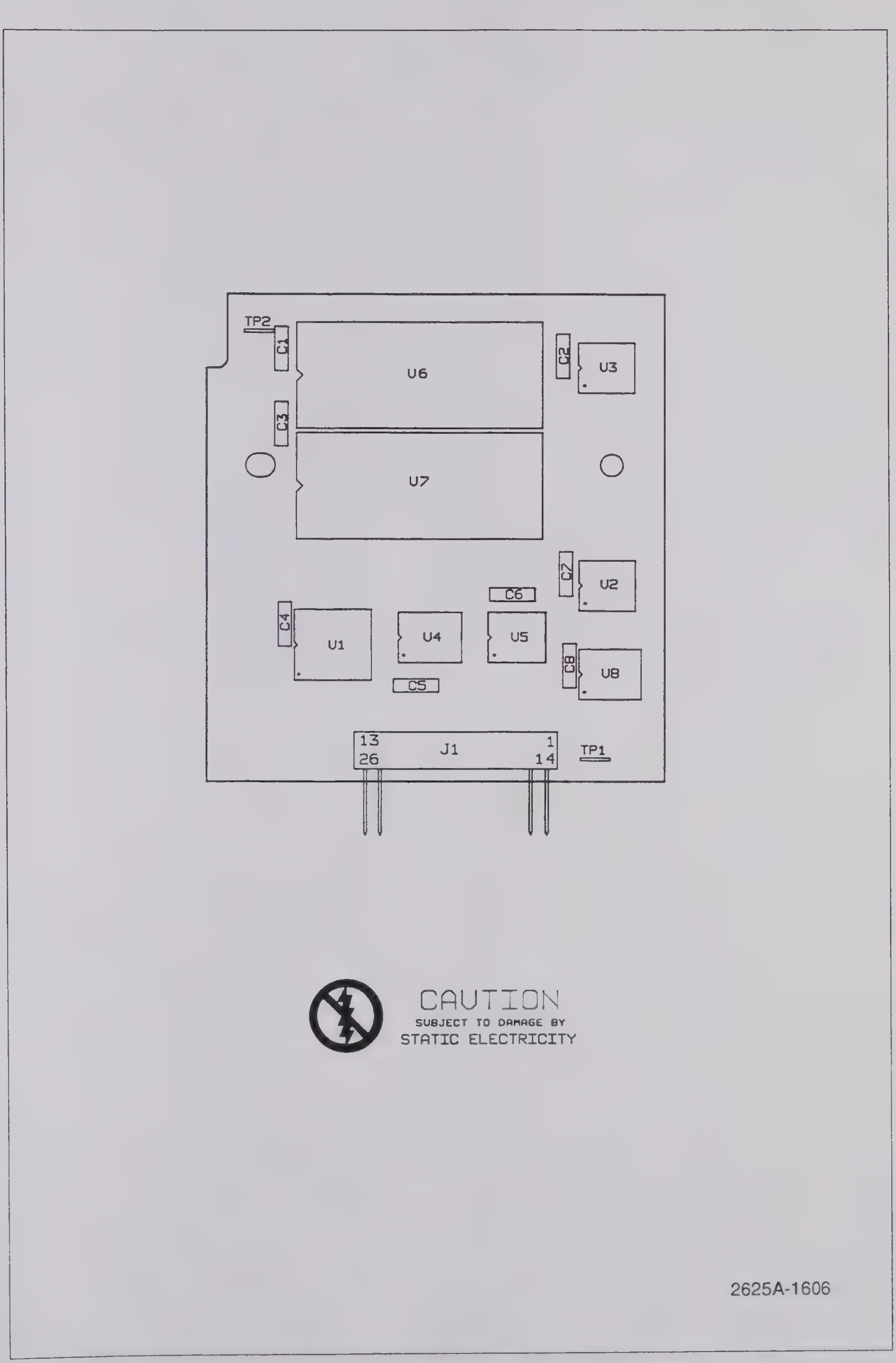
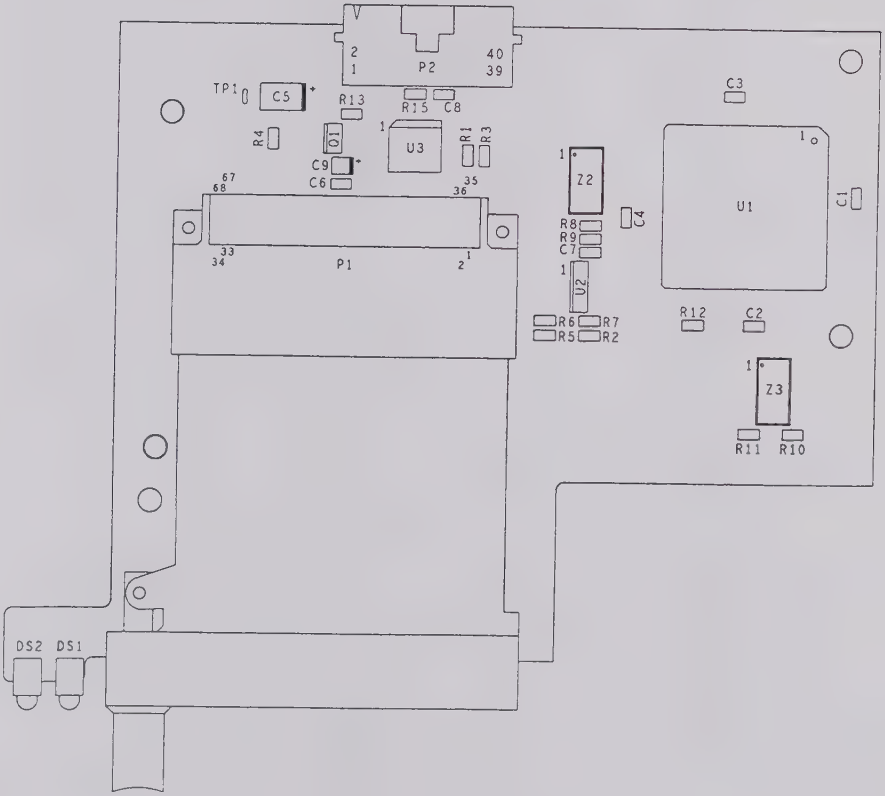

TP2
C1
U6
C2
U3
C3
U7
C7
U2
C6
C4
U1
U4
U5
C8
U8
C5
13
26
J1
1
14
TP1
CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY
2625A-1606

Figure 6-9. 2625A A6 Memory PCA

Table 6-10. 2635A A6 Memory Card I/F PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1- 4, 6- C 8	CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287 747287	04222	12065C104KATBA	7	
C 5	CAP,TA,47UF,+-20%,10V,7343	867580	56289	293D476X0010D2T or W	1	
C 9	CAP,TA,1UF,+-20%,35V,3528	866970	56289	293D105X0035B2T or W	1	
DS 1	LED,RED,RIGHT ANGLE T1,3.0 MCD	927389	28480	HLMP-1302-010	1	
DS 2	LED,YELLOW,RIGHT ANGLE T1,3 MCD	914242	28480	HLMP-1404-010	1	
P 1	CONN,MEMORY CARD,HEADER,RT ANG,68 PIN	914184	22526	89308-001	1	
P 2	HEADER,2 ROW,.050CTR,RT ANG,40 PIN	838540	00779	104069-6	1	
Q 1	ϟ TRANSISTOR,SI,N-MOS,2W,SOIC	914031	89536	914031	1	
R 1, 13	ϟ RES,CERM,1.5K,+-5%,.125W,200PPM,1206	746438	91637	CRCW1206-1501JB02	2	
R 2, 5- 7, R 12	ϟ RES,CERM,47K,+-5%,.125W,200PPM,1206 ϟ	746685 746685	91637	CRCW1206-4702JB02	5	
R 3, 4	ϟ RES,CERM,10K,+-5%,.125W,200PPM,1206	746610	91637	CRCW1206-1002JB02	2	
R 8, 9	ϟ RES,CERM,100,+-5%,.125W,200PPM,1206	746297	91637	CRCW1206-1000JB02	2	
R 10, 11	ϟ RES,CERM,360,+-5%,.125W,200PPM,1206	783290	91637	CRCW1206-3600JB02	2	
R 15	ϟ RES,CERM,33,+-5%,.125W,200PPM,1206	746248	91637	CRCW1206-33R0JB02	1	
TP 1	TERM,UNINSUL,WIRE FORM,TEST POINT	781237	27918	TP102-01	1	
U 1	ϟ IC,CMOS,CONTROLLER,MEMORY CARD,120QFP	914093	61271	MB86301PF	1	
U 2	ϟ IC,CMOS,QUAD BILATERAL SWITCH,SOIC	914098	04713	74HC4066AD	1	
U 3	ϟ GAL,PROGRAMMED,WAIT STATE TIMING	931915	89536	931915	1	
Z 2, 3	RES,CERM,SOIC,16 PIN,8 RES,100,+-2%	838086	91637	SOMC-1603-101G	2	
NOTES:	ϟ Static sensitive part.					


P2
2
1
40
39
TP1
C5
R13
R15
C8
C3
R4
Q1
1
U3
R1
R3
1
Z2
1
U1
C1
C9
C6
67
68
35
36
R8
R9
C7
C4
33
34
P1
1
2
1
U2
R6
R5
R7
R2
R12
C2
1
Z3
R11
R10
DS2
DS1

2635A-1606

Figure 6-10. 2635A A6 Memory Card I/F PCA

Manufacturers Federal Supply Codes

00779
AMP, Inc.
Harrisburg,PA

01295
Texas Instruments Inc.
Semiconductor Group
Dallas,TX

04222
AVX Kyocera Corp.
Myrtle Beach, SC

04713
Motorola Inc.
Semiconductor Products Sector
Phoenix, AZ

06229
Weiland Inc.
Formerly Electrovert Inc.
New Rochelle, NY

0B0A9
Dallas Semiconductor Corp.
Dallas, TX

0BW21
Noritake Co. Inc.
Burlington, MA

0D2A6
Mitsubishi Electronics America Inc.
Torrance, CA

0G8R9
Harting Electronik Inc.
Hoffman Estates, IL

0JNR4
Dupont Electronics
Wilmington, DE

0NFL0
Coiltronics Inc.
Pompano Beach, FL

17856
Siliconix Inc.
Santa Clara, CA

22526
DuPont, El DeNemours & Co. Inc.
DuPont Connector Systems
New Cumberland, PA

24355
Analog Devices Inc.
Norwood, MA

25088
Siemens Corp.
Iselin, NJ

25403
Philips Components
Formerly Amperex Electronic Corp.
Slatersville, RI

27014
National Semiconductor Corp.
Santa Clara, CA

27264
Molex Inc.
Lisle, IL

27918
Component Parts Corp.
Bellmore, NY

28213
Minnesota Mining & Mfg. Co.
Consumer Specialties Div. 3M Center
Saint Paul, MN

28480
Hewlett-Packard Co.
Corporate HQ
Palo Alto, CA

2M530
John Perine
Seattle, WA

31019
Allegro Microsystems Inc.
Formerly Sprague Electric Co.
Semiconductor Group
Willow Grove, PA

31918
ITT/Schadow Inc.
Eden Prairie, MN

33297
NEC Electronics USA Inc.
Electronic Arrays Inc. Div.
Mountain View, CA

34371
Harris Corp.
Semiconductor Sector
Military & Aerospace Div.
Melbourne, FL

Federal Supply Codes for Manufacturers

00779
AMP, Inc.
Harrisburg,PA

01295
Texas Instruments Inc.
Semiconductor Group
Dallas,TX

04222
AVX Kyocera Corp.
Myrtle Beach, SC

04713
Motorola Inc.
Semiconductor Products Sector
Phoenix, AZ

06229
Weiland Inc.
Formerly Electrovert Inc.
New Rochelle, NY

0B0A9
Dallas Semiconductor Corp.
Dallas, TX

0BW21
Noritake Co. Inc.
Burlington, MA

D2A6
Mitsubishi Electronics America Inc.
Torrance, CA

0G8R9
Harting Electronik Inc.
Hoffman Estates, IL

0JNR4
Dupont Electronics
Wilmington, DE

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Section 7

IEEE-488 Option -05

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INTRODUCTION 7-1.

The IEEE-488 Interface turns the Data Acquisition Unit 2620A into a fully programmable instrument for use with the IEEE Standard 488.1 (1987) interface bus (IEEE-488 bus). With the IEEE-488 Interface, the instrument can become part of an automated instrumentation system.

The IEEE-488 Interface cannot be used with the Hydra Data Logger (2625A).

THEORY OF OPERATION 7-2.

Functional Block Description 7-3.

The IEEE-488 Assembly (A5) requires power supply voltages, address, data and control signals from the instrument Main Assembly (A1) to operate. The A5 assembly implements the circuitry necessary to satisfy the IEEE-488.1 standard for programmable instrumentation.

IEEE-488 PCA DETAILED CIRCUIT DESCRIPTION (2620A Only) 7-4.

The IEEE-488 PCA comprises the following functional blocks: the Main PCA Connector, the IEEE-488 Controller, and the IEEE-488 Transceivers and Connector. These three blocks are described in the following paragraphs. Refer to Section 8 for a schematic diagram of the IEEE-488 PCA.

Pin numbering for the IEEE Controller (A5U1) differs somewhat on early production units. All A5U1 pin references in this section relate to newer production units. Differences for early production units can be identified by referencing the manufacturer's number on the A5U1 chip with the information provided in Table 7-1.

Table 7-1. A5U1 Pin Differences

WD9914 (Early Production A5U1)		TMS9914A (Newer Production A5U1)	
REFERENCE	NAME	NAME	REFERENCE
A5U1-1	ACCRQ*	(nc)	A5U1-1
A5U1-2	ACCGR*	ACCRQ*	A5U1-2
A5U1-3	CE*	ACCGR*	A5U1-3
A5U1-4	WE*	CE*	A5U1-4
A5U1-5	DBIN	WE*	A5U1-5
A5U1-6	(nc)	DBIN	A5U1-6
A5U1-17	(nc)	D1	A5U1-17
A5U1-19	D1	D0	A5U1-19
A5U1-20	D0	CLK	A5U1-20
A5U1-21	CLK	RESET*	A5U1-21
A5U1-22	RESET*	VSS	A5U1-22
A5U1-23	VSS	TE	A5U1-23
A5U1-24	TE	REN	A5U1-24
A5U1-25	REN	IFC	A5U1-25
A5U1-26	IFC	NDAC	A5U1-26
A5U1-27	NDAC	NRFD	A5U1-27
A5U1-28	NRFD	(nc)	A5U1-28

Main PCA Connector 7-5.

The IEEE-488 PCA interfaces to the Main PCA through a 26-pin, right-angle connector (A5J1). This connector routes the 8-bit data bus, the lower three bits of the address bus, memory control, system clock, and address decode signals from the Main PCA to the IEEE-488 PCA. The IRQ2* interrupt request signal is routed from the IEEE-488 PCA to the Main PCA. The IEEE-488 PCA is powered by the +5.1V dc power supply (VCC). The IEEE-488 PCA is sensed by the Microprocessor on the Main PCA through the connection of logic common to the option sense signal OPS* (A5J1-22).

IEEE-488 Controller 7-6.

The IEEE-488 Controller (A5U1) is an integrated circuit that performs the transfer of information between the IEEE-488 standard bus and the Main PCA Microprocessor (A1U4). Once it has been programmed by the Microprocessor via the eight-register microprocessor interface, A5U1 performs IEEE-488 bus transactions independently until it must interrupt the Microprocessor for additional information or data.

The IEEE-488 Controller is clocked by a 1.2288-MHz square-wave clock. This clock (A5U1-20) is generated by the Microprocessor. The IEEE-488 Controller uses this clock to run the internal state machines that handle IEEE-488 bus transactions. The IEEE-488 Controller is reset when the system RESET* signal (A5U1-21) is low.

For each character that it receives or transmits, the IEEE-488 Controller generates an interrupt to the Microprocessor. These interrupts are generated by driving the open-drain interrupt output A5U1-10 low. This signal drives the IRQ2* input to the Microprocessor low. When the Microprocessor responds to the interrupt and takes the necessary actions by reading and writing registers in the IEEE-488 Controller, A5U1-10 goes high again. Resistor A5R1 provides a pull-up termination on open-drain interrupt output A5U1-10.

When the Microprocessor performs a memory cycle to the IEEE-488 Controller, the lower three bits of the address bus select the register being accessed in A5U1. When a memory read cycle is performed, chip-enable A5U1-4 goes low, and A5U1-6 (DBIN) goes high. These actions enable A5U1, driving the contents of the selected register onto the data bus to the Microprocessor. When a memory write cycle is performed, chip-enable A5U1-4 goes low, and A5U1-5 (WE*) goes first low and then high to latch the data being driven from the Microprocessor into the IEEE-488 Controller.

The IEEE-488 Controller interfaces to the IEEE-488 Transceivers using an eight-bit data bus, eight interface signals, and two transceiver control signals (A5U1-33 and A5U1-23).

The controller-in-charge signal (A5U1-33), which should always be high, controls the direction of the SRQ, ATN, IFC, and REN IEEE-488 transceivers in A5U3.

The talk enable output (A5U1-2) is either low when the IEEE-488 Controller is not addressed to talk or high when the controller is addressed to talk. This signal determines the direction of all IEEE-488 Transceivers except SRQ, ATN, IFC, and REN.

IEEE-488 Transceivers/Connector 7-7.

The IEEE-488 Transceivers (A5U2 and A5U3) are octal transceivers that are specifically designed to exhibit the proper electrical drive characteristics to meet the IEEE-488 standard. These transceivers are configured to match the control signals available on the IEEE-488 Controller. Assuming that A5U1-33 is always high, Table 7-2 describes the transceiver direction control. The IEEE-488 Transceivers connect to a 24-position connector (A5J2), which mates with the ribbon cable leading to the IEEE-488 connector mounted at the rear of the instrument chassis.

GENERAL MAINTENANCE 7-8.

Removing the IEEE-488 Option 7-9.

Remove the instrument cover as shown in Figure 7-1. Then remove the IEEE-488 Option with the following procedure:

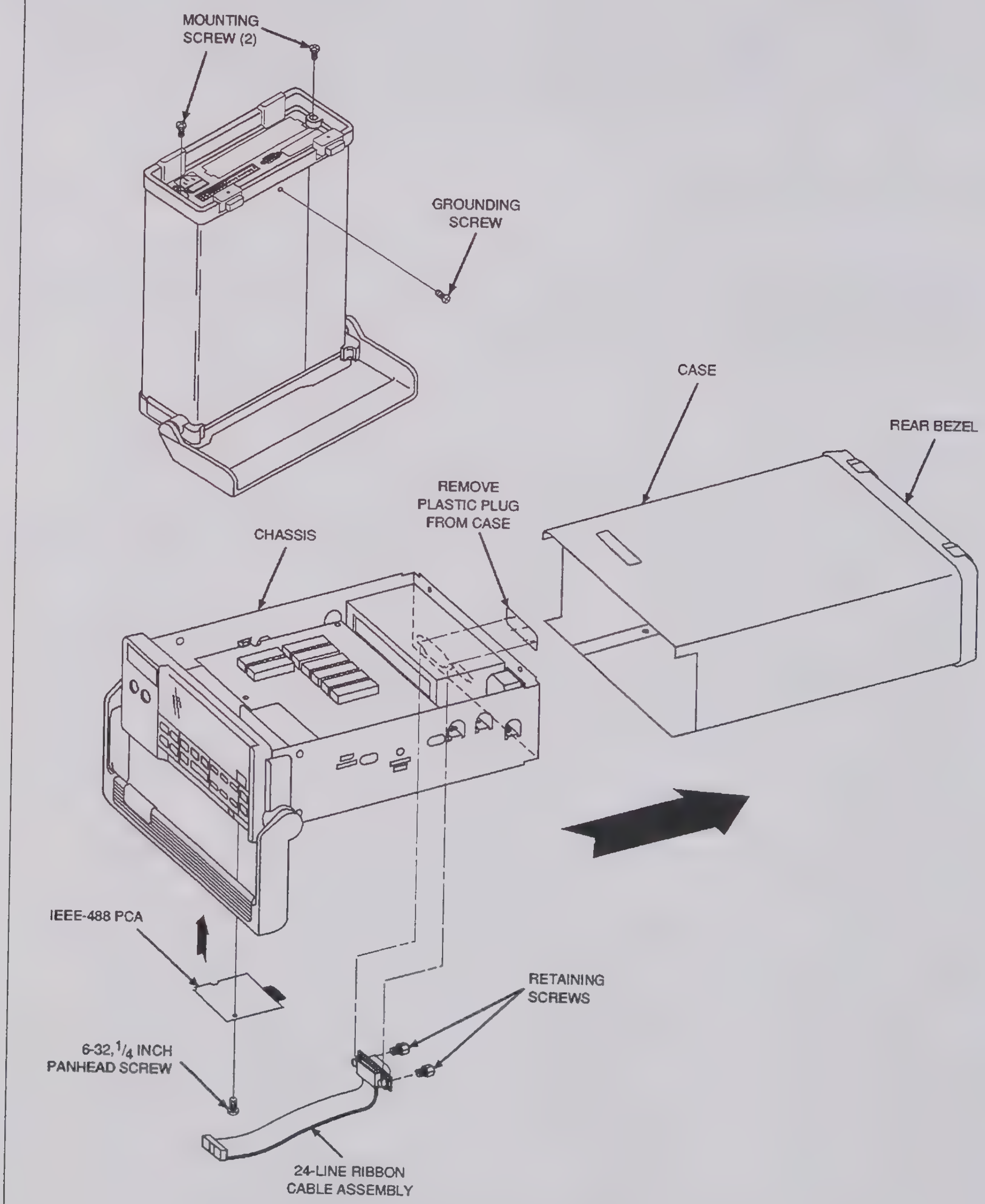
NOTE

Parts referenced by letter (e.g., A) are shown in Section 3 (Figure 3-4.)

1. From the bottom of the instrument, locate the IEEE-488 PCA (N). This pca is connected to the front of Main PCA, with a ribbon cable (O) leading across both pca's to the Rear Panel. Refer to Figure 7-1.
2. Use needle nose pliers to disconnect the 24-line cable assembly at the IEEE-488 PCA, alternately pulling on each end of the cable connector. Leave the other end of this cable attached to its Rear Panel connector.
3. Remove the 6-32, 1/4-inch panhead Phillips screw (P) securing the IEEE-488 PCA. See Figure 7-1.
4. Disengage the IEEE-488 PCA by sliding it away from the Main PCA.

Table 7-2. IEEE-488 Transceiver Control

TRANSCEIVER	TE = 0 (LISTENER)	TE = 1 (TALKER)
DI01..DI08	Receiver	Transmitter
SRQ	Transmitter	Transmitter
ATN	Receiver	Receiver
EOI	Receiver	Receiver (ATN = 0)
-	Receiver	Transmitter (ATN = 1)
DAV	Receiver	Transmitter
NRFD	Transmitter	Receiver
NDAC	Transmitter	Receiver
IFC	Receiver	Receiver
REN	Receiver	Receiver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GROUNDING SCREW
CASE
REAR BEZEL
REMOVE PLASTIC PLUG FROM CASE
CHASSIS
IEEE-488 PCA
RETAINING SCREWS
6-32, 1/4 INCH PANHEAD SCREW
24-LINE RIBBON CABLE ASSEMBLY

Figure 7-1. Installation

Installing the IEEE-488 Option 7-10.

1. Place the IEEE-488 PCA into position so that the edge of the pca fits in the chassis guide. Then line up connecting pins with the matching connector on the Main PCA, and slide the pca into position.

2. Install the single 6-32, 1/4-inch panhead Phillips head screw in the corner of the IEEE-488 PCA.

3. If necessary, attach the rear panel connector using 7 mm nut driver.

4. At the pca, attach the ribbon cable leading from the rear panel connector.

PERFORMANCE TESTING 7-11.

Use the following performance test program to verify operation of the IEEE-488 Interface. This program is written for use with the Fluke 1722A Instrument Controller and its interpreted BASIC language. The program may be adapted to the language of any IEEE-488 controller.

```
140 IA% = 0%                          ! instrument IEEE address
150 S% = -1%                          ! initialize spl response
160 TERM                              ! terminate input only on EOI
170 INIT PORT 0                       ! initialize IEEE-488 bus
180 CLEAR @@IA%                       ! selective device clear
190 PRINT @@IA%,"*cls"                ! clear instrument status
200 ON SRQ GOTO 530                   ! enable SRQ interrupt
210 PRINT @@IA%,"*cls;*sre 16;*idn?"  ! SRQ on Message Available
220 WAIT 500% FOR SRQ                 ! allow time to execute commands
230 IF S% >= 0% THEN 260
240   PRINT "Instrument failed to generate a Service Request"
250   STOP
260 PRINT "Serial Poll =";S%;"(should be 80)."
270 PRINT "Identification Query Response = ";R$
280 STOP
500 !
510 ! Service Request interrupt
520 !
530 S% = SPL(IA%)                     ! get instrument serial poll status
540 IF S% AND 16% THEN 550 ELSE 560
550   INPUT LINE @IA%,R$              ! if MAV set get the response
560 RESUME 230                        ! end of SRQ interrupt
999 END
```

This performance test communicates to an instrument that has been configured for IEEE-488 operation at address 0. Lines 170 and 180 initialize the IEEE-488 bus and send a selective device clear to the instrument. A multiple byte command is sent to the instrument (by line 190) to clear the instrument status. Another command sequence (including a query) is sent to the instrument by line 210; the instrument asserts Service Request (SRQ) to signal that a response is available. Lines 530 through 560 first poll the instrument for status, then input the response from the instrument. Lines 230 through 270 test for proper operation and print the results.

TROUBLESHOOTING 7-12.

Power-Up Problems 7-13.

The following discussion identifies probable fault areas if the installation of an IEEE-488 Option causes power-up failure for the instrument. The problem is probably a short on A5J1; the Microprocessor on the Main Assembly is prevented from accessing ROM and RAM correctly.

- First check if VCC is shorted to GND on the IEEE Assembly.
- The short may also be caused by an interface signal to either VCC, GND, or another interface signal. The logical signals to check are D7 .. D0, A2 .. A0, RD*, IEEE*, WR*, E, RESET*, and IRQ2*.
- The short may be due to a CMOS input that has been damaged due to static discharge; the short is then detectable only when the circuit is powered up. Use an oscilloscope to check activity on each of the interface signals. Verify that signals are able to transition normally between 0 and 5V dc.

Communication Problems 7-14.

FAILURE TO SELECT IEEE-488 OPTION 7-15.

IEEE-488 Interface selection procedures are described in Section 3 of the Hydra User Manual.

If the IEEE-488 option is not detected by instrument software, there may be a problem with the OPS* signal. The IEEE option grounds the OPS* signal (A5J1-22), which is normally pulled up to VCC on the instrument Main PCA. The Microprocessor determines that the IEEE-488 option is not installed if OPS* (A1U4-29) is high during the power-up option detection.

FAILURE TO HANDSHAKE ON IEEE-488 BUS 7-16.

After power-up or when the active computer interface is changed from RS-232 to IEEE-488, the Microprocessor sends six write cycles to initialize A5U1. The IRQ2* interrupt is then enabled, and the serial poll status byte is initialized. At this point, the IEEE-488 option is ready to respond to transactions on the IEEE-488 bus.

FAILURE TO ENTER REMOTE 7-17.

If the IEEE-488 option does not enter remote, check that the remote/local control circuit is operating properly. When the IEEE-488 option is the active instrument interface, the remote/local control state is polled by the Microprocessor approximately every 400 ms. Normally, A5U1-4 goes low for approximately 800 ns during the read cycle that checks the state of A5U1. If D(0) (A5U1-11) is low during the read cycle, A5U1 is in the local state. If A5U1-11 is high during the read cycle, A5U1 is in the remote state. When A5U1 indicates that it is in remote, the REM indicator on the display is turned on.

FAILURE TO RECEIVE MULTIPLE CHARACTER COMMANDS 7-18.

Monitor the IRQ2* interrupt signal from A5U1-10 during attempts to communicate with the instrument. Each byte received with the ATN signal (A5U1-31) high should cause the interrupt signal to go low. Verify that the signal arrives at A5J1 properly. An interrupt not detected by A1U4 will remain low indefinitely. A5U1-10 will go high only when both the interrupt is detected and the received byte is removed from A5U1 by A1U4.

FAILURE TO TRANSMIT QUERY RESPONSES 7-19.

Check that TE (A5U1-23) goes high when the interface is addressed to talk. This signal must go high to allow the bus interface transceivers to change the direction of DIO1 through DIO8, EOI, DAV, NRFD, and NDAC. Verify that each of these signals passes through A5U2 and A5U3 properly.

FAILURE TO GENERATE AN END OR IDENTIFY (EOI) 7-20.

When the IEEE-488 option sends the Line Feed termination character at the end of a response, the EOI signal should also be set true. When EOI is true, A5U1-30 should go low. Follow this signal from A5J2 through A5U3 to A5U1.

FAILURE TO GENERATE A SERVICE REQUEST (SRQ) 7-21.

When a Service Request is being generated, A5U1-32 should be low. Follow this signal through A5U3 to connector A5J2. When a Serial Poll (SPL) is performed by the IEEE-488 bus controller, A5U1-32 will go high again.

NOTE

If the instrument is in the remote state without front panel lockout (i.e., REMS), a service request can be sent from the front panel by pressing the up arrow button.

LIST OF REPLACEABLE PARTS 7-22.

Refer to Section 6 for an illustrated parts list of the IEEE-488 Option.

SCHEMATIC DIAGRAM 7-23.

The schematic diagram for the IEEE-488 Option is included in Section 8 of this manual.

Section 8

Schematic Diagrams

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8-1	A1 Main PCA (2620A/2625A)	8-3
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8-3	A2 Display PCA	8-21
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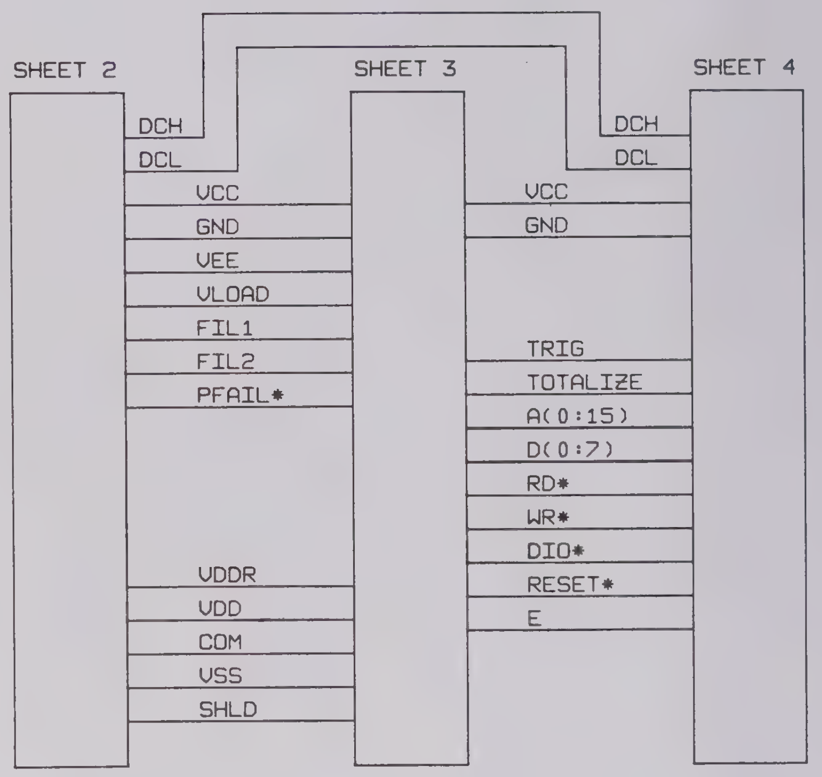
8-6	A5 (Option -05) IEEE-488 Interface PCA	8-31
8-7	A6 Memory PCA (2625A)....................................	8-33
8-8	A6 Memory Card I/F PCA (2635A)	8-35

NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS ARE 1/4W,5%.
   ALL CAPACITOR VALUES ARE IN MICROFARADS.

REFERENCE DESIGNATIONS		
LAST USED		NOT USED
AR	AR3	
C	C59	
CR	CR19	
J	J6	
L	L2	
P	P10	P1-P9
Q	Q9	
R	R64	
RT	RT1	
RV	RV1	
S	S1	
T	T2	
TP	TP32	TP21-29
U	U29	
VR	VR4	
W	W1	
Y	Y1	
Z	Z3	

INTERCONNECT DIAGRAM


SHEET 2
SHEET 3
SHEET 4
DCH
DCL
VCC
GND
VEE
VLOAD
FIL1
FIL2
PFAIL*
VDDR
VDD
COM
VSS
SHLD
DCH
DCL
VCC
GND
TRIG
TOTALIZE
A(0:15)
D(0:7)
RD*
WR*
DIO*
RESET*
E

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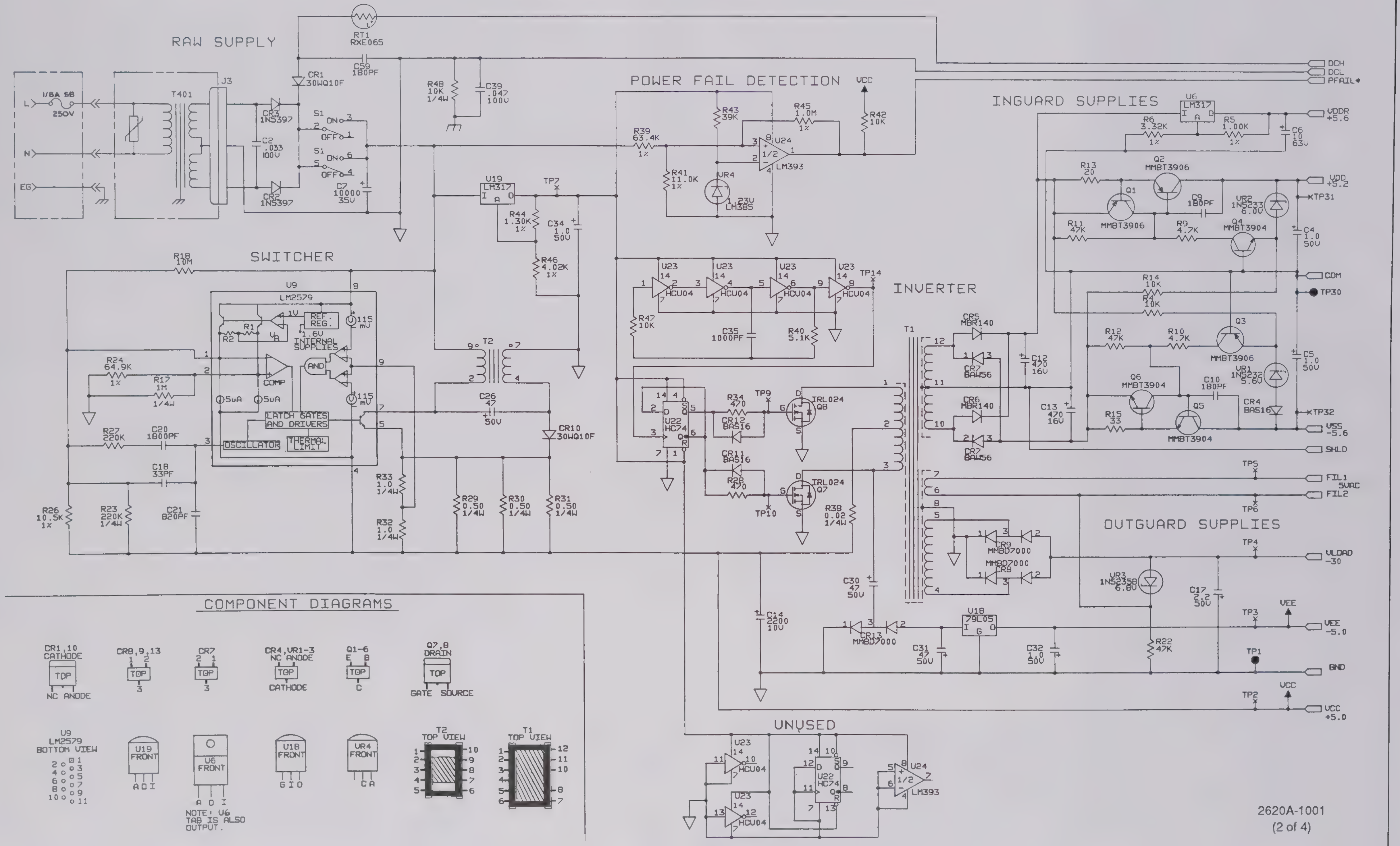
(1 of 4)

Figure 8-1. A1 Main PCA (2620A/2625A)

REF RES	POWER SUPPLY PIN NUMBERS				
	VCC (5.1V dc)	GND	VEE (5.0V dc)	VDDR (5.6V dc)	COM
A1AR1	8	4	–	–	–
A1AR2	4	11	–	–	–
A1AR3	4	11	–	–	–
A1U1	8	5	–	–	–
A1U2	14,16	1,2,5,7,26	–	–	–
A1U3	26,28	14	–	–	–
A1U4	5,36	1,2,6,18,35,45,54	–	–	–
A1U5	5	–	–	1	–
A1U6	–	–	–	3	–
A1U7	–	–	–	–	4
A1U8	28	14	–	–	–
A1U9	4	–	–	–	–
A1U10	14	7	–	–	–
A1U11	16	5,8	–	–	–
A1U12	14	7	–	–	–
A1U13	20	10	–	–	–
A1U14	4,9,10,14	7	–	–	–
A1U15	14	7	–	–	–
A1U16	20	10	–	–	–
A1U18	–	2	3	–	–
A1U20	16	8	–	–	–
A1U21	13,14	7	–	–	–
A1U22	–	7,11,12	–	–	–
A1U23	–	7,11,13	–	–	–
A1U24	–	4,5,6	–	–	–
A1U25	1,16	2,6,9,14	8	–	–
A1U26	20	10	–	–	–
A1U28	14	7	–	–	–
A1U29	16	8,15	–	–	–
A1Z2	16	–	–	–	–


RAW SUPPLY
1/8A SB
250V
L
N
EG
T401
J3
CR1 30WQ10F
CR3 1N5397
CR2 1N5397
C2 .033 100V
S1 ON OFF
C7 10000 35V
RT1 RXE065
C59 180PF
R48 10K 1/4W
C39 .047 100V
POWER FAIL DETECTION
VCC
R39 63.4K 1%
R43 39K
R45 1.0M 1%
R42 10K
U24 1/2 LM393
R41 11.0K 1%
VR4 1.23V LM385
U19 LM317
TP7
R44 1.30K 1%
C34 1.0 50V
R46 4.02K 1%
SWITCHER
R18 10M
U9 LM2579
REF. REG.
1.6V
INTERNAL SUPPLIES
AND
COMP
5uA
115 mV
LATCH GATES AND DRIVERS
OSCILLATOR
THERMAL LIMIT
R1
R2
R24 64.9K 1%
R17 1M 1/4W
R27 220K
C20 1800PF
C18 33PF
R26 10.5K 1%
R23 220K 1/4W
C21 820PF
T2
C26 47 50V
CR10 30WQ10F
R33 1.0 1/4W
R32 1.0 1/4W
R29 0.50 1/4W
R30 0.50 1/4W
R31 0.50 1/4W
U23 HCU04
TP14
R47 10K
C35 1000PF
R40 5.1K
INVERTER
T1
U22 HC74
R34 470
TP9
CR12 BAS16
CR11 BAS16
R28 470
TP10
IRL024 Q8
IRL024 Q7
R38 0.02 1/4W
C30 47 50V
C14 2200 10V
CR5 MBR140
CR7 BAW56
CR6 MBR140
C12 470 16V
C13 470 16V
INGUARD SUPPLIES
U6 LM317
R6 3.32K 1%
R5 1.00K 1%
C6 10 63V
R13 20
Q1 MMBT3906
Q2 MMBT3906
C9 180PF
VR2 1N5233 6.0V
R11 47K
R9 4.7K
Q4 MMBT3904
C4 1.0 50V
R14 10K
R4 10K
R12 47K
R10 4.7K
Q3 MMBT3906
C5 1.0 50V
VR1 1N5232 5.6V
Q6 MMBT3904
C10 180PF
R15 33
Q5 MMBT3904
CR4 BAS16
TP31
TP30
TP32
VDDR +5.6
VDD +5.2
COM
VSS -5.6
SHLD
DCH
DCL
PFAIL
FIL1
5VAC
FIL2
TP5
TP6
OUTGUARD SUPPLIES
CR9 MMBD7000
CR8 MMBD7000
VR3 1N5235B 6.8V
C17 2.2 50V
TP4
VLOAD -30
TP3
VEE
VEE -5.0
U18 79L05
CR13 MMBD7000
C31 47 50V
C32 1.0 50V
R22 47K
TP1
GND
TP2
VCC
VCC +5.0
UNUSED
U23 HCU04
U22 HC74
U24 1/2 LM393
COMPONENT DIAGRAMS
CR1,10 CATHODE
TOP
NC ANODE
CR8,9,13
CR7
CR4,VR1-3 NC ANODE
CATHODE
Q1-6 E B C
Q7,8 DRAIN
GATE SOURCE
U9 LM2579 BOTTOM VIEW
U19 FRONT A O I
U6 FRONT A O I
NOTE: U6 TAB IS ALSO OUTPUT.
U18 FRONT G I O
VR4 FRONT C A
T2 TOP VIEW
T1 TOP VIEW

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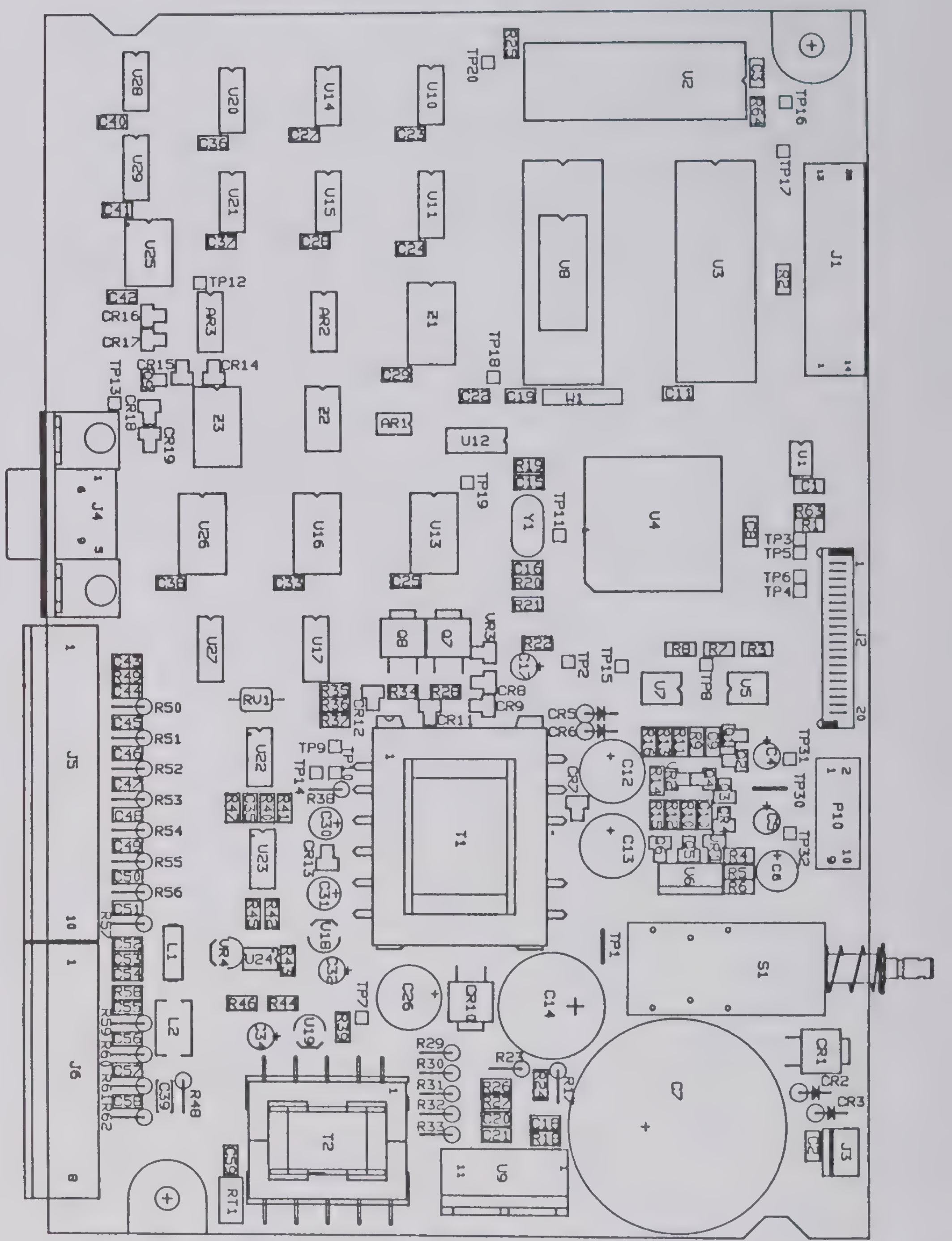
(2 of 4)

Figure 8-1. A1 Main PCA (2620A/2625A) (cont)


U28
U29
U25
U20
U21
U14
U15
U10
U11
U2
U8
U3
J1
TP12
TP13
TP16
TP17
TP18
TP19
TP20
AR3
AR2
AR1
Z1
Z2
Z3
CR14
CR15
CR16
CR17
CR18
CR19
W1
U12
U1
J4
U26
U16
U13
Y1
TP11
U4
TP3
TP5
TP6
TP4
J2
U27
U17
Q8
Q7
VR3
TP2
TP15
TP8
U7
U5
R50
R51
R52
R53
R54
R55
R56
R57
J5
RV1
CR8
CR9
CR11
CR12
CR5
CR6
CR7
U22
TP9
TP14
R38
C30
CR13
U23
C31
U18
T1
C12
C13
TP31
TP30
TP32
P10
U6
C8
L1
L2
VR4
U24
TP7
TP1
C26
CR10
C14
S1
J6
R59
R60
R61
R62
C39
R48
U19
T2
R29
R30
R31
R32
R33
R23
R17
U9
C7
CR1
CR2
CR3
J3
RT1

2620A-1601

NOTE: TP2-TP20, TP31, TP32, W1 ARE NOT COMPONENTS.

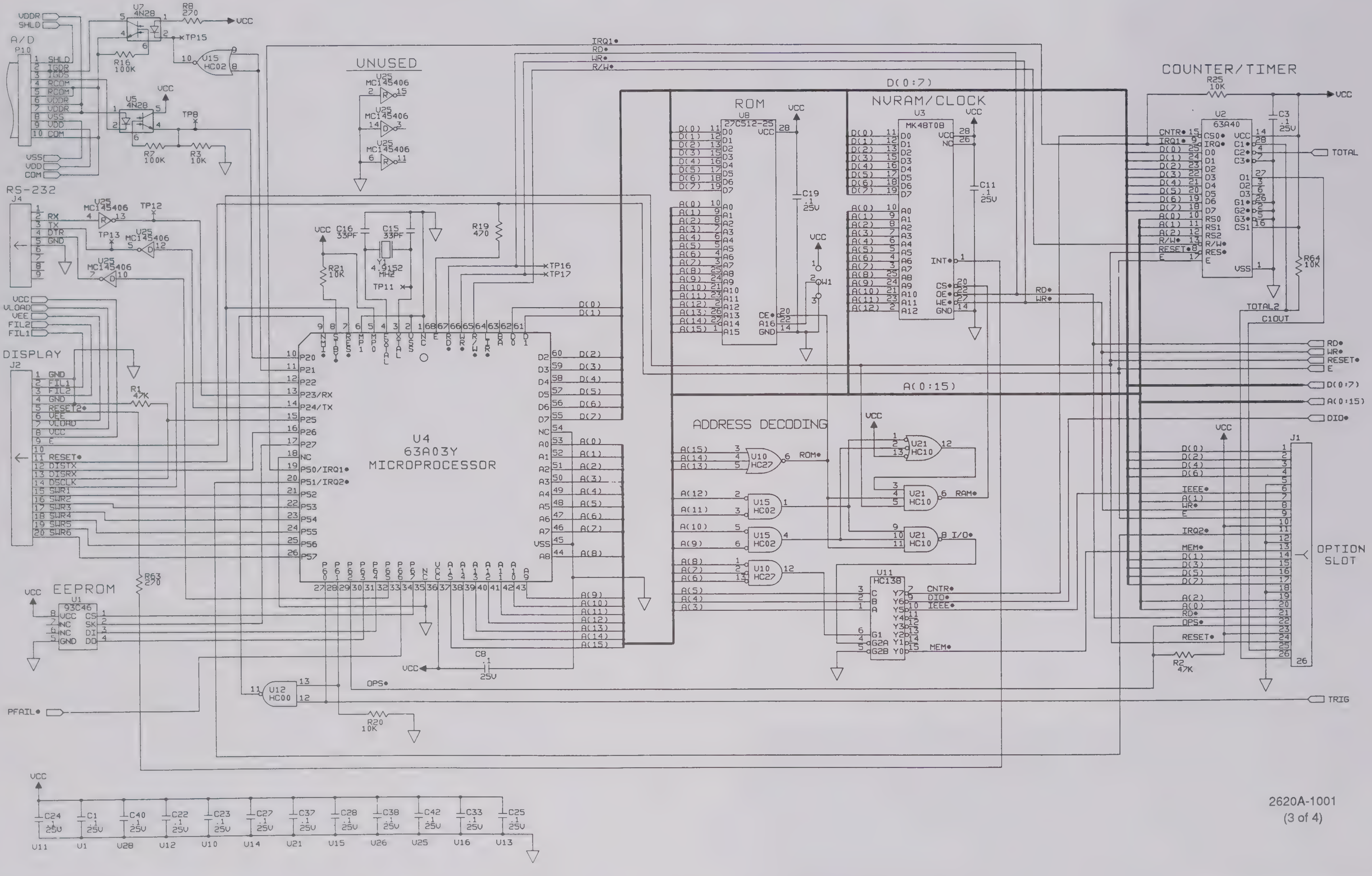
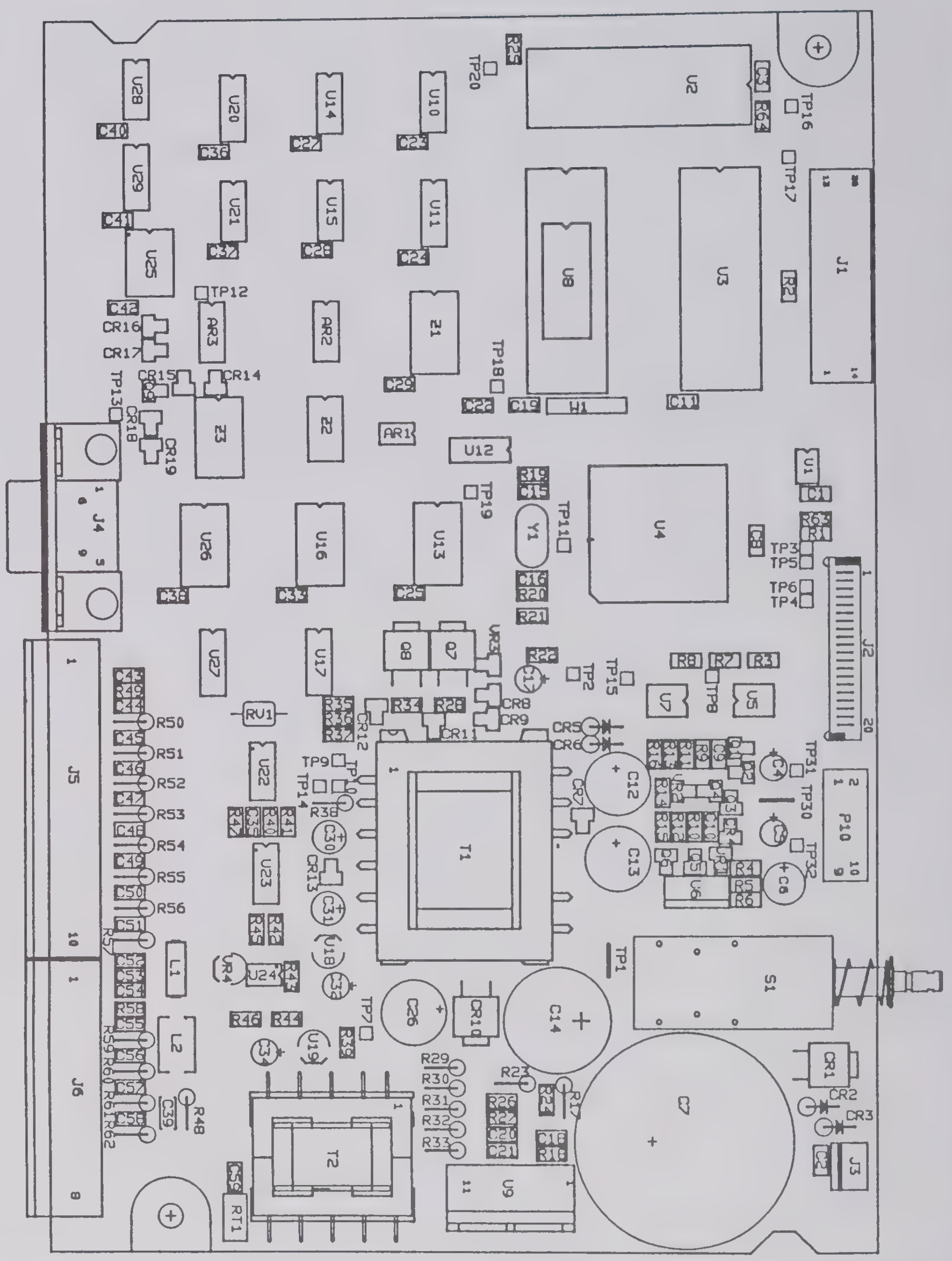

A/D
P10
RS-232
J4
DISPLAY
J2
EEPROM
U1
93C46
UNUSED
U25
MC145406
U7
4N28
U5
4N28
U15
HC02
U4
63A03Y
MICROPROCESSOR
U12
HC00
ROM
U8
27C512-25
NVRAM/CLOCK
U3
MK48T08
D(0:7)
A(0:15)
ADDRESS DECODING
U10
HC27
U21
HC10
U11
HC138
COUNTER/TIMER
U2
63A40
OPTION SLOT
J1
ROM•
RAM•
I/O•
IRQ1•
RD•
WR•
R/W•
RESET•
E
DIO•
TOTAL
TRIG
PFAIL•
OPS•
VCC
2620A-1001
(3 of 4)

Figure 8-1. A1 Main PCA (2620A/2625A) (cont)


U28
U20
U14
U10
U2
U29
U21
U15
U11
U25
U8
U3
J1
AR3
AR2
Z1
Z3
Z2
AR1
U12
U1
J4
U26
U16
U13
Y1
U4
U27
U17
Q8
Q7
J2
J5
RV1
U22
T1
C12
C13
P10
U23
U18
U24
L1
L2
C26
CR10
C14
S1
J6
T2
U19
U9
C7
CR1
J3
RT1
TP1
TP12
TP13
TP16
TP17
TP18
TP19
TP20
R50
R51
R52
R53
R54
R55
R56
R48
R29
R30
R31
R32
R33

2620A-1601

NOTE: TP2-TP20,TP31,TP32,W1 ARE NOT COMPONENTS.

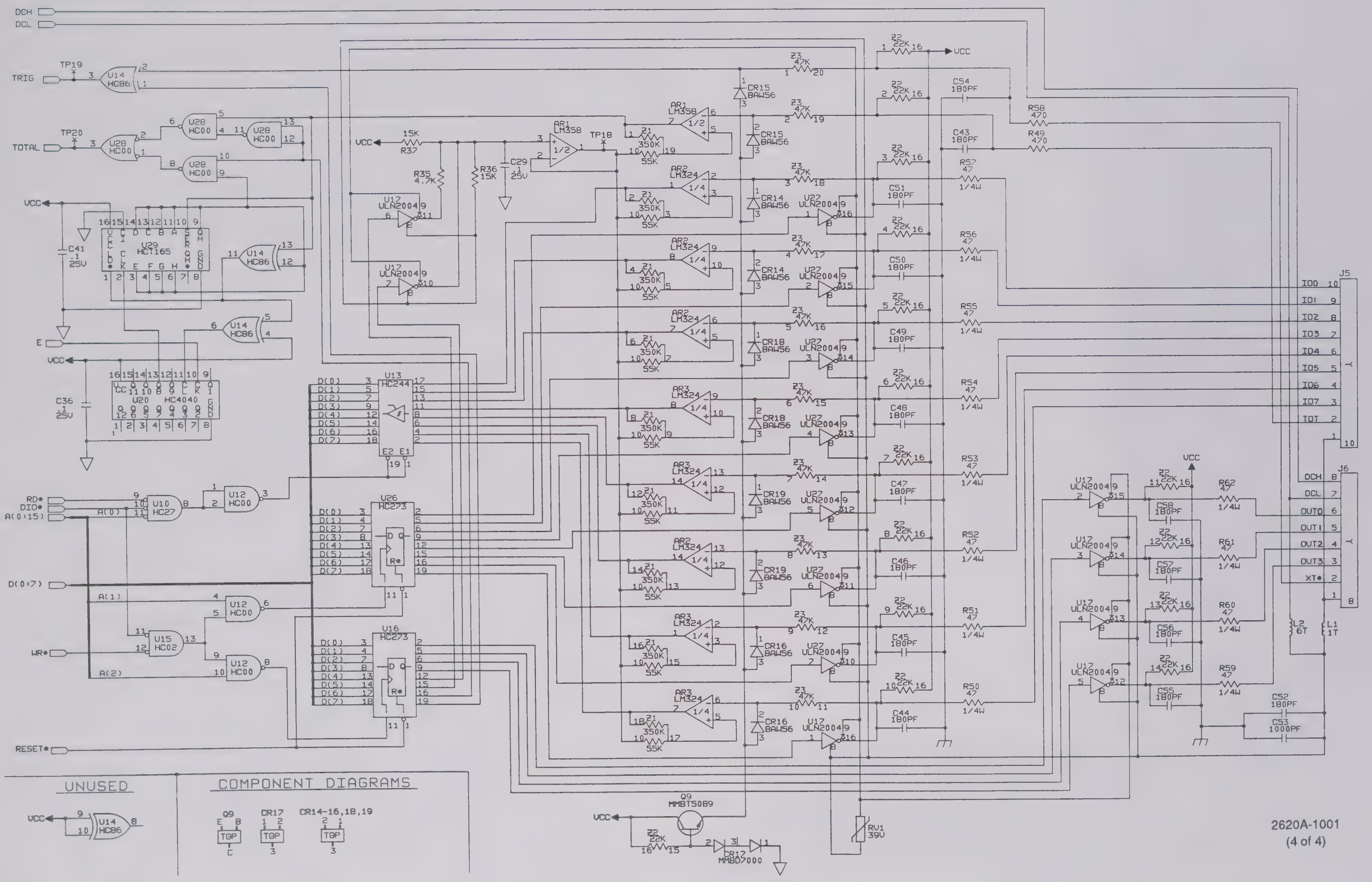
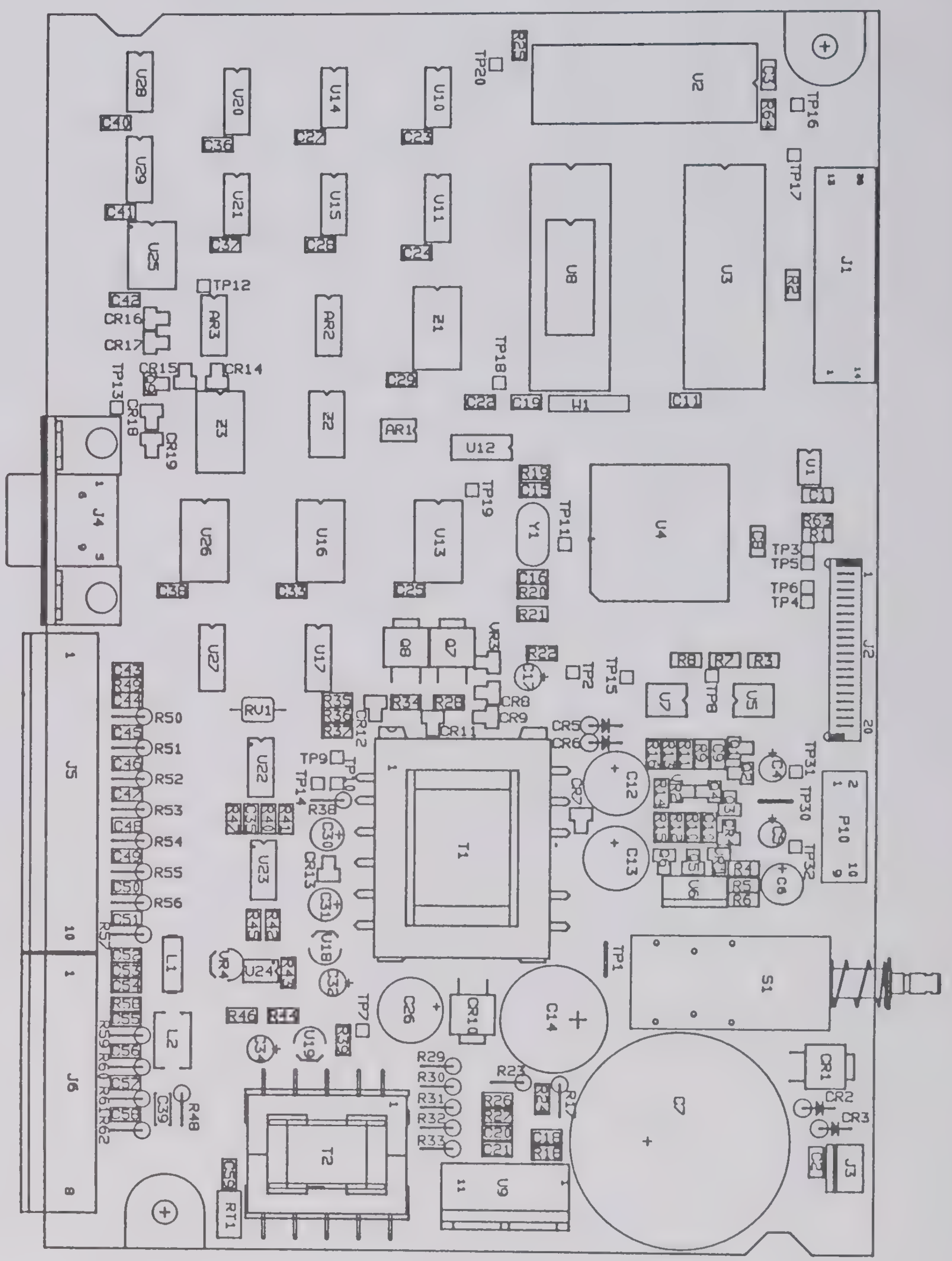

DCH
DCL
TRIG
TP19
TOTAL
TP20
VCC
E
RD•
DIO•
A(0:15)
A(0)
A(1)
A(2)
D(0:7)
WR•
RESET•
U14 HC86
U28 HC00
U29 HCT165
U20 HC4040
U10 HC27
U12 HC00
U15 HC02
U13 HC244
U26 HC273
U16 HC273
C41 .1 25V
C36 .1 25V
R37 15K
R35 4.7K
R36 15K
C29 .1 25V
AR1 LM358
TP18
AR2 LM324
AR3 LM324
Z1 350K 55K
Z2 22K
Z3 47K
CR14 BAW56
CR15 BAW56
CR16 BAW56
CR18 BAW56
CR19 BAW56
U17 ULN2004
U27 ULN2004
C43 180PF
C44 180PF
C45 180PF
C46 180PF
C47 180PF
C48 180PF
C49 180PF
C50 180PF
C51 180PF
C54 180PF
C55 180PF
C56 180PF
C57 180PF
C58 180PF
C52 180PF
C53 1000PF
R49 470
R58 470
R50 47 1/4W
R51 47 1/4W
R52 47 1/4W
R53 47 1/4W
R54 47 1/4W
R55 47 1/4W
R56 47 1/4W
R57 47 1/4W
R59 47 1/4W
R60 47 1/4W
R61 47 1/4W
R62 47 1/4W
L1 1T
L2 6T
J5
J6
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IOT
DCH
DCL
OUT0
OUT1
OUT2
OUT3
XT•
Y
RV1 39V
Q9 MMBT5089
CR17 MMBD7000
UNUSED
COMPONENT DIAGRAMS
Q9
E B C
TOP
CR17
CR14-16,18,19
2620A-1001
(4 of 4)

Figure 8-1. A1 Main PCA (2620A/2625A) (cont)


U28
U20
U14
U10
U2
C40
C36
C27
C23
TP20
R25
C3
R64
TP16
TP17
U29
U21
U15
U11
C41
C37
C28
C24
U25
U8
U3
J1
C42
TP12
CR16
CR17
AR3
AR2
Z1
R2
CR15
CR14
TP13
CR18
CR19
TP18
C29
C22
C19
W1
C11
Z3
Z2
AR1
U12
J4
U26
U16
U13
R19
C15
TP19
TP11
Y1
U4
U1
C1
R63
R1
TP3
TP5
TP6
TP4
C38
C33
C25
C16
R20
R21
Q8
Q7
VR3
R22
TP2
TP15
R8
R7
R3
J2
U27
U17
U7
TP8
U5
R50
R51
R52
R53
R54
R55
R56
R57
RV1
R35
R36
R37
R34
R28
CR8
CR9
CR11
CR12
CR5
CR6
CR7
J5
U22
TP9
TP14
TP10
R38
R42
R41
R40
T1
C12
C13
TP31
TP30
TP32
P10
C30
CR13
C31
U23
U6
R4
R5
R6
C6
C4
C5
L1
R45
R43
U18
C32
VR4
U24
R44
S1
TP1
C26
CR10
C14
TP7
R46
R47
R39
U19
C34
L2
R29
R30
R31
R32
R33
R23
R17
C7
CR1
CR2
CR3
J3
C2
R59
R60
R61
R62
C39
R48
J6
T2
R26
R27
C20
C21
C18
R18
U9
RT1
C59

2620A-1601

NOTE: TP2-TP20,TP31,TP32,W1 ARE NOT COMPONENTS.

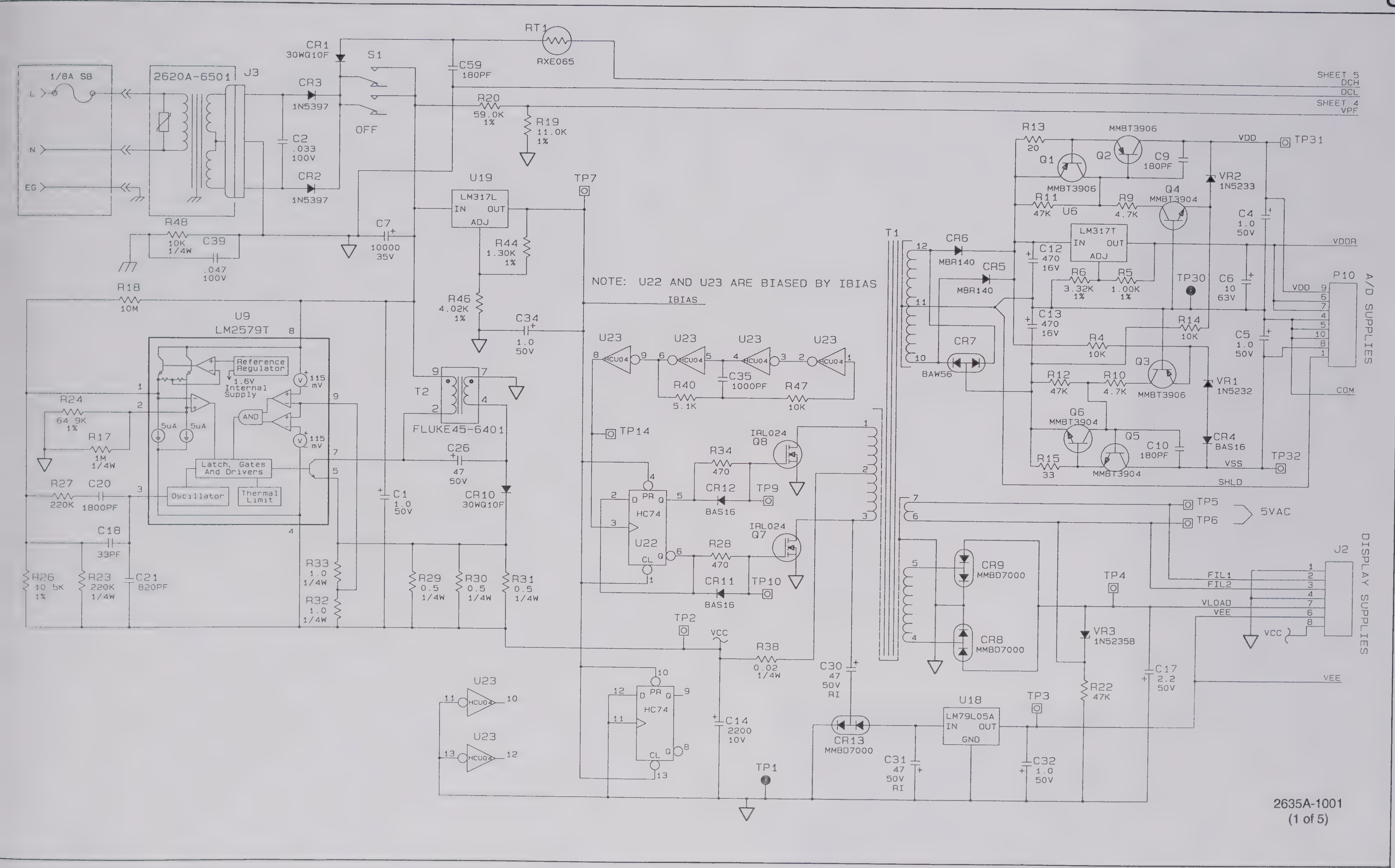
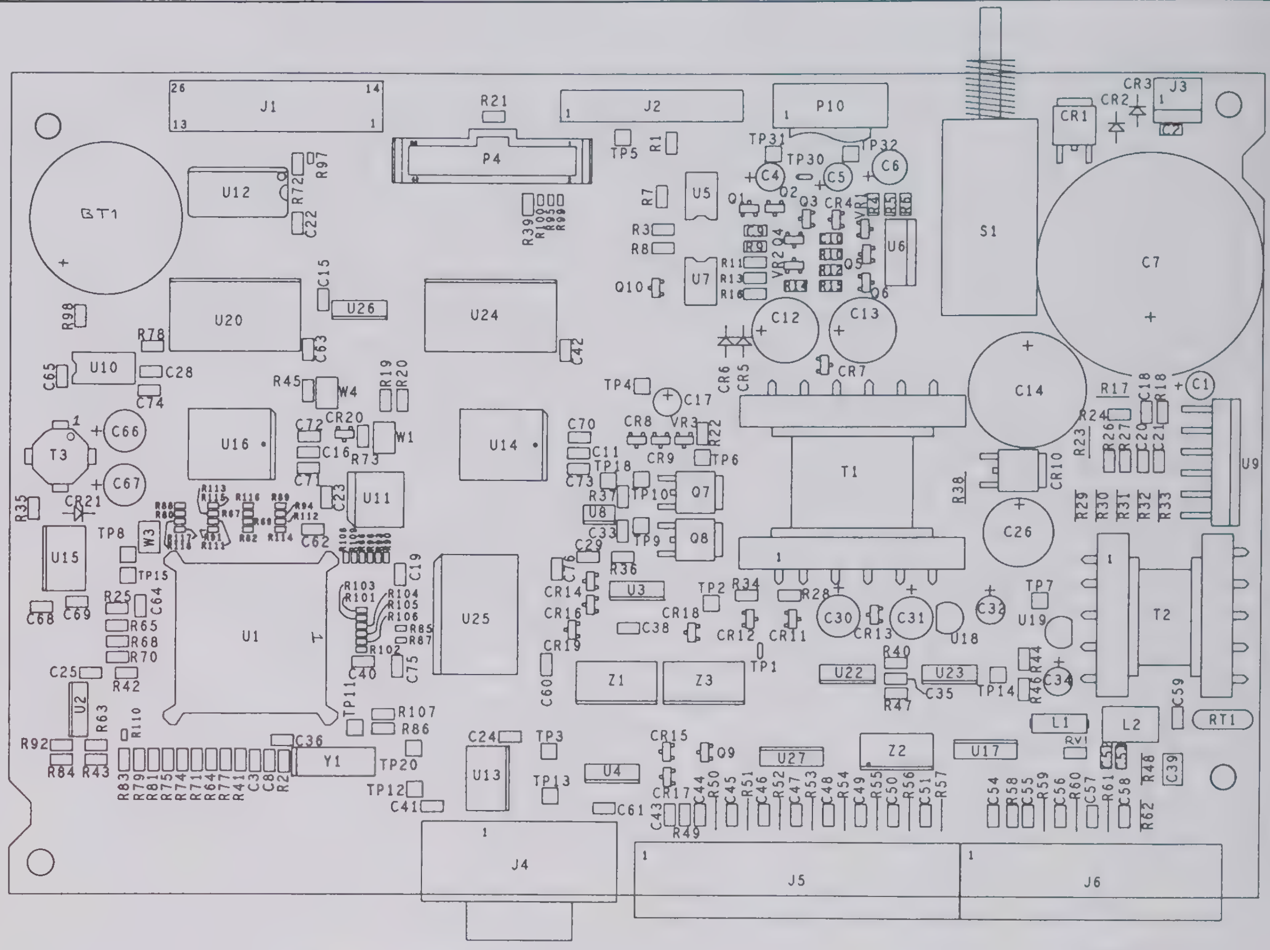

1/8A SB
L
N
EG
2620A-6501
J3
CR1 30WQ10F
CR3 1N5397
CR2 1N5397
C2 .033 100V
S1
OFF
RT1 RXE065
C59 180PF
R20 59.0K 1%
R19 11.0K 1%
SHEET 5 DCH
DCL
SHEET 4 VPF
R48 10K 1/4W
C39 .047 100V
C7 10000 35V
U19 LM317L IN OUT ADJ
R44 1.30K 1%
R46 4.02K 1%
TP7
C34 1.0 50V
R18 10M
U9 LM2579T
Reference Regulator
1.6V Internal Supply
115 mV
AND
5uA
Latch, Gates And Drivers
Oscillator
Thermal Limit
R24 64.9K 1%
R17 1M 1/4W
R27 220K
C20 1800PF
C18 33PF
R26 10.5K 1%
R23 220K 1/4W
C21 820PF
R33 1.0 1/4W
R32 1.0 1/4W
C1 1.0 50V
R29 0.5 1/4W
R30 0.5 1/4W
R31 0.5 1/4W
T2 FLUKE45-6401
C26 47 50V
CR10 30WQ10F
NOTE: U22 AND U23 ARE BIASED BY IBIAS
IBIAS
U23 HCU04
R40 5.1K
C35 1000PF
R47 10K
TP14
R34 470
Q8 IRL024
CR12 BAS16
TP9
U22 HC74 D PR Q CL
R28 470
Q7 IRL024
CR11 BAS16
TP10
TP2
VCC
R38 0.02 1/4W
C14 2200 10V
TP1
T1
CR6 MBR140
CR5 MBR140
CR7 BAW56
C30 47 50V RI
CR13 MMBD7000
C31 47 50V RI
U18 LM79L05A IN OUT GND
TP3
C32 1.0 50V
CR9 MMBD7000
CR8 MMBD7000
TP4
VR3 1N52358
R22 47K
C17 2.2 50V
TP5
TP6
5VAC
FIL1
FIL2
VLOAD
VEE
J2
DISPLAY SUPPLIES
R13 20
Q1 MMBT3906
Q2 MMBT3906
C9 180PF
VR2 1N5233
VDD
TP31
R11 47K
U6 LM317T IN OUT ADJ
R9 4.7K
Q4 MMBT3904
C4 1.0 50V
C12 470 16V
R6 3.32K 1%
R5 1.00K 1%
TP30
C6 10 63V
VDDR
P10
A/D SUPPLIES
C13 470 16V
R14 10K
R4 10K
C5 1.0 50V
R12 47K
R10 4.7K
Q3 MMBT3906
VR1 1N5232
COM
Q6 MMBT3904
Q5 MMBT3904
C10 180PF
CR4 BAS16
R15 33
VSS
SHLD
TP32
2635A-1001
(1 of 5)

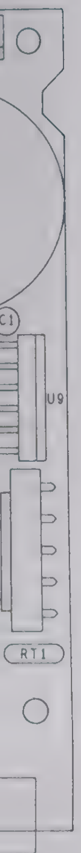
Figure 8-2. A1 Main PCA (2635A)


J1
J2
P10
P4
J3
CR1
CR2
CR3
BT1
U12
S1
C7
U20
U26
U24
U10
U5
U7
U6
Q10
C12
C13
C14
U16
U14
U11
T3
C66
C67
W3
U15
U1
U25
T1
C26
T2
U9
Q7
Q8
U3
U8
Z1
Z3
Z2
U22
U23
U27
U17
Y1
U13
U4
U2
L1
L2
RT1
J4
J5
J6
C30
C31
C32
C34
U18
U19
CR10
R38

2635A-1601

POWER SUPPLY PIN NUMBERS						
REF DES	GND	VCC (5.0V dc)	VBB (+5 dc)	VEE (-5V dc)	COM	VDDR (5.6V dc)
A1U1	4,13,23,	18,28,	-	-	-	-
-	29,34,	39,62,	-	-	-	-
-	44,50,	72,74,	-	-	-	-
-	57,67,	83,99,	-	-	-	-
-	73,84,	112,131	-	-	-	-
-	102,107,	-	-	-	-	-
-	116,126	-	-	-	-	-
A1U2	2,5,7,	14	-	-	-	-
-	9,12	-	-	-	-	-
A1U3	11	4	-	-	-	-
A1U4	11	4	-	-	-	-
A1U5	4	-	-	-	-	1
A1U7	-	-	-	-	4	-
A1U8	4	8	-	-	-	-
A1U9	-	4	-	-	-	-
A1U10	3	2	1	-	-	-
A1U11	10	20	-	-	-	-
A1U12	1,2,12,	-	24	-	-	-
-	21	-	-	-	-	-
A1U13	9	1,16	-	8	-	-
A1U14	16	32	-	-	-	-
A1U15	7,8,9	16	-	-	-	-
A1U16	16	32	-	-	-	-
A1U20	16	-	32	-	-	-
A1U22	7,11,12	-	-	-	-	-
A1U23	7,11,13	-	-	-	-	-
A1U24	16	-	32	-	-	-
A1U25	4,16,28,	3,6,27,	-	-	-	-
-	52,53,	29,41,	-	-	-	-
-	66,77,	54,55,	-	-	-	-
-	93	56,79,	-	-	-	-
-	-	91	-	-	-	-
A1U26	7	-	9,12,14	-	-	-
A1Z2	-	16	-	-	-	-

Reference Designations		
Last Used		Not Used
BT	BT1	
C	C76	C27, 37
CR	CR21	
J	J6	
L	L2	
P	P10	P1–3, 5–9
Q	Q10	
R	R118	R76
RT	RT1	
RV	RV1	
S	S1	
T	T3	
TP	TP32	TP16–17, 19, 21–29
U	U27	U21
VR	VR3	
W	W4	W2
Y	Y1	
Z	Z3	



601

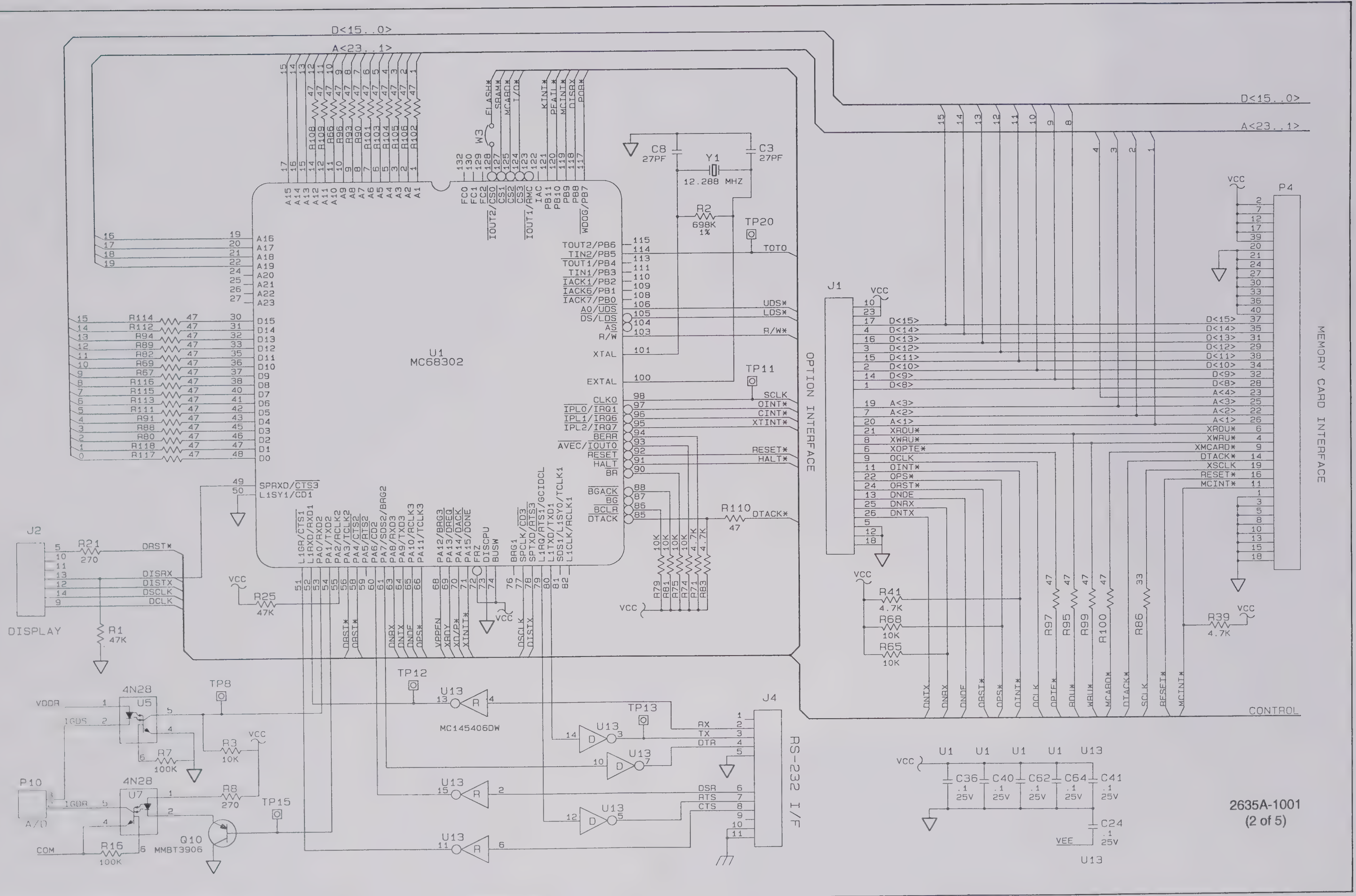
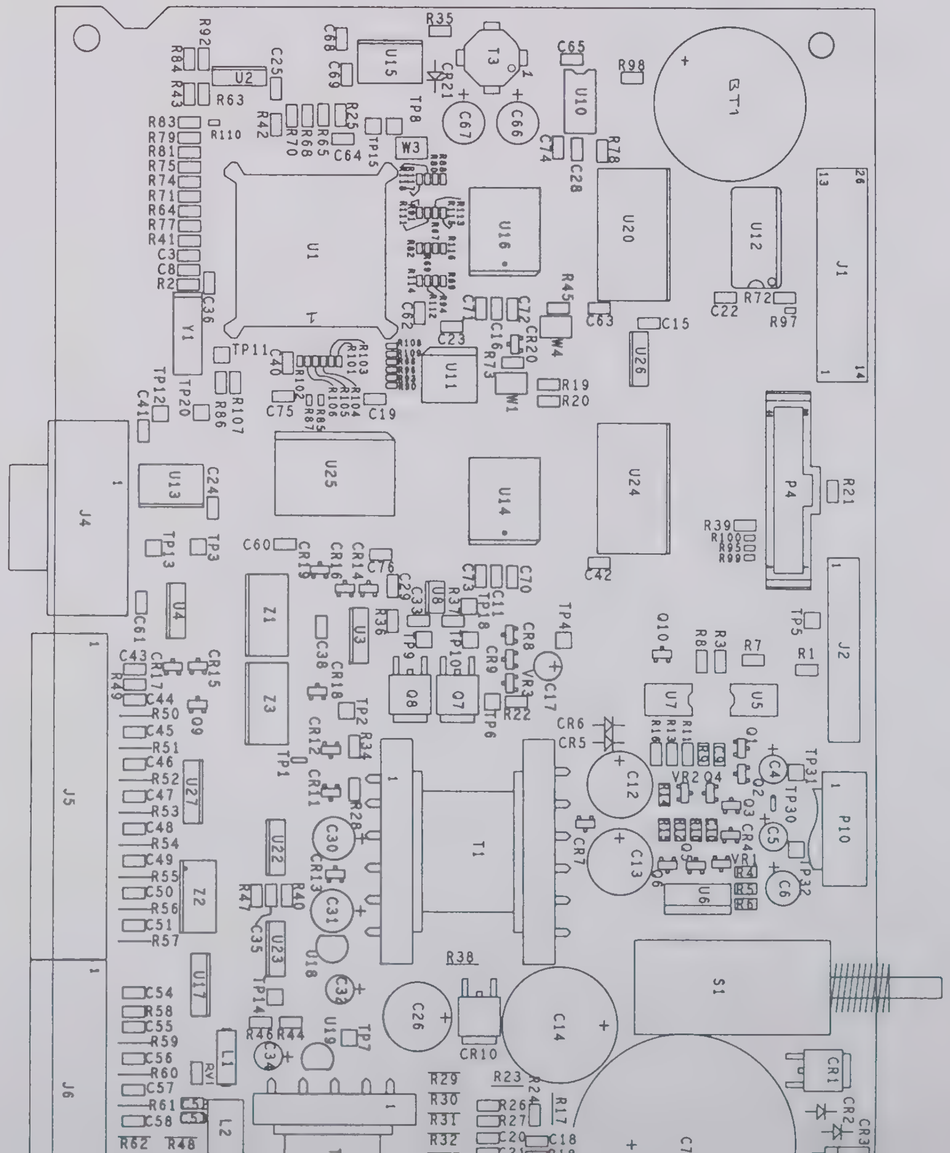

U1
MC68302
MEMORY CARD INTERFACE
OPTION INTERFACE
RS-232 I/F
DISPLAY
CONTROL
P4
J1
J2
J4
P10
A/D
D<15..0>
A<23..1>
Y1
12.288 MHZ
C8
27PF
C3
27PF
R2
698K
1%
TP20
TOTO
TP11
R110
47
DTACK*
UDS*
LDS*
R/W*
SCLK
OINT*
CINT*
XTINT*
RESET*
HALT*
W3
FLASH*
SRAM*
MCARD*
I/O*
KINT*
PFAIL*
MCINT*
DISRX
POR*
R21
270
DRST*
DISRX
DISTX
DSCLK
DCLK
R1
47K
R25
47K
VCC
R41
4.7K
R68
10K
R65
10K
R39
4.7K
R97
R95
R99
R100
R86
33
U13
MC145406DW
4N28
U5
U7
R3
10K
R7
100K
R8
270
R16
100K
Q10
MMBT3906
TP8
TP12
TP13
TP15
VDDR
IGDS
IGDR
COM
RX
TX
DTR
DSR
RTS
CTS
C36
C40
C62
C64
C41
C24
.1
25V
VEE
U1
U13
2635A-1001
(2 of 5)

Figure 8-2. A1 Main PCA (2635A) (cont)


BT1
J1
U12
U20
U16
U1
Y1
U15
T3
C66
C67
U10
U2
W3
U11
U26
J4
U13
U25
U14
U24
P4
J2
Z1
Z3
U4
U3
Q7
Q8
T1
J5
U27
U22
Z2
U23
U17
C30
C31
C12
C13
U5
U7
U6
P10
S1
C14
C26
CR10
J6
L1
L2
CR1

2635/

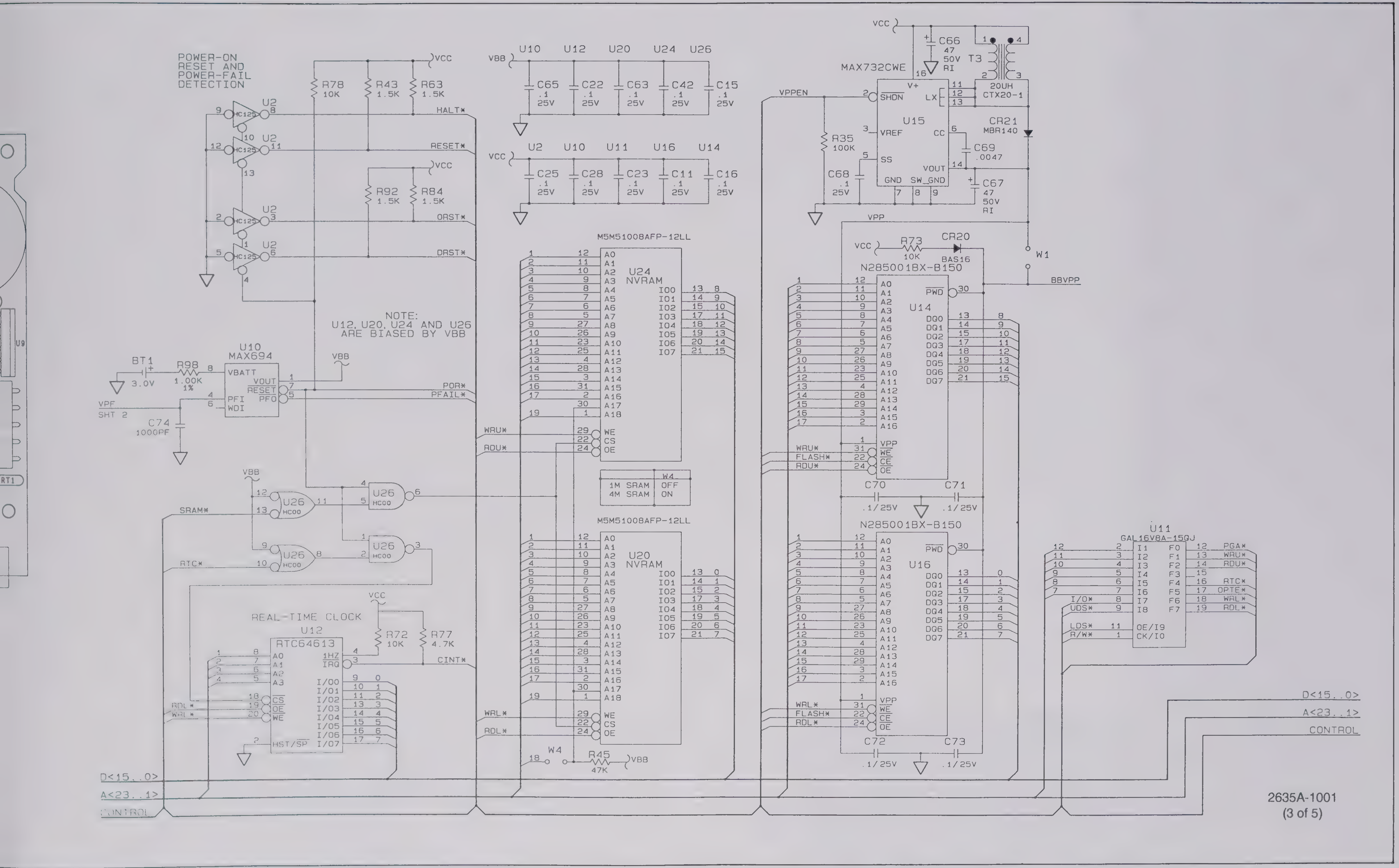
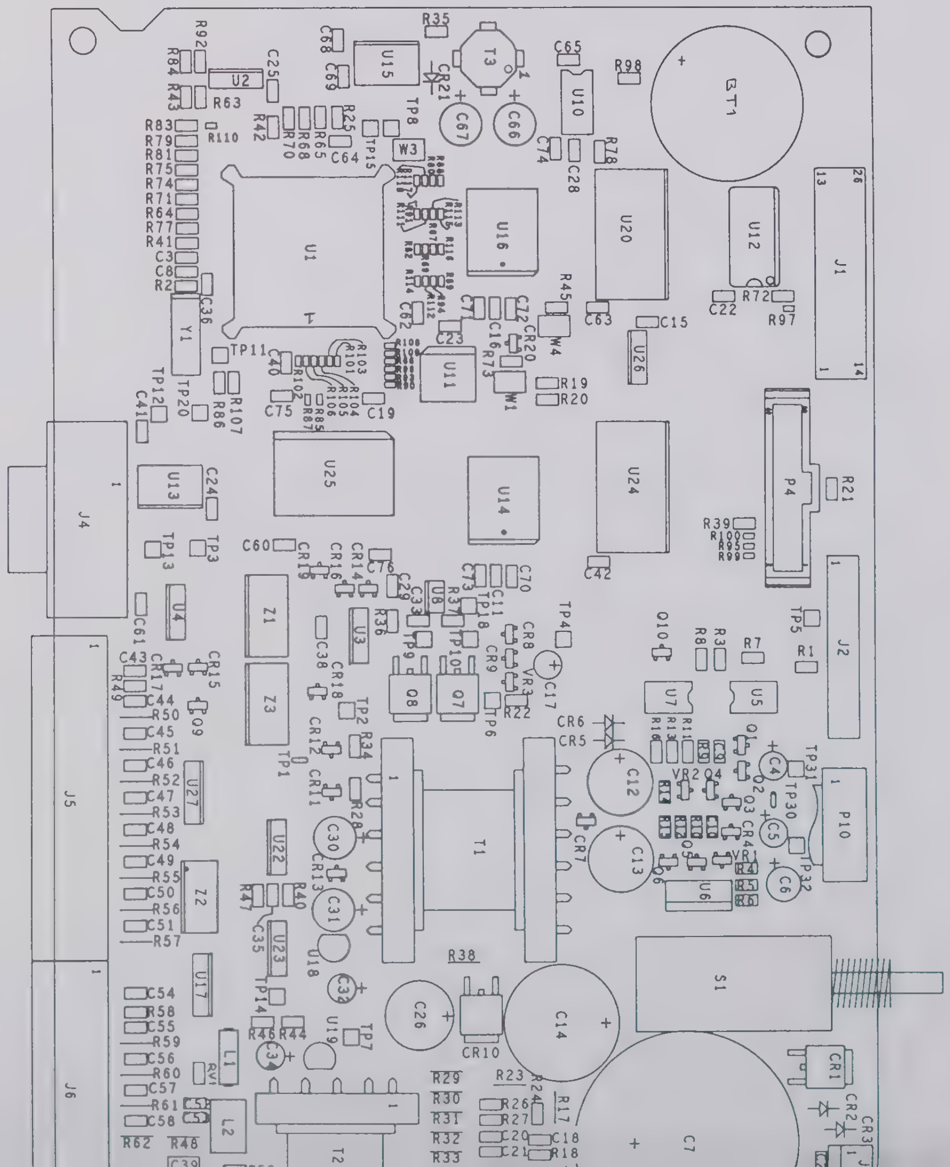

POWER-ON RESET AND POWER-FAIL DETECTION
U2 HC125
R78 10K
R43 1.5K
R63 1.5K
R92 1.5K
R84 1.5K
VCC
HALT*
RESET*
ORST*
DRST*
U10 MAX694
VBATT
VOUT
RESET
PFO
PFI
WDI
BT1 3.0V
R98 1.00K 1%
VPF SHT 2
C74 1000PF
POR*
PFAIL*
VBB
NOTE: U12, U20, U24 AND U26 ARE BIASED BY VBB
U26 HC00
SRAM*
RTC*
REAL-TIME CLOCK
U12 RTC64613
1HZ
IRQ
CS
OE
WE
HST/SP
R72 10K
R77 4.7K
CINT*
RDL*
WRL*
U10 U12 U20 U24 U26
C65 .1 25V
C22 .1 25V
C63 .1 25V
C42 .1 25V
C15 .1 25V
U2 U10 U11 U16 U14
C25 .1 25V
C28 .1 25V
C23 .1 25V
C11 .1 25V
C16 .1 25V
M5M51008AFP-12LL
U24 NVRAM
U20 NVRAM
WRU*
RDU*
W4
1M SRAM OFF
4M SRAM ON
R45 47K
MAX732CWE
U15
SHDN
VREF
SS
GND
SW_GND
VOUT
CC
LX
V+
VPPEN
R35 100K
C68 .1 25V
C66 47 50V RI
T3 20UH CTX20-1
CR21 MBR140
C69 .0047
C67 47 50V RI
VPP
W1
BBVPP
R73 10K
CR20 BAS16
N285001BX-B150
U14
U16
PWD
FLASH*
C70 .1/25V
C71 .1/25V
C72 .1/25V
C73 .1/25V
U11 GAL16V8A-15QJ
PGA*
WRU*
RDU*
RTC*
OPTE*
WRL*
RDL*
I/O*
UDS*
LDS*
R/W*
OE/I9
CK/I0
D<15..0>
A<23..1>
CONTROL
2635A-1001 (3 of 5)

Figure 8-2. A1 Main PCA (2635A) (cont)


BT1
J1
J2
J4
J5
J6
P4
P10
U1
U2
U4
U5
U6
U7
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U22
U23
U24
U25
U26
U27
T1
T2
T3
S1
Y1
Z1
Z2
Z3
W1
W3
W4
L1
L2
Q7
Q8
Q9
Q10
C7
C12
C13
C14
C26
C30
C31
C66
C67
CR1
CR2
CR5
CR6
CR10
R35
R38
R98
VR1
VR2
VR3
TP1
TP2
TP3
TP4
TP5

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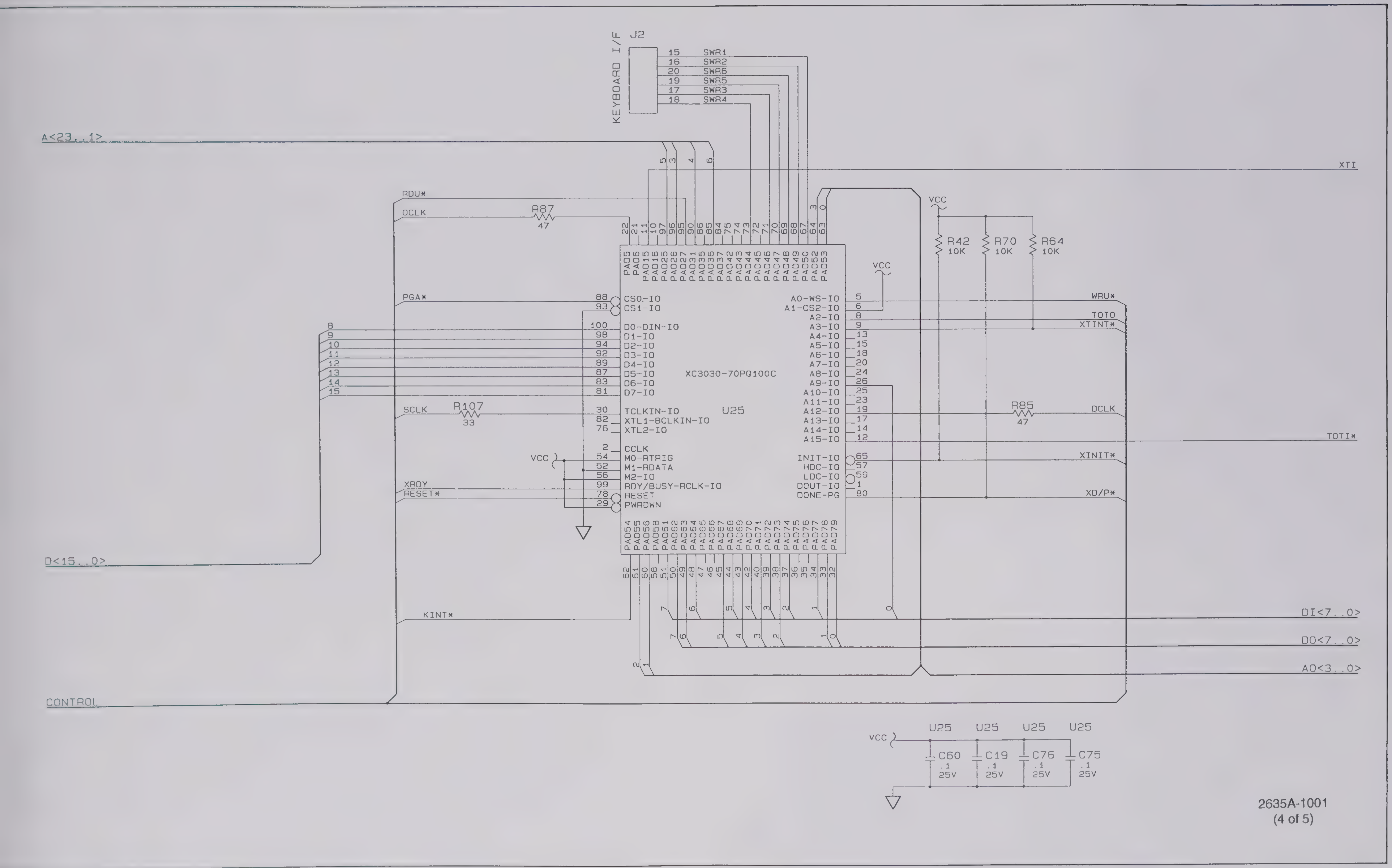
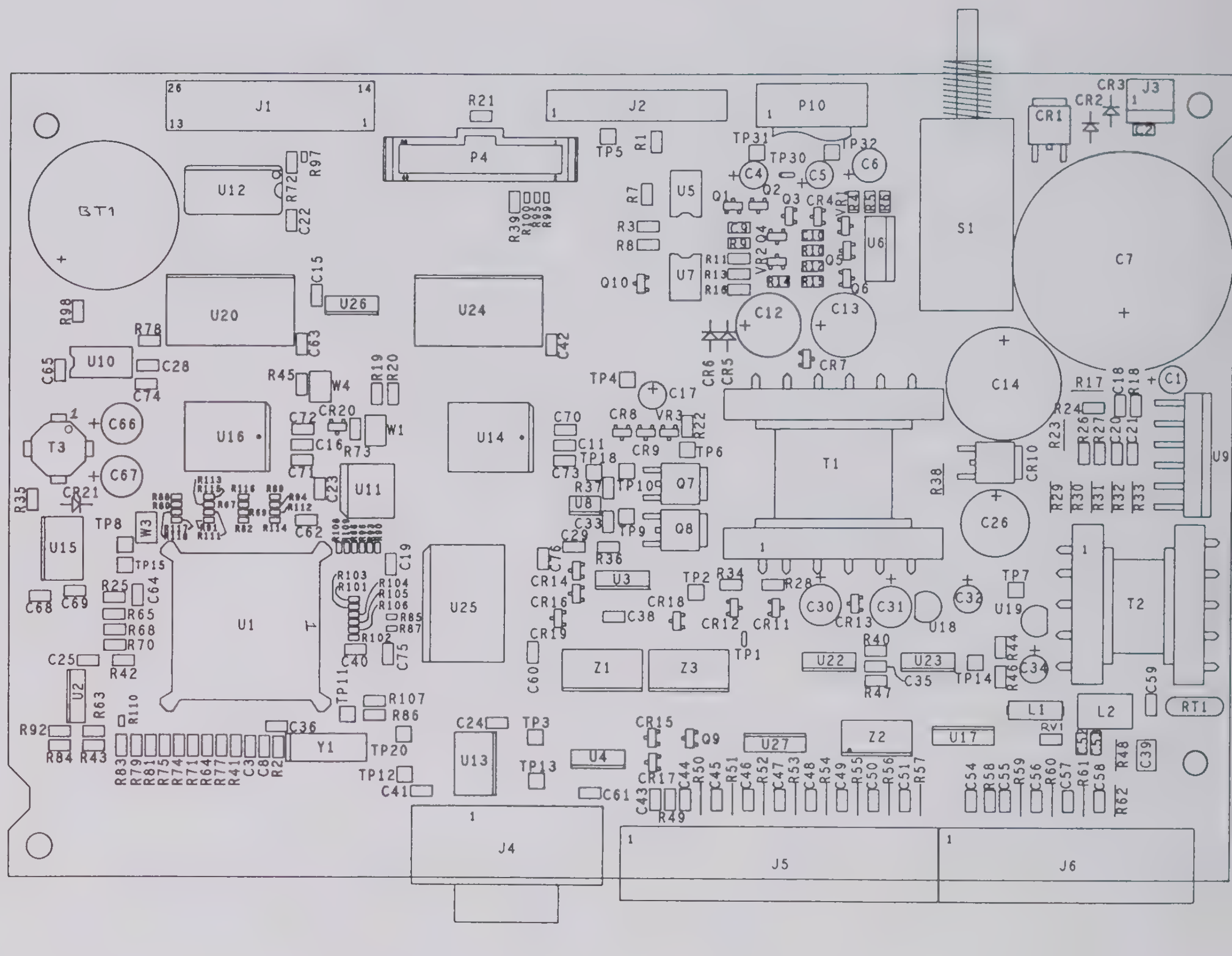

KEYBOARD I/F
J2
15 SWR1
16 SWR2
20 SWR6
19 SWR5
17 SWR3
18 SWR4
A<23..1>
XTI
RDU*
OCLK
R87
47
PGA*
SCLK
R107
33
XRDY
RESET*
KINT*
D<15..0>
CONTROL
VCC
XC3030-70PQ100C
U25
CS0-IO
CS1-IO
D0-DIN-IO
D1-IO
D2-IO
D3-IO
D4-IO
D5-IO
D6-IO
D7-IO
TCLKIN-IO
XTL1-BCLKIN-IO
XTL2-IO
CCLK
M0-RTRIG
M1-RDATA
M2-IO
RDY/BUSY-RCLK-IO
RESET
PWRDWN
A0-WS-IO
A1-CS2-IO
A2-IO
A3-IO
A4-IO
A5-IO
A6-IO
A7-IO
A8-IO
A9-IO
A10-IO
A11-IO
A12-IO
A13-IO
A14-IO
A15-IO
INIT-IO
HDC-IO
LDC-IO
DOUT-IO
DONE-PG
PAD5 PAD6 PAD15 PAD16 PAD25 PAD26 PAD27 PAD31 PAD35 PAD36 PAD37 PAD42 PAD43 PAD44 PAD45 PAD46 PAD47 PAD48 PAD49 PAD50 PAD52 PAD53
PAD54 PAD55 PAD56 PAD58 PAD61 PAD62 PAD63 PAD64 PAD65 PAD66 PAD67 PAD68 PAD69 PAD70 PAD71 PAD72 PAD73 PAD74 PAD75 PAD76 PAD77 PAD78 PAD79
R42 10K
R70 10K
R64 10K
R85
47
WRU*
TOTO
XTINT*
DCLK
TOTI*
XINIT*
XD/P*
DI<7..0>
DO<7..0>
AO<3..0>
U25
C60 .1 25V
C19 .1 25V
C76 .1 25V
C75 .1 25V
2635A-1001
(4 of 5)

Figure 8-2. A1 Main PCA (2635A) (cont)


J1
J2
P10
J3
P4
BT1
U12
U20
U24
U26
U10
U16
U14
U11
U15
T3
C66
C67
W3
W4
W1
U1
U25
Y1
U13
J4
J5
J6
T1
T2
Q7
Q8
U3
U5
U6
U7
U8
S1
C7
C12
C13
C14
C26
C30
C31
Z1
Z2
Z3
U22
U23
U27
U17
U4
U2
U9
L1
L2
RT1
CR1
CR2
CR3

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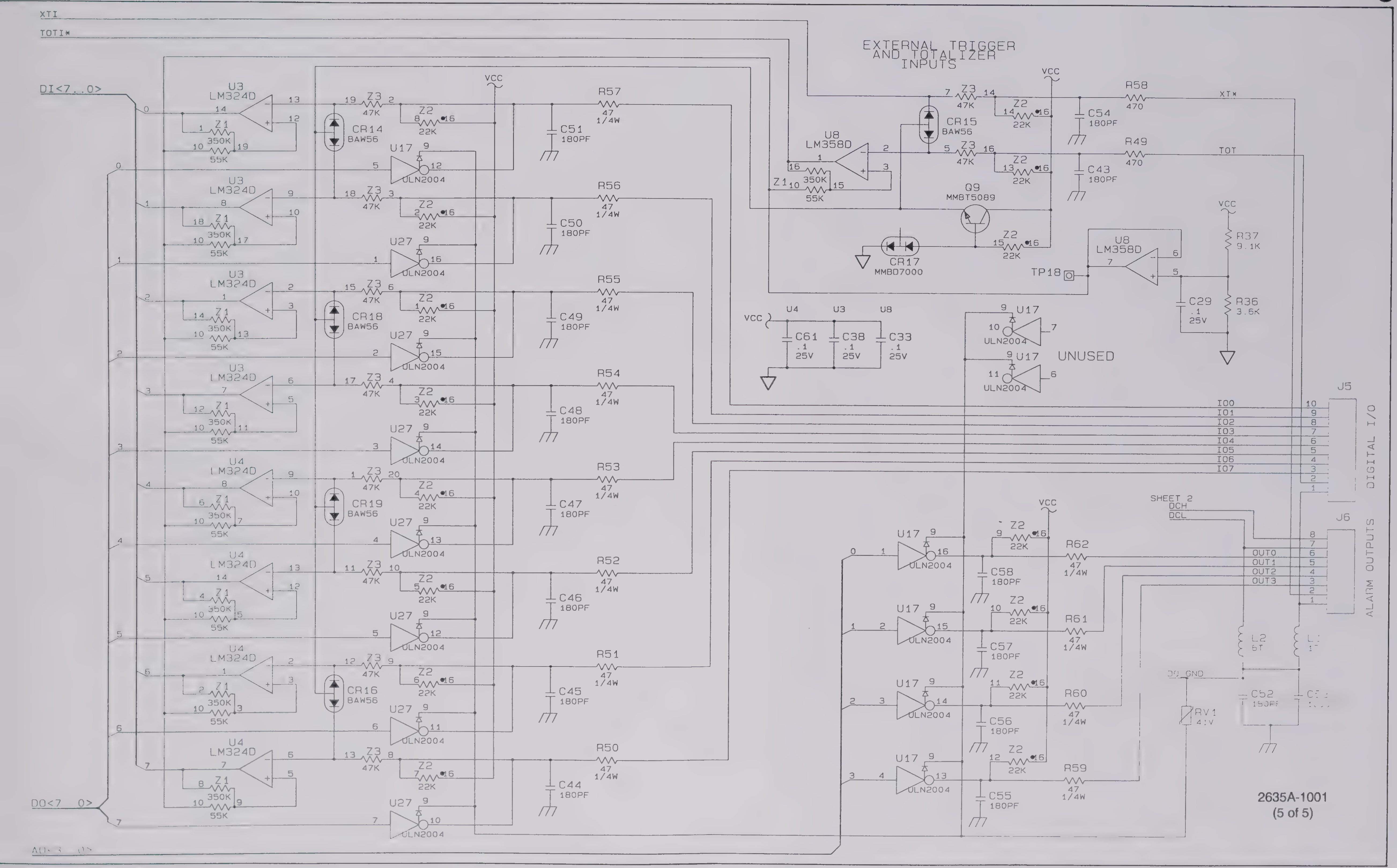
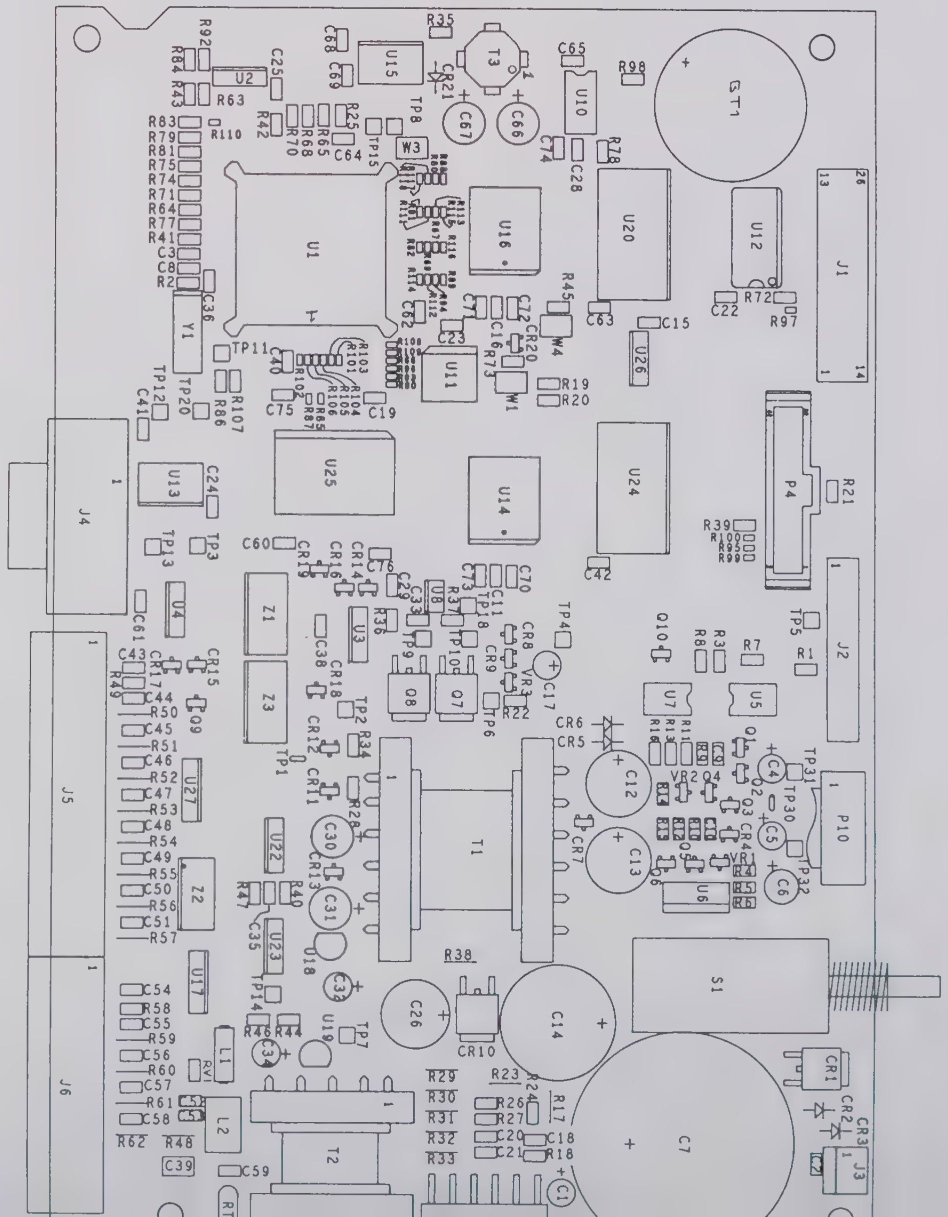

XTI
TOTI*
DI<7..0>
DO<7..0>
EXTERNAL TRIGGER AND TOTALIZER INPUTS
VCC
U3 LM324D
U4 LM324D
Z1 350K 55K
Z3 47K
Z2 22K
CR14 BAW56
CR18 BAW56
CR19 BAW56
CR16 BAW56
U17 ULN2004
U27 ULN2004
R57 47 1/4W
R56 47 1/4W
R55 47 1/4W
R54 47 1/4W
R53 47 1/4W
R52 47 1/4W
R51 47 1/4W
R50 47 1/4W
C51 180PF
C50 180PF
C49 180PF
C48 180PF
C47 180PF
C46 180PF
C45 180PF
C44 180PF
U8 LM358D
CR15 BAW56
Q9 MMBT5089
CR17 MMBD7000
R58 470
R49 470
C54 180PF
C43 180PF
XT*
TOT
R37 9.1K
R36 3.6K
C29 .1 25V
TP18
U4 U3 U8
C61 .1 25V
C38 .1 25V
C33 .1 25V
UNUSED
J5
DIGITAL I/O
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
SHEET 2
DCH
DCL
J6
ALARM OUTPUTS
OUT0
OUT1
OUT2
OUT3
R62 47 1/4W
R61 47 1/4W
R60 47 1/4W
R59 47 1/4W
C58 180PF
C57 180PF
C56 180PF
C55 180PF
L2 6T
L1 1T
DO_GND
C52 150PF
RV1 41V
2635A-1001
(5 of 5)

Figure 8-2. A1 Main PCA (2635A) (cont)


U1
U2
U3
U4
U5
U6
U7
U8
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U22
U23
U24
U25
U26
U27
J1
J2
J3
J4
J5
J6
P4
P10
T1
T2
T3
BT1
S1
Y1
Z1
Z2
Z3
Q7
Q8
Q9
Q10
L1
L2
C7
C12
C13
C14
C26
C30
C31
C66
C67
W1
W3
W4
CR1
CR2
CR3
CR5
CR6
CR7
CR10
VR1
VR2
VR3
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP18
TP20
TP30
TP31
TP32
R1
R2
R3
R7
R17
R21
R35
R38
R39
R45
R72
R97
R98

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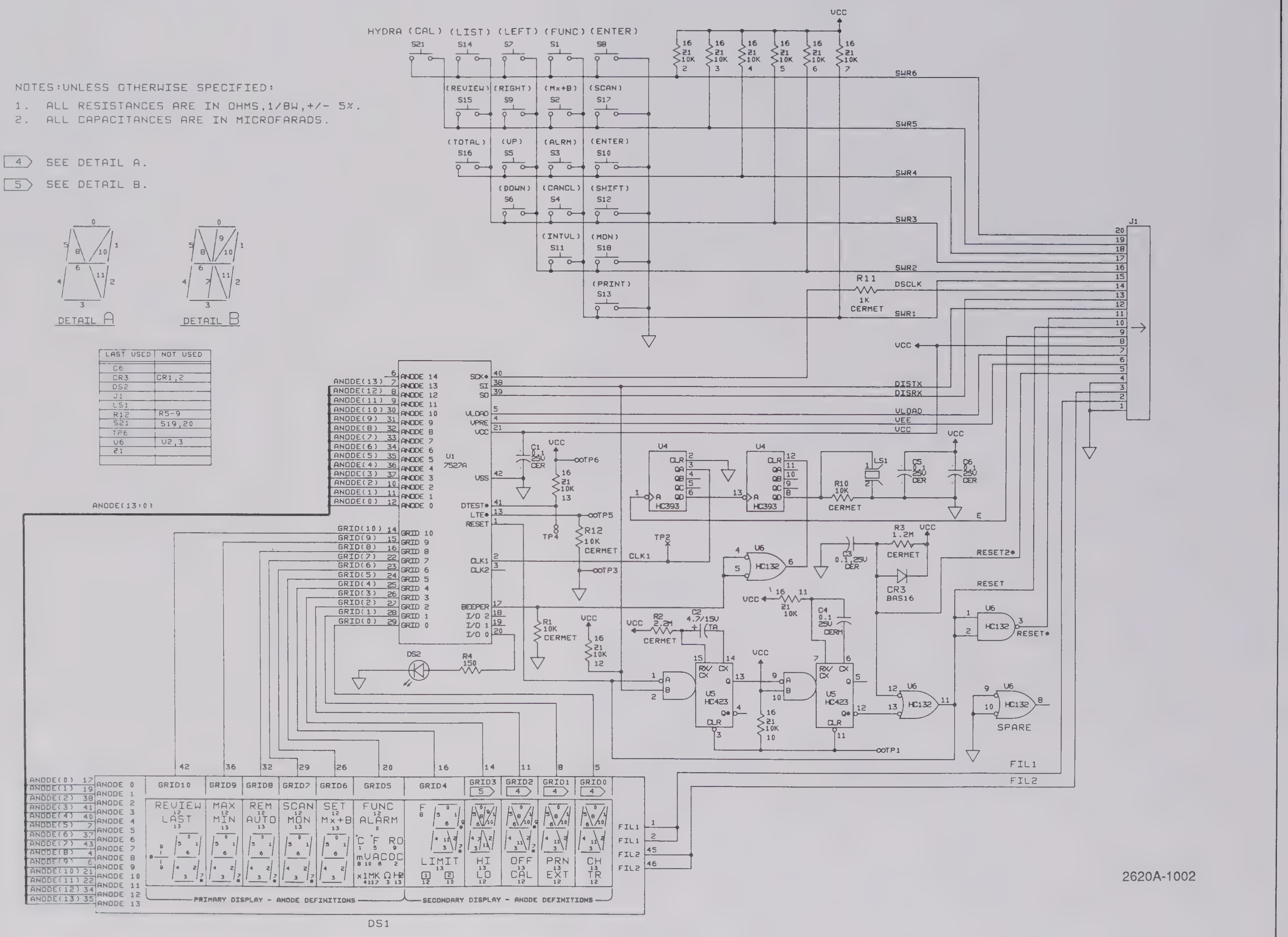

HYDRA (CAL) (LIST) (LEFT) (FUNC) (ENTER)
S21 S14 S7 S1 S8
(REVIEW) (RIGHT) (Mx+B) (SCAN)
S15 S9 S2 S17
(TOTAL) (UP) (ALRM) (ENTER)
S16 S5 S3 S10
(DOWN) (CANCL) (SHIFT)
S6 S4 S12
(INTVL) (MON)
S11 S18
(PRINT)
S13
SWR6
SWR5
SWR4
SWR3
SWR2
DSCLK
SWR1
R11 1K CERMET
J1
VCC
DISTX
DISRX
VLOAD
VEE
U1 7527A
U4 HC393
U5 HC423
U6 HC132
SPARE
RESET2
RESET
FIL1
FIL2
LS1
R10 10K CERMET
R3 1.2M CERMET
CR3 BAS16
R2 2.2M CERMET
R1 10K CERMET
R12 10K CERMET
R4 150
DS2
TP1
TP2
TP3
TP4
TP5
TP6
CLK1
ANODE(13:0)
GRID10 GRID9 GRID8 GRID7 GRID6 GRID5 GRID4 GRID3 GRID2 GRID1 GRID0
REVIEW LAST
MAX MIN
REM AUTO
SCAN MON
SET Mx+B
FUNC ALARM
°C °F RO
mVACDC
x1MK Ω HZ
LIMIT
HI LO
OFF CAL
PRN EXT
CH TR
PRIMARY DISPLAY - ANODE DEFINITIONS
SECONDARY DISPLAY - ANODE DEFINITIONS
DS1
DETAIL A
DETAIL B
2620A-1002

NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCES ARE IN OHMS,1/8W,+/- 5%.
2. ALL CAPACITANCES ARE IN MICROFARADS.

4 SEE DETAIL A.
5 SEE DETAIL B.

LAST USED	NOT USED
C6	
CR3	CR1,2
DS2	
J1	
LS1	
R12	R5-9
S21	S19,20
TP6	
U6	U2,3
Z1	

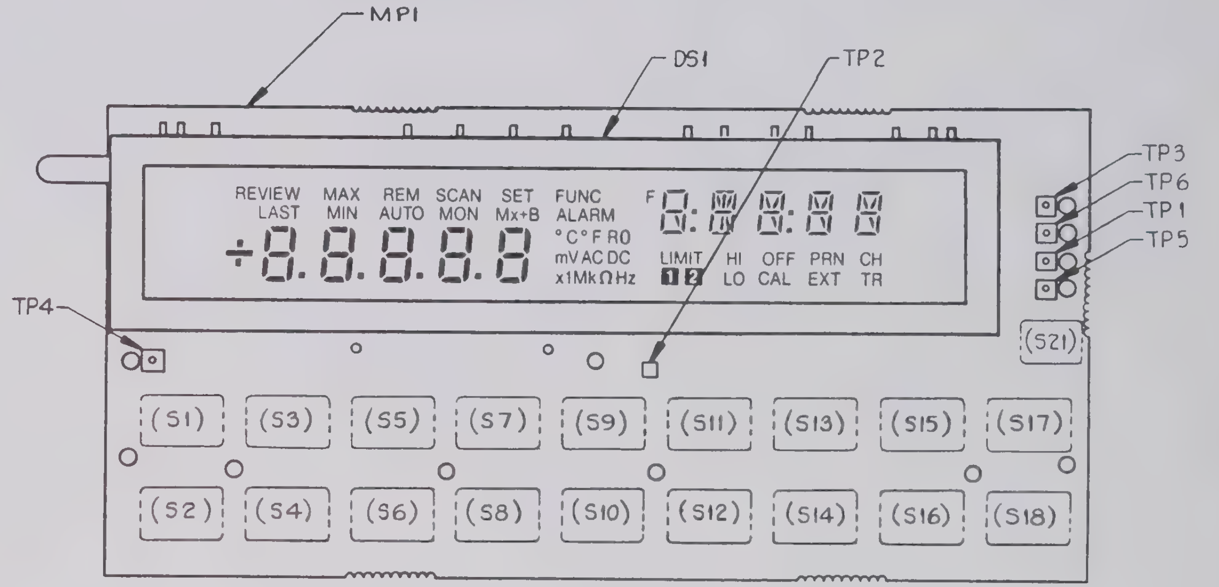
NOTES:

1. TP1 – TP6, S1 – S18, S21 ARE NOT COMPONENTS.
2. JUMPER INSTALLED BETWEEN TP1 AND TP3 ON 2635A ONLY.

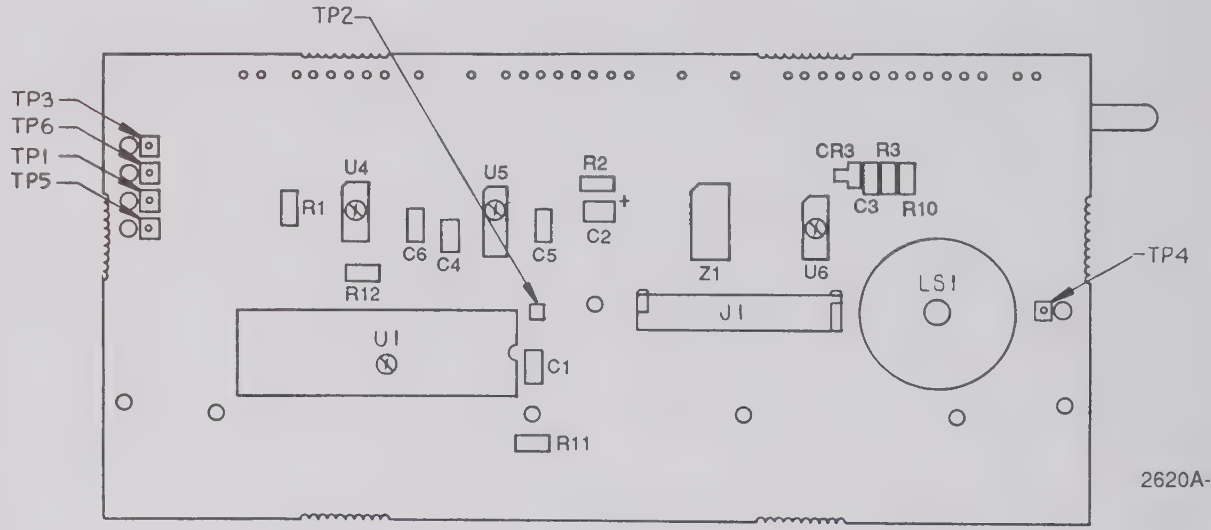
CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY

Figure 8-3. A2 Display PCA

REF DES	POWER SUPPLY PIN NUMBERS			
	VCC (5.1V dc)	GND	VEE (5.0V dc)	VLOAD (-28.5 to -30.0V dc)
A2U1	21	42	4	5
A2U4	16	2,8	_	_
A2U5	10,16	8	_	_
A2U6	14	7,9,10	_	_
A2Z1	16	_	_	_


MPI
DS1
TP2
TP3
TP6
TP1
TP5
TP4
REVIEW LAST
MAX MIN
REM AUTO
SCAN MON
SET Mx+B
FUNC ALARM
°C°F RO
mV AC DC
x1MkΩHz
LIMIT 1 2
HI LO
OFF CAL
PRN EXT
CH TR
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S21

CKT 1


TP2
TP3
TP6
TP1
TP5
TP4
R1
U4
U5
R2
C2
C6
C4
C5
R12
U1
C1
R11
Z1
J1
U6
CR3
R3
C3
R10
LS1

2620A-4002

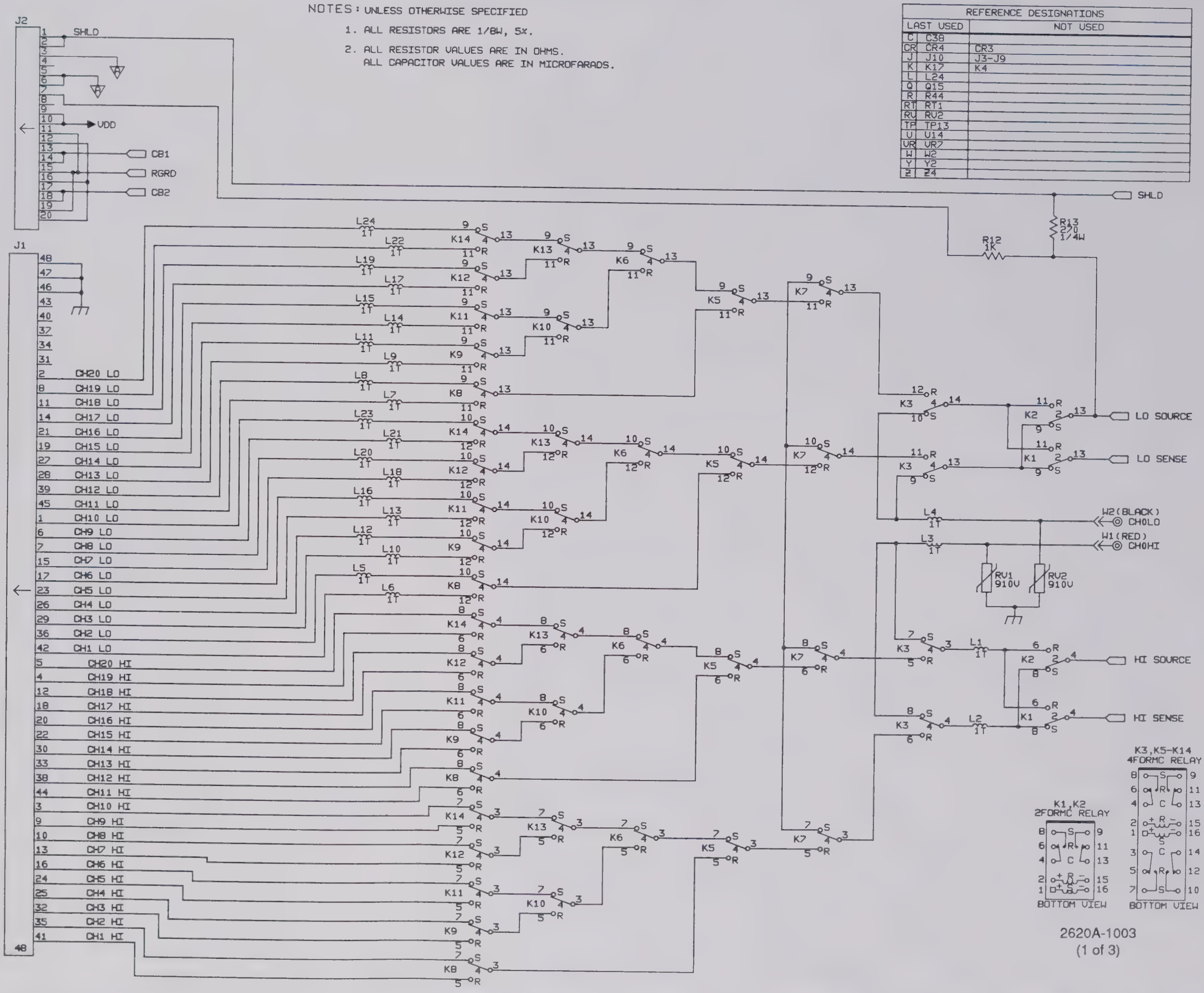
CKT 2

POWER SUPPLY PIN NUMBERS				
VDD 5.3V dc)	VSS (-5.4V dc)	ANALOG_GND	VDDR (5.6V dc)	RCOM
3	–	10,11,12	–	–
1,16	8	6,9	–	–
1,10,11,	–	2,7	–	–
12,13,14	–	–	–	–
–	–	–	9	8
–	–	–	9	8
–	–	1,3,4	–	–
–	–	3	–	–
1	44	4,25,27,38	–	–
5,6,9,36	–	2,45	–	–
–	–	–	9	8
–	–	–	9	8
–	–	–	9	8
8	–	4	–	–
8	4	–	–	–
–	–	4	–	–
1	–	–	–	–
–	–	8	–	–

NOTES:

1. TP1 – TP8, TP10 – TP13 ARE NOT COMPONENTS.

CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY

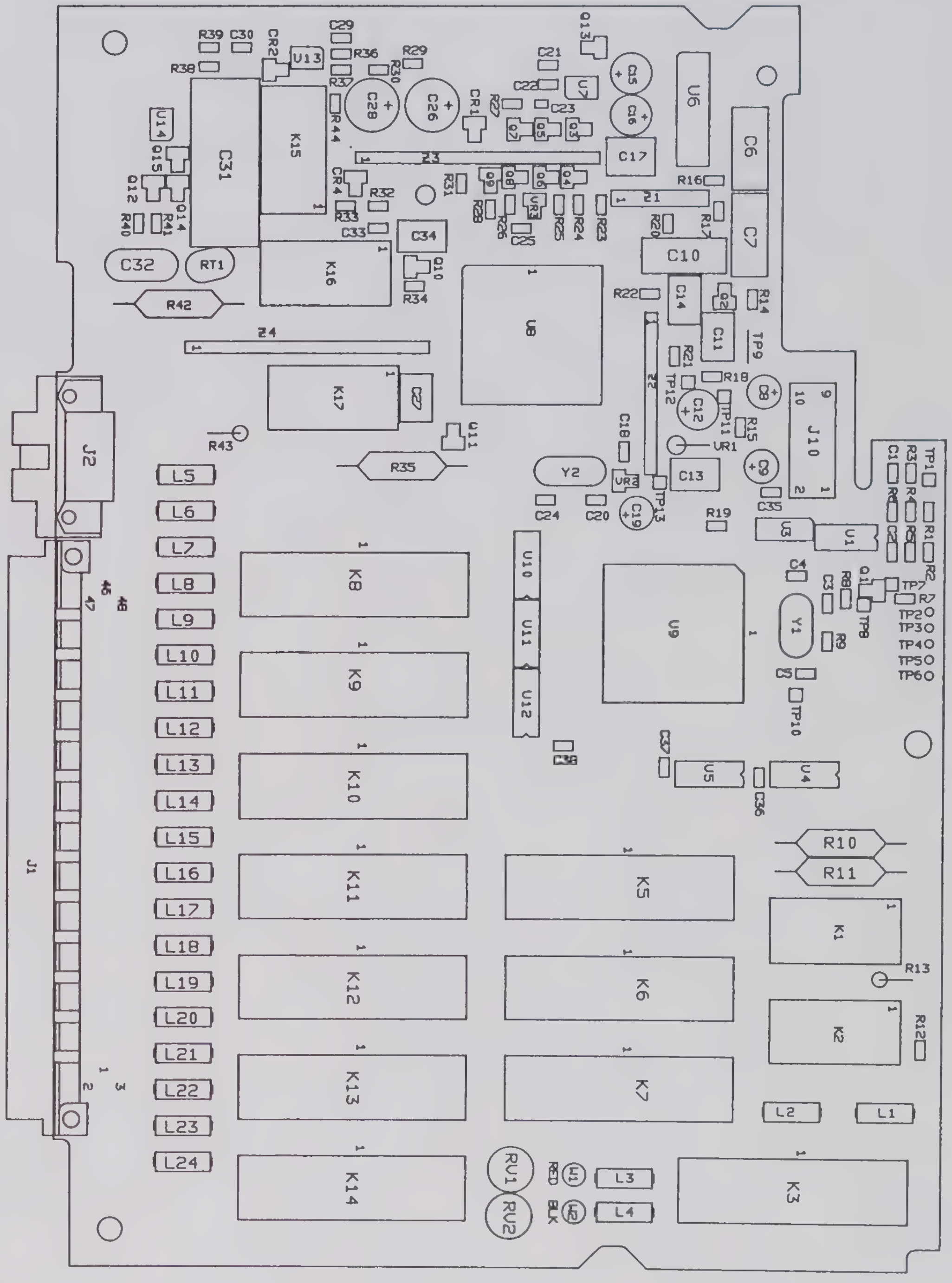

J2
SHLD
VDD
CB1
RGRD
CB2
J1
CH20 LO
CH19 LO
CH18 LO
CH17 LO
CH16 LO
CH15 LO
CH14 LO
CH13 LO
CH12 LO
CH11 LO
CH10 LO
CH9 LO
CH8 LO
CH7 LO
CH6 LO
CH5 LO
CH4 LO
CH3 LO
CH2 LO
CH1 LO
CH20 HI
CH19 HI
CH18 HI
CH17 HI
CH16 HI
CH15 HI
CH14 HI
CH13 HI
CH12 HI
CH11 HI
CH10 HI
CH9 HI
CH8 HI
CH7 HI
CH6 HI
CH5 HI
CH4 HI
CH3 HI
CH2 HI
CH1 HI
K14
K13
K12
K11
K10
K9
K8
K7
K6
K5
K3
K2
K1
R12 1K
R13 270 1/4W
SHLD
LO SOURCE
LO SENSE
W2(BLACK) CH0LO
W1(RED) CH0HI
RV1 910V
RV2 910V
HI SOURCE
HI SENSE
K1,K2 2FORMC RELAY
K3,K5-K14 4FORMC RELAY
BOTTOM VIEW
BOTTOM VIEW
2620A-1003
(1 of 3)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/8W, 5%.
2. ALL RESISTOR VALUES ARE IN OHMS.
   ALL CAPACITOR VALUES ARE IN MICROFARADS.

REFERENCE DESIGNATIONS		
LAST USED		NOT USED
C	C38	
CR	CR4	CR3
J	J10	J3-J9
K	K17	K4
L	L24	
Q	Q15	
R	R44	
RT	RT1	
RV	RV2	
TP	TP13	
U	U14	
VR	VR7	
W	W2	
Y	Y2	
Z	Z4	

Figure 8-4. A3 A/D Converter PCA


J1
J2
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
L16
L17
L18
L19
L20
L21
L22
L23
L24
K1
K2
K3
K5
K6
K7
K8
K9
K10
K11
K12
K13
K14
K15
K16
K17
L1
L2
L3
L4
RU1
RU2
RED
BLK
R10
R11
R12
R13
R35
R42
R43
C31
C32
RT1
U1
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
Y1
Y2
J10
C6
C7
C10
C11
C13
C14
C17
C34
Z1
Z2
Z3
Z4
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
VR1
1
2
3
46
47
48

2620A-1603

REF DES
A3U1
A3U2
A3U3
–
A3U4
A3U5
A3U6
A3U7
A3U8
A3U9
A3U10
A3U11
A3U12
A3U13
A3U14
A3Z1
A3Z2
A3Z3

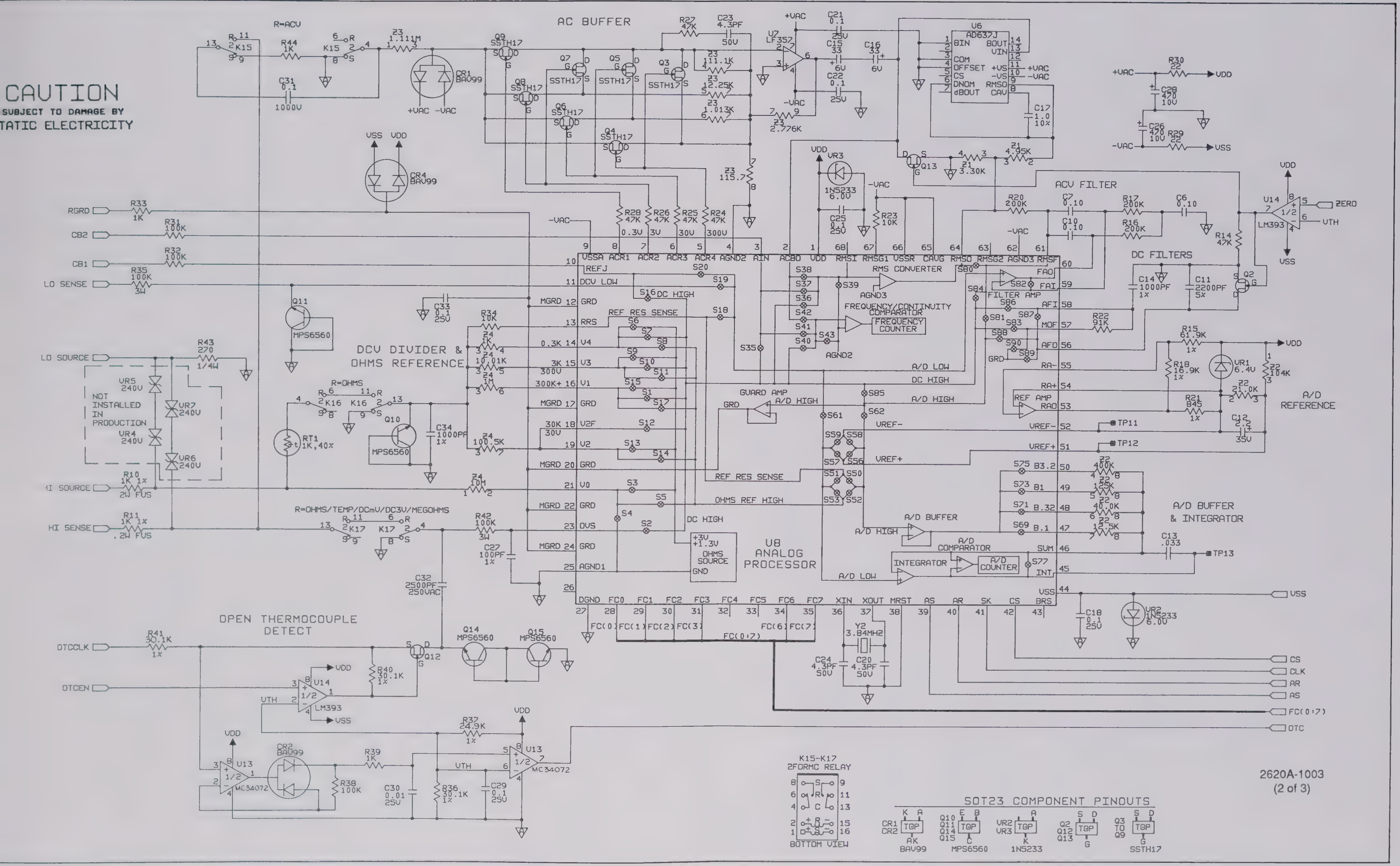
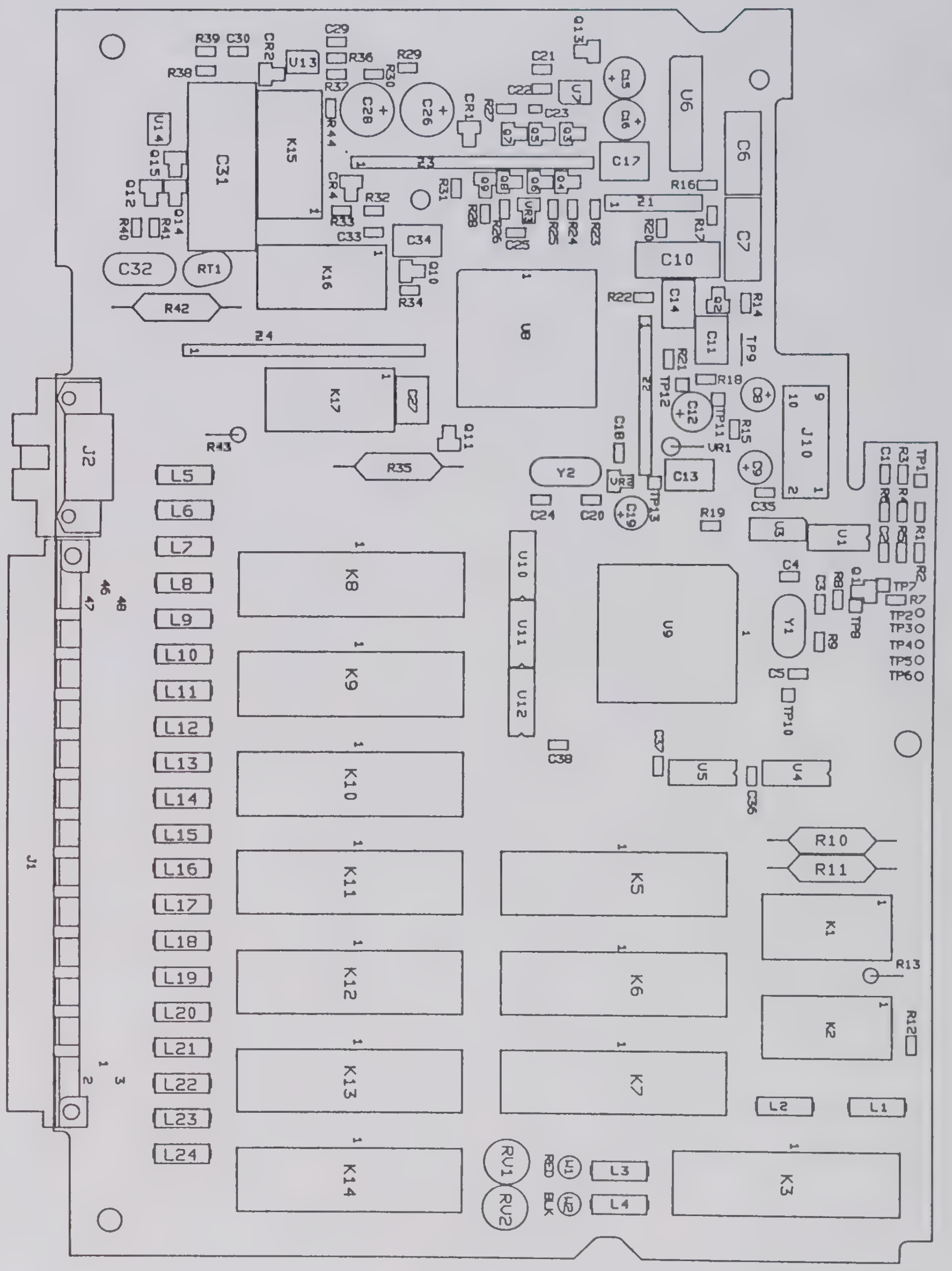

CAUTION
SUBJECT TO DAMAGE BY
TATIC ELECTRICITY
AC BUFFER
R=ACV
K15
R44 1K
C31 0.1 1000V
Z3 1.111M
CR1 BAV99
+VAC -VAC
Q9 SSTH17
Q8 SSTH17
Q7 SSTH17
Q6 SSTH17
Q5 SSTH17
Q4 SSTH17
Q3 SSTH17
R27 47K
C23 4.3PF 50V
Z3 111.1K
Z3 12.25K
Z3 1.013K
Z3 115.7
Z3 2.776K
U7 LF357
C21 0.1 25V
C15 33 6V
C16 33 6V
C22 0.1 25V
U6 AD637J
BIN
BOUT
VIN
COM
OFFSET
+VS
-VS
CS
DNOM
RMSO
dBOUT
CAV
C17 1.0 10%
R30 22
C28 470 10V
C26 470 10V
R29 22
+VAC
-VAC
VDD
VSS
CR4 BAV99
Q13
Z1 3.30K
Z1 4.95K
VR3 1N5233 6.0V
C25 0.1 25V
R23 10K
ACV FILTER
R20 200K
C7 0.10
C10 0.10
R17 200K
R16 200K
C6 0.10
R14 47K
U14 1/2 LM393
ZERO
VTH
DC FILTERS
C14 1000PF 1%
C11 2200PF 5%
Q2
RGRD
CB2
CB1
LO SENSE
LO SOURCE
HI SOURCE
HI SENSE
R33 1K
R31 100K
R32 100K
R35 100K 3W
R43 270 1/4W
VR5 240V
VR7 240V
VR4 240V
VR6 240V
NOT INSTALLED IN PRODUCTION
R10 1K 1% 2W FUS
R11 1K 1% .2W FUS
Q11 MPS6560
C33 0.1 25V
DCV DIVIDER & OHMS REFERENCE
R34 10K
Z4 1K
Z4 10.01K
Z4 1M
Z4 100.5K
Z4 10M
R=OHMS
K16
RT1 1K,40%
Q10 MPS6560
C34 1000PF 1%
R=OHMS/TEMP/DCmV/DC3V/MEGOHMS
K17
R42 100K 3W
C27 100PF 1%
C32 2500PF 250VAC
R28 47K 0.3V
R26 47K 3V
R25 47K 30V
R24 47K 300V
VSSA ACR1 ACR2 ACR3 ACR4 AGND2 AIN ACBO VDD RMSI RMSG1 VSSR CAVG RMSO RMSG2 AGND3 RMSF
REFJ
DCV LOW
MGRD GRD
RRS
0.3K V4
3K V3 300V
300K+ V1
MGRD GRD
30K V2F 30V
V2
MGRD GRD
V0
MGRD GRD
OVS
MGRD GRD
AGND1
DGND FC0 FC1 FC2 FC3 FC4 FC5 FC6 FC7 XIN XOUT MRST AS AR SK CS BRS
FC(0) FC(1) FC(2) FC(3) FC(6) FC(7) FC(0:7)
RMS CONVERTER
FILTER AMP
FAO FAI AFI MOF AFO
FREQUENCY/CONTINUITY COMPARATOR
FREQUENCY COUNTER
AGND3
AGND2
DC HIGH
REF RES SENSE
GUARD AMP
GRD
A/D HIGH
A/D LOW
VREF-
VREF+
RA- RA+ RAO
REF AMP
OHMS REF HIGH
+3V +1.3V OHMS SOURCE GND
U8 ANALOG PROCESSOR
A/D BUFFER
A/D COMPARATOR
INTEGRATOR
A/D COUNTER
SUM INT VSS
B3.2 B1 B.32 B.1
A/D BUFFER & INTEGRATOR
Z2 400K
Z2 125K
Z2 40.0K
Z2 12.5K
C13 .033
TP11 TP12 TP13
R15 61.9K 1%
R18 16.9K 1%
R21 845 1%
VR1 6.4V
Z2 104K
Z2 21.0K
C12 2.2 35V
A/D REFERENCE
C18 0.1 25V
VR2 1N5233 6.0V
Y2 3.84MHZ
C24 4.3PF 50V
C20 4.3PF 50V
CS CLK AR AS FC(0:7) OTC
OPEN THERMOCOUPLE DETECT
OTCCLK
OTCEN
R41 30.1K 1%
Q12
Q14 MPS6560
Q15 MPS6560
R40 30.1K 1%
U14 1/2 LM393
UTH
U13 1/2 MC34072
CR2 BAV99
R38 100K
R39 1K
R37 24.9K 1%
C30 0.01 25V
R36 30.1K 1%
C29 0.1 25V
K15-K17 2FORMC RELAY
BOTTOM VIEW
SOT23 COMPONENT PINOUTS
CR1 CR2 TOP AK BAV99
Q10 Q11 Q14 Q15 TOP MPS6560
VR2 VR3 TOP 1N5233
Q2 Q12 Q13 TOP
Q3 TO Q9 TOP SSTH17
2620A-1003 (2 of 3)

Figure 8-4. A3 A/D Converter PCA (cont)


J1
J2
J10
K1
K2
K3
K5
K6
K7
K8
K9
K10
K11
K12
K13
K14
K15
K16
K17
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
L16
L17
L18
L19
L20
L21
L22
L23
L24
U1
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
C6
C7
C10
C11
C13
C14
C17
C31
C32
C34
R10
R11
R35
R42
RT1
RU1
RU2
RED
BLK
Y1
Y2
Z1
Z3
Z4
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP12
TP13

NOTES:

1. TP1 – TP8, TP10 – TP13 ARE NOT COMPONENTS.

2620A-1603

CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY

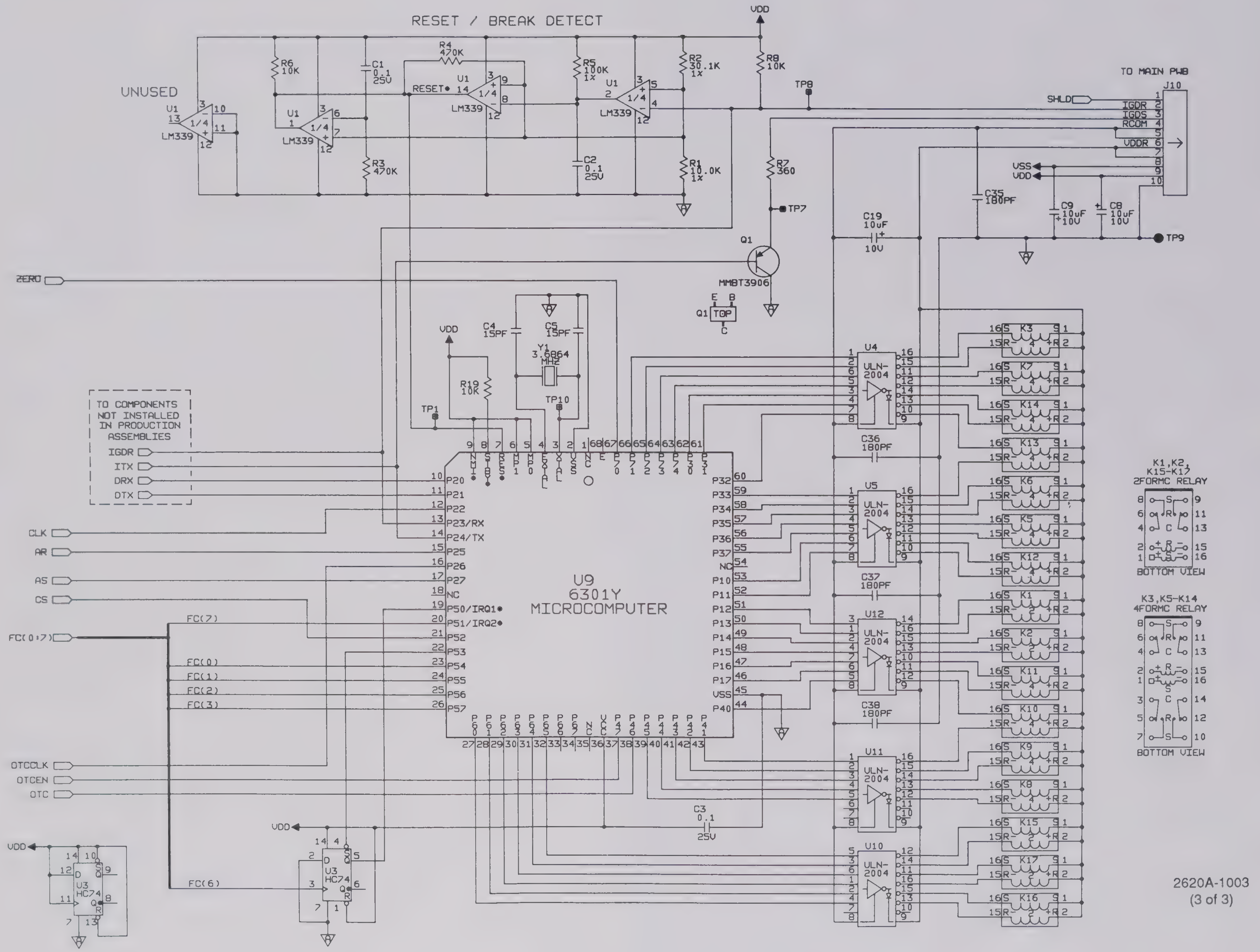
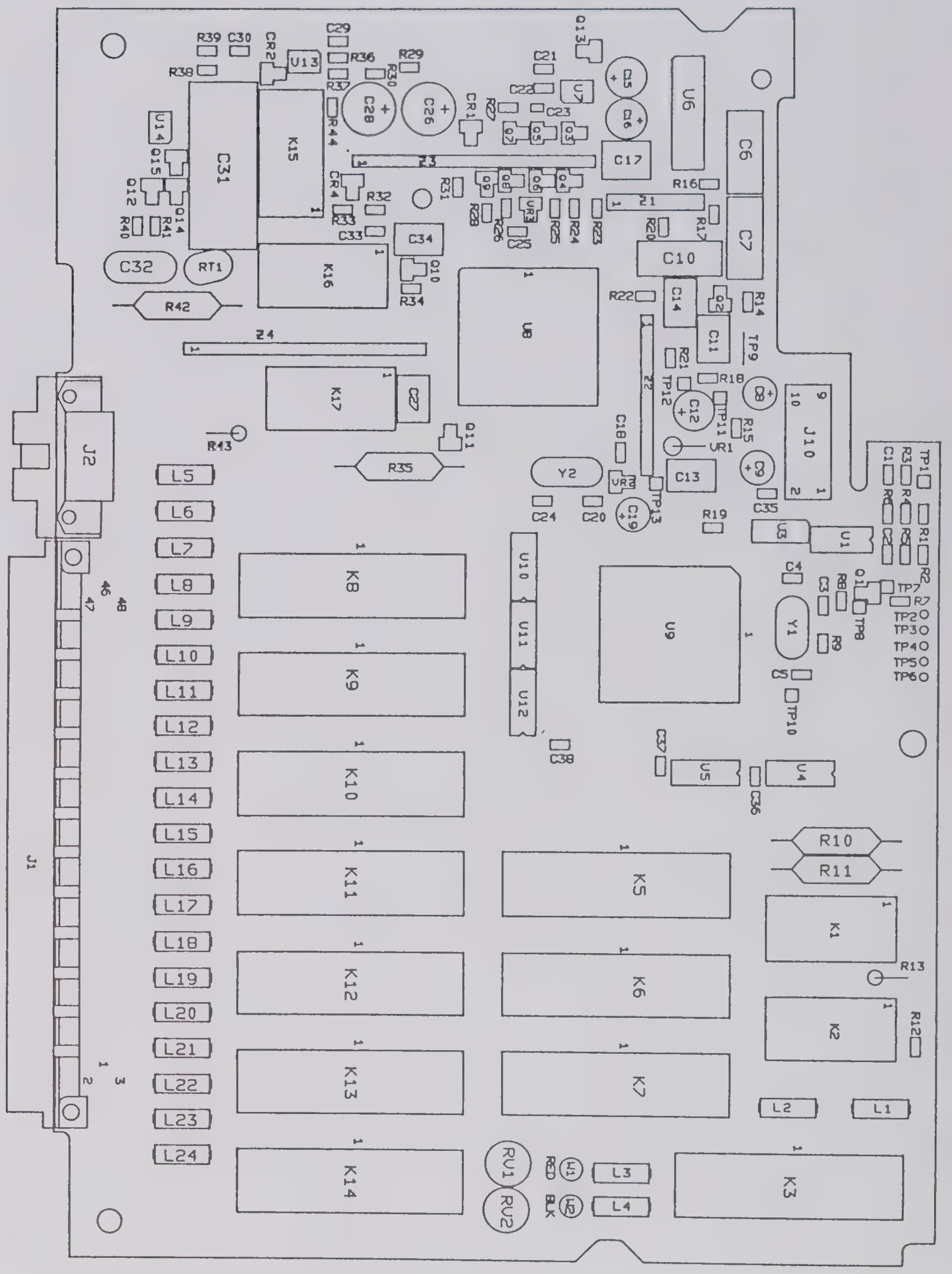

RESET / BREAK DETECT
UNUSED
U1 LM339 1/4
R6 10K
C1 0.1 25V
R3 470K
R4 470K
RESET•
R5 100K 1%
C2 0.1 25V
R2 30.1K 1%
R1 10.0K 1%
R8 10K
VDD
TP8
TO MAIN PWB
J10
SHLD
IGDR
IGDS
RCOM
VDDR
VSS
VDD
R7 360
TP7
Q1
MMBT3906
Q1 TOP E B C
C19 10uF 10V
C35 180PF
C9 10uF 10V
C8 10uF 10V
TP9
ZERO
C4 15PF
C5 15PF
Y1 3.6864 MHZ
R19 10K
TP1
TP10
TO COMPONENTS NOT INSTALLED IN PRODUCTION ASSEMBLIES
IGDR
ITX
DRX
DTX
CLK
AR
AS
CS
FC(0:7)
FC(7)
FC(0)
FC(1)
FC(2)
FC(3)
FC(6)
OTCCLK
OTCEN
OTC
U9 6301Y MICROCOMPUTER
P20
P21
P22
P23/RX
P24/TX
P25
P26
P27
NC
P50/IRQ1•
P51/IRQ2•
P52
P53
P54
P55
P56
P57
P32
P33
P34
P35
P36
P37
NC
P10
P11
P12
P13
P14
P15
P16
P17
VSS
P40
C3 0.1 25V
U3 HC74
U4 ULN-2004
U5 ULN-2004
U12 ULN-2004
U11 ULN-2004
U10 ULN-2004
C36 180PF
C37 180PF
C38 180PF
K3
K7
K14
K13
K6
K5
K12
K1
K2
K11
K10
K9
K8
K15
K17
K16
K1,K2, K15-K17 2FORMC RELAY
BOTTOM VIEW
K3,K5-K14 4FORMC RELAY
BOTTOM VIEW
2620A-1003
(3 of 3)

Figure 8-4. A3 A/D Converter PCA (cont)

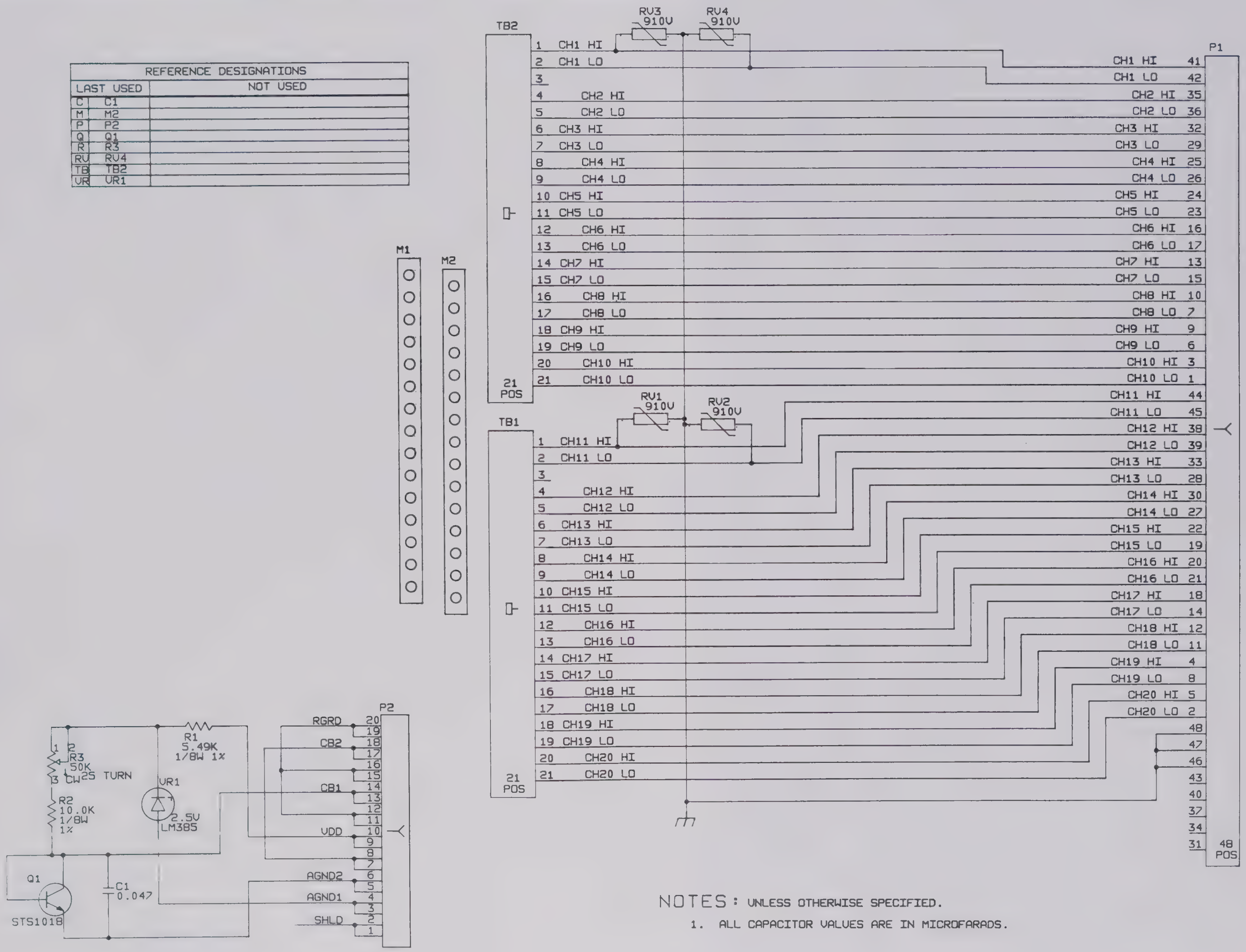

J1
J2
J10
K1
K2
K3
K5
K6
K7
K8
K9
K10
K11
K12
K13
K14
K15
K16
K17
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
L16
L17
L18
L19
L20
L21
L22
L23
L24
U1
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
Y1
Y2
C6
C7
C10
C11
C13
C14
C17
C31
C32
C34
RT1
R10
R11
R35
R42
R43
R13
RU1
RU2
RED
BLK
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP12
TP13
Z1
Z2
Z3
Z4

NOTES:

1. TP1 – TP8, TP10 – TP13 ARE NOT COMPONENTS.

2620A-1603

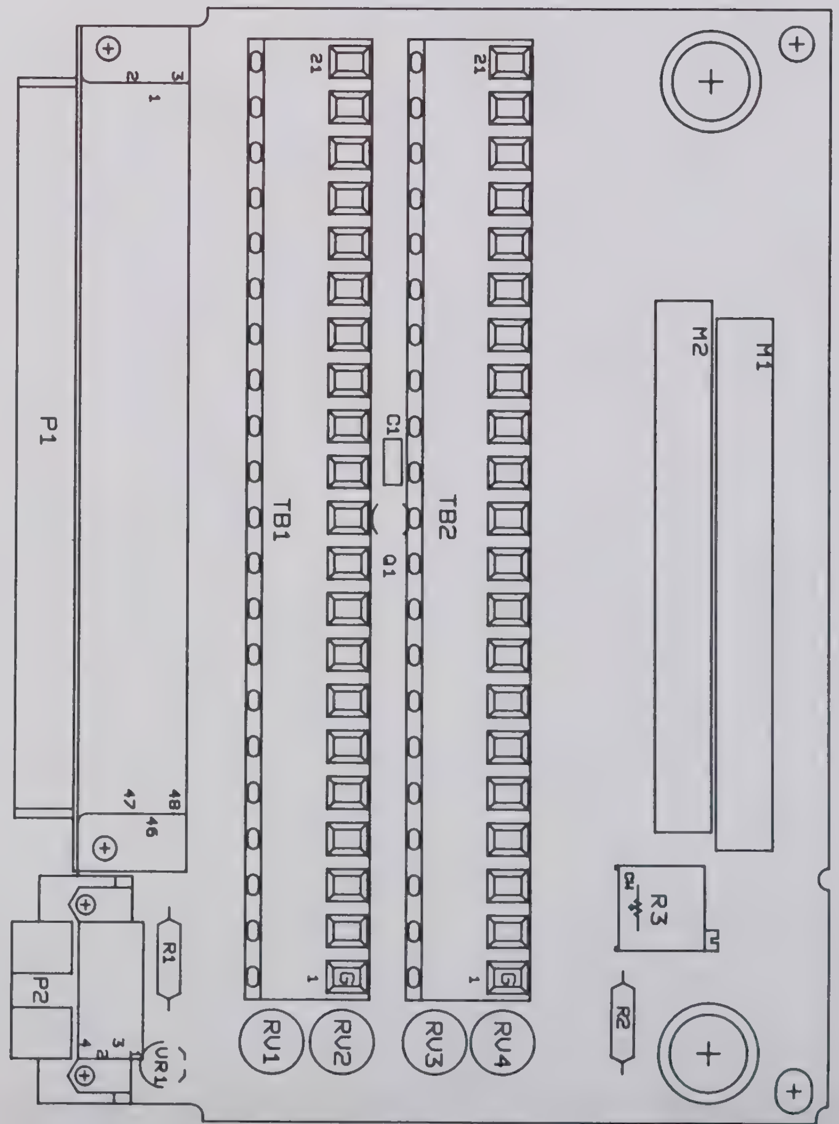
REFERENCE DESIGNATIONS		
LAST USED		NOT USED
C	C1	
M	M2	
P	P2	
Q	Q1	
R	R3	
RV	RV4	
TB	TB2	
VR	VR1	


TB2
1 CH1 HI
2 CH1 LO
3
4 CH2 HI
5 CH2 LO
6 CH3 HI
7 CH3 LO
8 CH4 HI
9 CH4 LO
10 CH5 HI
11 CH5 LO
12 CH6 HI
13 CH6 LO
14 CH7 HI
15 CH7 LO
16 CH8 HI
17 CH8 LO
18 CH9 HI
19 CH9 LO
20 CH10 HI
21 CH10 LO
21 POS
RV3 910V
RV4 910V
TB1
1 CH11 HI
2 CH11 LO
3
4 CH12 HI
5 CH12 LO
6 CH13 HI
7 CH13 LO
8 CH14 HI
9 CH14 LO
10 CH15 HI
11 CH15 LO
12 CH16 HI
13 CH16 LO
14 CH17 HI
15 CH17 LO
16 CH18 HI
17 CH18 LO
18 CH19 HI
19 CH19 LO
20 CH20 HI
21 CH20 LO
21 POS
RV1 910V
RV2 910V
P1
CH1 HI 41
CH1 LO 42
CH2 HI 35
CH2 LO 36
CH3 HI 32
CH3 LO 29
CH4 HI 25
CH4 LO 26
CH5 HI 24
CH5 LO 23
CH6 HI 16
CH6 LO 17
CH7 HI 13
CH7 LO 15
CH8 HI 10
CH8 LO 7
CH9 HI 9
CH9 LO 6
CH10 HI 3
CH10 LO 1
CH11 HI 44
CH11 LO 45
CH12 HI 38
CH12 LO 39
CH13 HI 33
CH13 LO 28
CH14 HI 30
CH14 LO 27
CH15 HI 22
CH15 LO 19
CH16 HI 20
CH16 LO 21
CH17 HI 18
CH17 LO 14
CH18 HI 12
CH18 LO 11
CH19 HI 4
CH19 LO 8
CH20 HI 5
CH20 LO 2
48
47
46
43
40
37
34
31
48 POS
M1
M2
P2
RGRD 20
19
CB2 18
17
16
15
CB1 14
13
12
11
VDD 10
9
8
7
AGND2 6
5
AGND1 4
3
SHLD 2
1
R1 5.49K 1/8W 1%
1 2 R3 50K 3 CW 25 TURN
R2 10.0K 1/8W 1%
VR1 2.5V LM385
C1 0.047
Q1 STS1018
2620A-1004

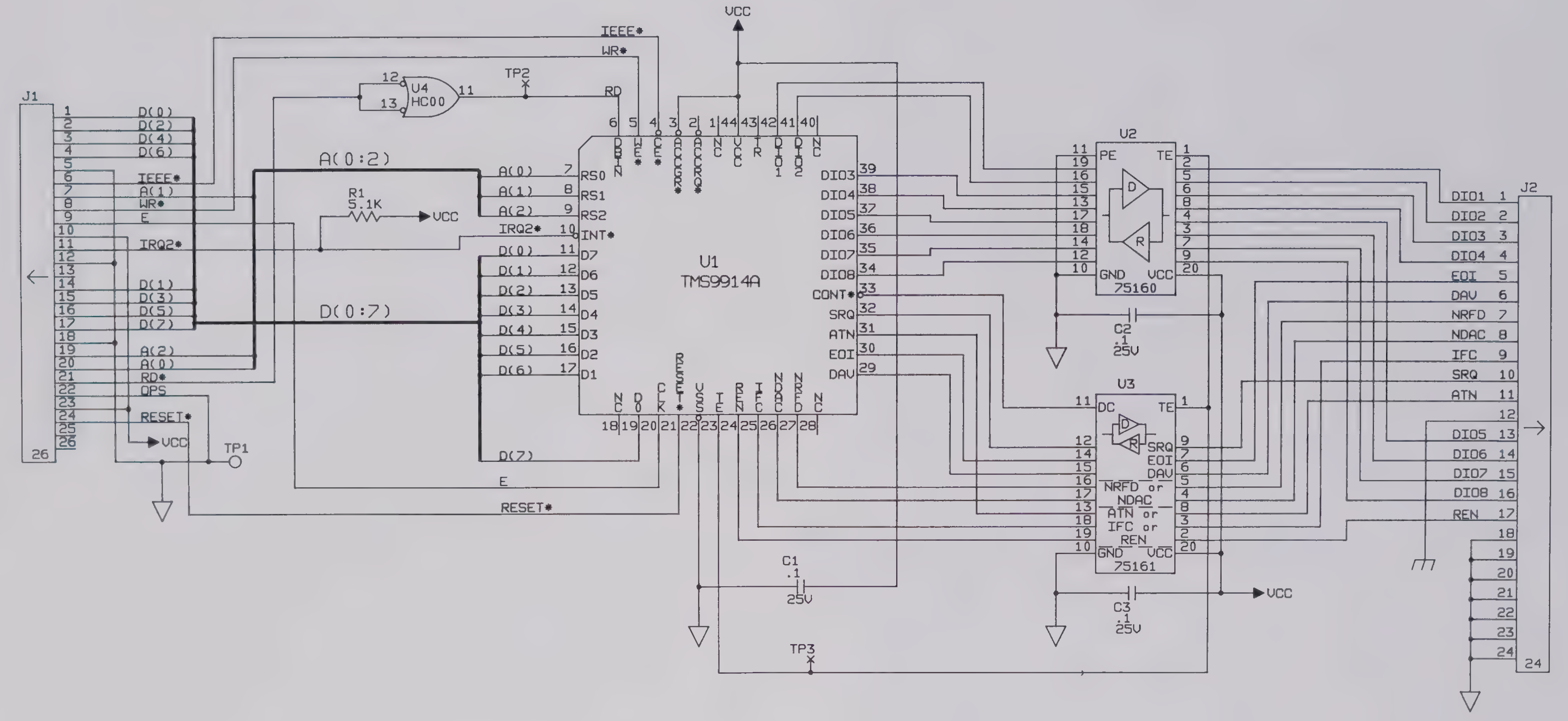
NOTES: UNLESS OTHERWISE SPECIFIED.

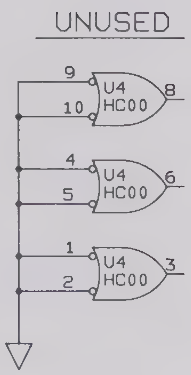
1. ALL CAPACITOR VALUES ARE IN MICROFARADS.

Figure 8-5. A4 Analog Input PCA


P1
P2
TB1
TB2
M1
M2
R1
R2
R3
C1
Q1
VR1
RU1
RU2
RU3
RU4
1
2
3
46
47
48
21
G

2620A-1604


J1
D(0)
D(2)
D(4)
D(6)
IEEE*
A(1)
WR*
E
IRQ2*
D(1)
D(3)
D(5)
D(7)
A(2)
A(0)
RD*
OPS
RESET*
VCC
TP1
26
A(0:2)
D(0:7)
R1
5.1K
VCC
U4
HC00
12
13
11
TP2
RD
IEEE*
WR*
VCC
U1
TMS9914A
RS0
RS1
RS2
INT*
D7
D6
D5
D4
D3
D2
D1
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
CONT*
SRQ
ATN
EOI
DAV
E
RESET*
C1
.1
25V
TP3
U2
75160
PE
TE
GND
VCC
C2
.1
25V
U3
75161
DC
TE
SRQ
EOI
DAV
NRFD or
NDAC
ATN or
IFC or
REN
C3
.1
25V
VCC
J2
DIO1
DIO2
DIO3
DIO4
EOI
DAV
NRFD
NDAC
IFC
SRQ
ATN
DIO5
DIO6
DIO7
DIO8
REN
24

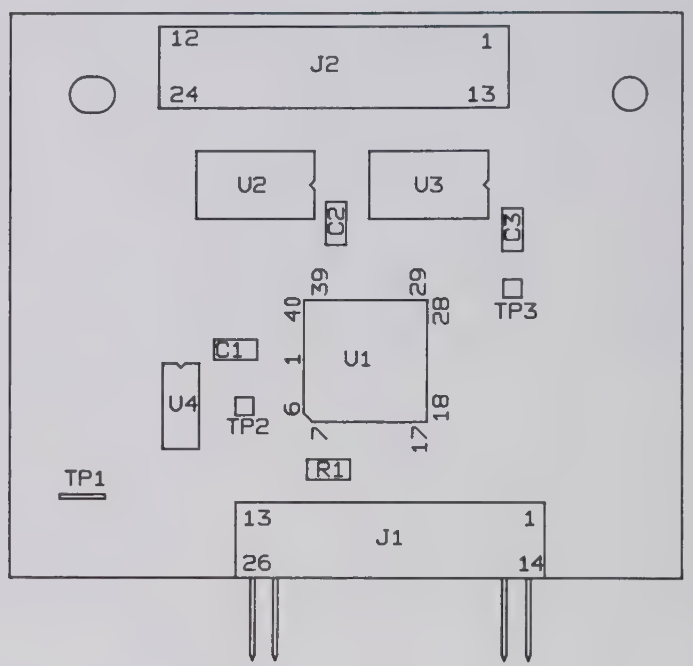

UNUSED
U4
HC00
9
10
8
4
5
6
1
2
3

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE 1/4W, 5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.

REFERENCE DESIGNATIONS		
LAST USED		NOT USED
C	C3	
J	J2	
R	R1	
U	U4	
TP	TP3	

2620A-1005

Figure 8-6. A5 IEEE-488 Interface PCA (2620A only)

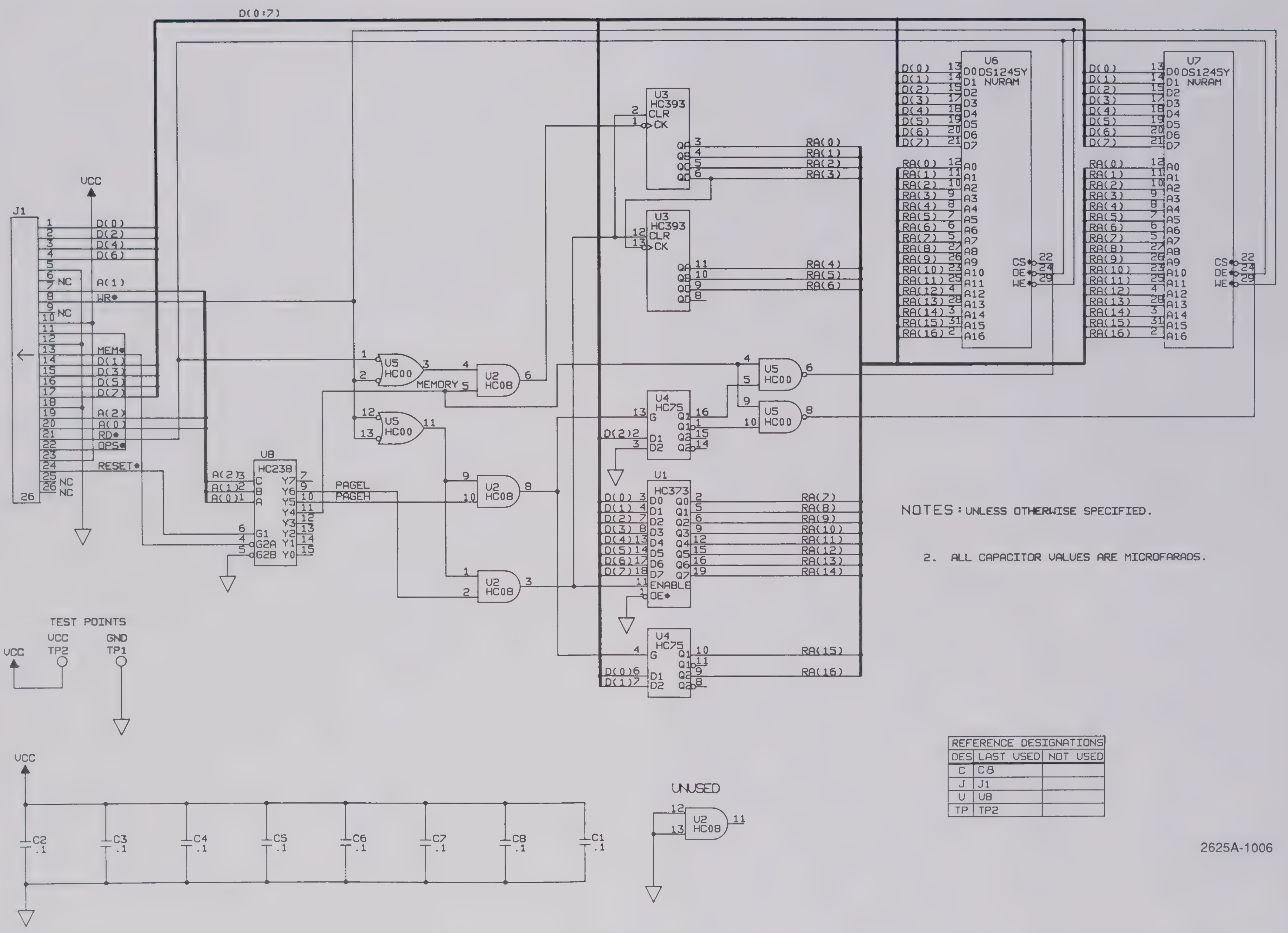


J2
12
1
24
13
U2
U3
C2
C3
U1
39
29
40
28
1
6
18
7
17
TP3
C1
U4
TP2
R1
TP1
J1
13
1
26
14

2620A-1605

CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY

REF DES	POWER SUPPLY PIN NUMBERS	
	VCC (5.1V dc)	GND
A5U1	3,44	22
A5U2	20	10,11
A5U3	20	10
A5U4	14	1,2,4,5,7,9,10


D(0:7)
J1
VCC
D(0)
D(2)
D(4)
D(6)
NC
A(1)
WR*
NC
MEM*
D(1)
D(3)
D(5)
D(7)
A(2)
A(0)
RD*
OPS*
RESET*
NC
NC
26
U8
HC238
A(2)
A(1)
A(0)
G1
G2A
G2B
PAGEL
PAGEH
U5
HC00
MEMORY 5
U2
HC08
U3
HC393
CLR
CK
QA
QB
QC
QD
RA(0)
RA(1)
RA(2)
RA(3)
RA(4)
RA(5)
RA(6)
U4
HC75
D(2)
U1
HC373
ENABLE
OE*
RA(7)
RA(8)
RA(9)
RA(10)
RA(11)
RA(12)
RA(13)
RA(14)
RA(15)
RA(16)
U6
DS1245Y
NVRAM
U7
DS1245Y
NVRAM
CS*
OE*
WE*
TEST POINTS
VCC
TP2
GND
TP1
C2 .1
C3 .1
C4 .1
C5 .1
C6 .1
C7 .1
C8 .1
C1 .1
UNUSED

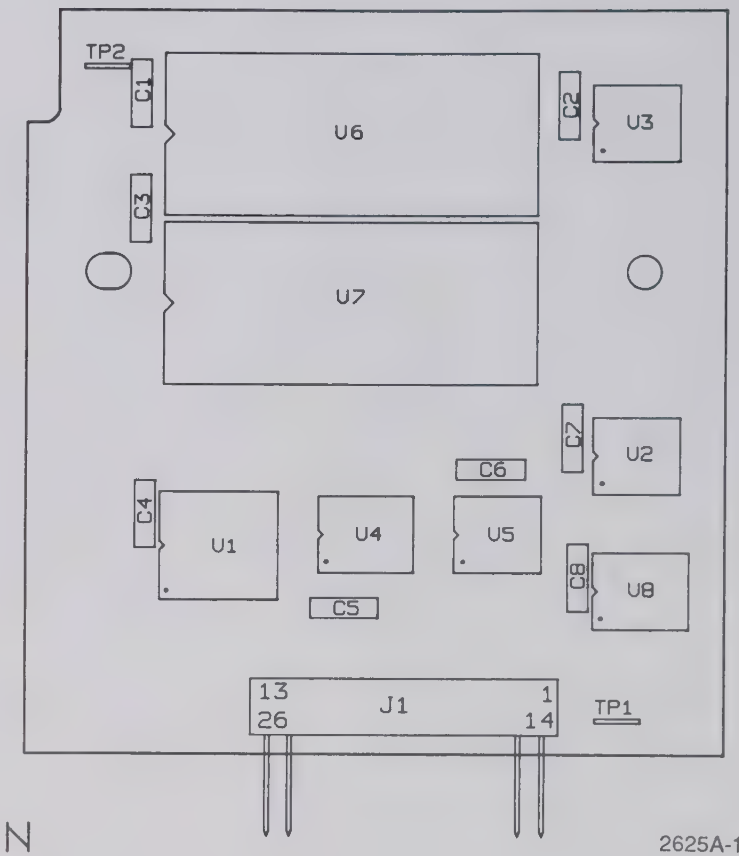
NOTES: UNLESS OTHERWISE SPECIFIED.

2. ALL CAPACITOR VALUES ARE MICROFARADS.

REFERENCE DESIGNATIONS		
DES	LAST USED	NOT USED
C	C8	
J	J1	
U	U8	
TP	TP2	

2625A-1006

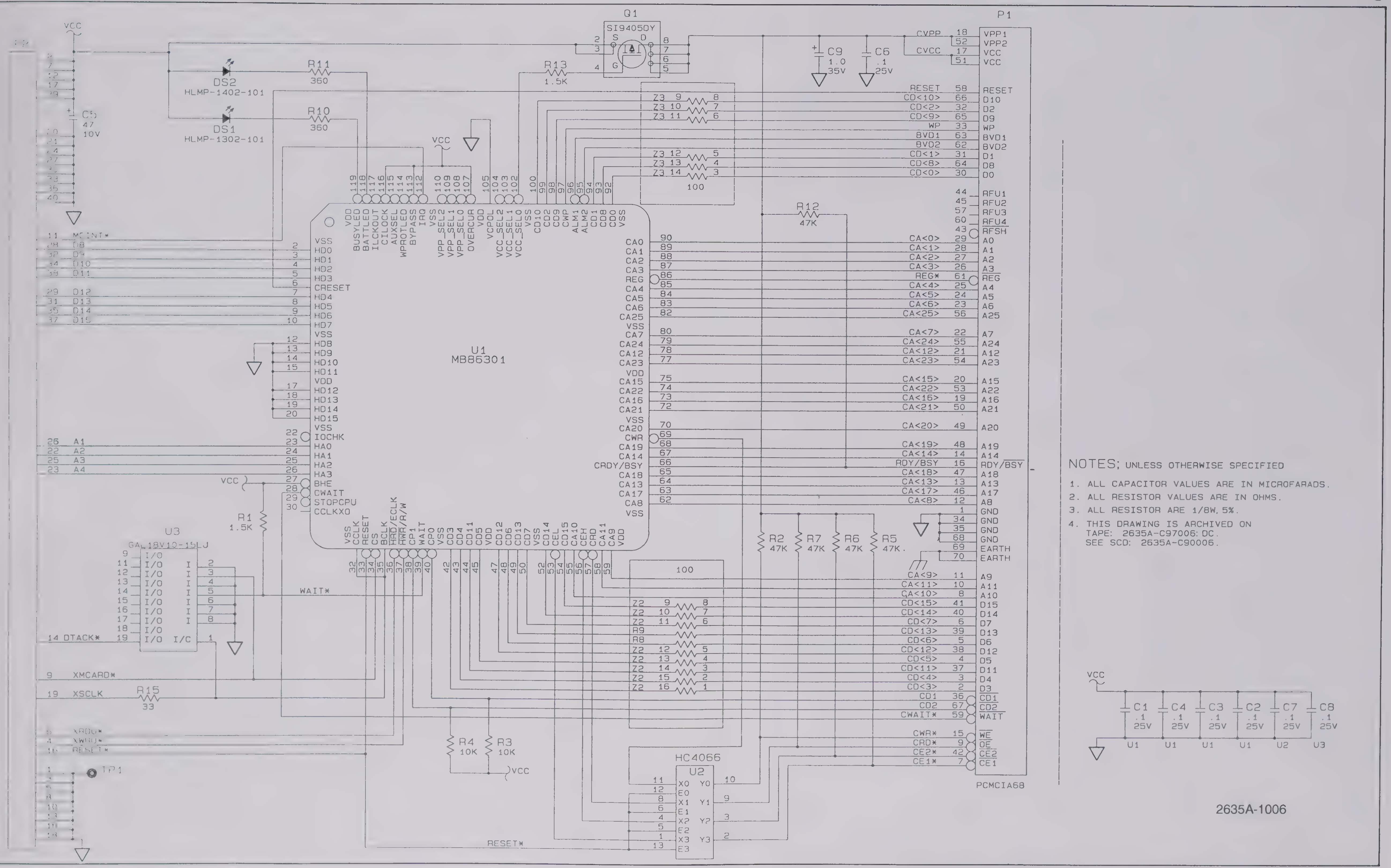
Figure 8-7. A6 Memory PCA (2625A)


TP2
C1
U6
C2
U3
C3
U7
C7
U2
C6
C4
U1
U4
U5
C8
U8
C5
13
26
J1
1
14
TP1

2625A-1606

CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY

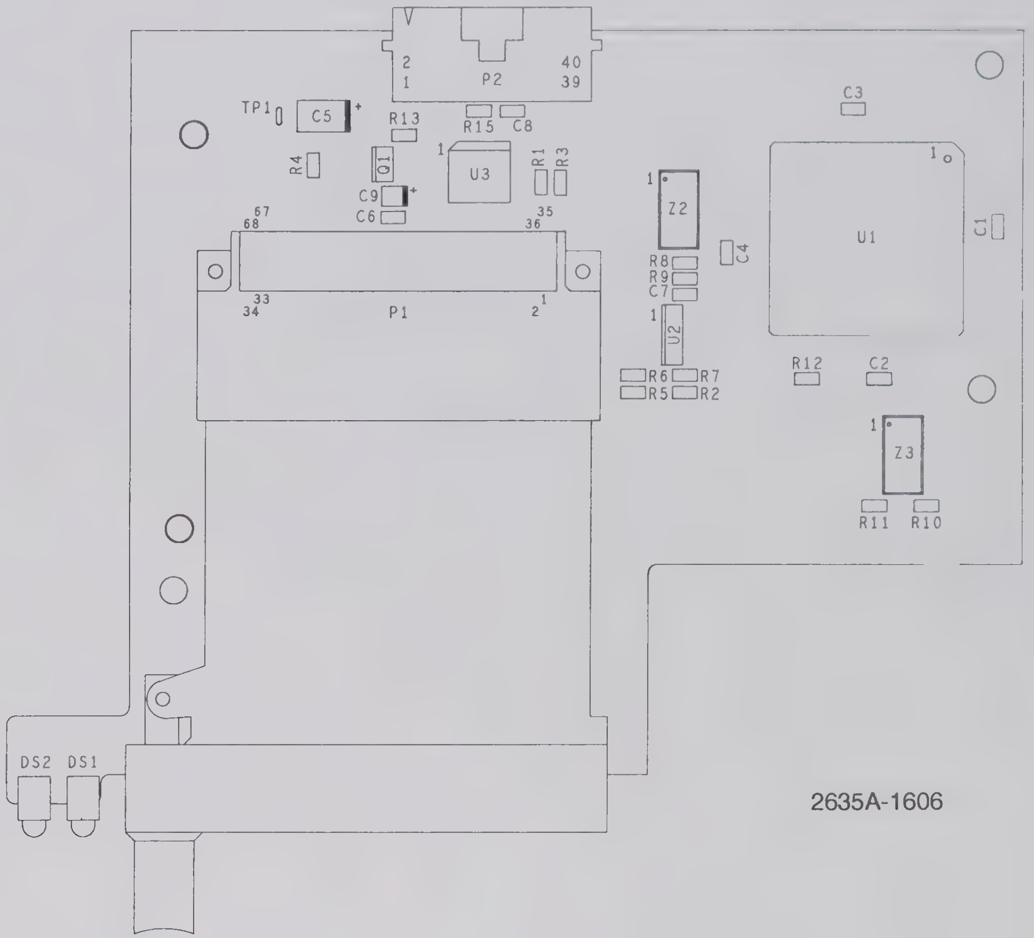
REF DES	POWER SUPPLY PIN NUMBERS	
	VCC (5.1V dc)	GND
A6U1	20	1,10
A6U2	14	7,12,13
A6U3	14	7
A6U4	5	3,12
A6U5	14	7
A6U6	32	16
A6U7	32	16
A6U8	16	5,8


Q1
SI9405DY
P1
PCMCIA68
U1
MB86301
U2
HC4066
U3
GAL18V10-15LJ
DS2
HLMP-1402-101
DS1
HLMP-1302-101
R11 360
R10 360
R13 1.5K
R12 47K
R1 1.5K
R15 33
R2 47K
R7 47K
R6 47K
R5 47K
R4 10K
R3 10K
C9 1.0 35V
C6 .1 25V
C5 47 10V
C1 .1 25V
C4 .1 25V
C3 .1 25V
C2 .1 25V
C7 .1 25V
C8 .1 25V
U1
U1
U1
U1
U2
U3
VCC
100
100
WAIT*
RESET*
DTACK*
XMCARD*
XSCLK
TP1
2635A-1006

NOTES; UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. ALL RESISTOR VALUES ARE IN OHMS.
3. ALL RESISTOR ARE 1/8W, 5%.
4. THIS DRAWING IS ARCHIVED ON
TAPE: 2635A-C97006: DC.
SEE SCD: 2635A-C90006.

Figure 8-8. A6 Memory Card I/F PCA (2635A)


P2
2
1
40
39
TP1
C5
R13
R15
C8
R4
Q1
U3
R1
R3
C9
C6
67
68
35
36
33
34
P1
1
2
Z2
C4
R8
R9
C7
U2
R6
R5
R7
R2
C3
U1
C1
R12
C2
Z3
R11
R10
DS2
DS1

2635A-1606

POWER SUPPLY PIN NUMBERS		
REF DES	VCC (5.0V dc)	GND
A6U1	1,11,12,13,14,15,17,18,	16,27,46,60,76,106,107,
–	19,20,21,31,41,51,61,	113,116,120
–	71,81,91,101,105,111	–
A6U2	7	14
A6U3	2,4,6,7,8,10	20

Reference Designations		
Last Used		Not Used
C	C9	
DS	DS2	
P	P2	
Q	Q1	
R	R15	R14
TP	TP1	
U	U3	
Z	Z3	Z1

HYDRA Starter
Calibration Software

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Section 1
Introducing the Hydra Starter with Cal Package

INTRODUCTION

Hydra Starter with Cal Package™(Starter with Cal) is a menu-driven, software package that operates Hydra remotely from an IBM PC®(or compatible) over an EIA-232-D interface. It is used to transfer configuration data from and to Hydra, log measurement data collected by the Hydra, and manage the acquired data. Hydra Starter With Cal includes an instrument calibration capability not found in the standard starter package.

For details on how to operate Hydra, refer to the Hydra Users Manual (P/N 885988).

Some major features of the Starter with Cal software are:

- Supports one Hydra on EIA-232-D (on COM1 or COM2).
- EIA-232-D communication parameters (baud, parity, etc.,) are selectable, allowing easy communication between the PC and Hydra.
- Hydra can be queried for measurement updates automatically at a user-defined interval. Recorded data are automatically written to a disk file.
- Up load and down load of configuration files.
- Up load of model 2625A logging memory.
- Perform Hydra Calibration

SYSTEM REQUIREMENTS

The Starter with Cal software is designed to run on the IBM PC®, PC-XT®, and PC-AT®, or true compatibles on the MS/PC-DOS operating system.

All instrument setup (channel programming, instrument COM configuration, scan rate selection, etc.) must be done from the Hydra front panel. Starter with Cal does not support remote programming of the instrument configuration. However, Starter with Cal does support up and down loading of the instrument channels configuration and storage of this information to files on the PC.

Hydra Starter with Cal Package is a trademark of John Fluke Mfg. Co., Inc.
IBM PC, PC-XT, and PC-AT are registered trademarks of the International Business Machines Corporation.

Starter with Cal also supports uploading and storing of the Model 2625A data logging memory contents.

Starter with Cal consists of:

1. An executable program file (cal.exe).
2. A help text file (cal.hlp).
3. A default setup save file (cal.ini).
4. MetCal files (flhydrai.cal,flhydrai.ver,flhydrar.cal,flhydrar.ver).

These files are distributed on both 5-1/4 inch (360k) and 3-1/2 inch (720k) diskettes to accommodate PCs with various diskette drives.

Starter with Cal will work with the following standard IBM (or compatible) display boards:

- Standard monochrome text display
- Hercules Graphics Adapter
- Color Graphics Adapter (CGA)
- Enhanced Graphics Adapter (EGA)
- Video Graphics Array (VGA)

USING THIS MANUAL

This manual provides an extended tutorial that demonstrates how to perform a series of operations. These operations introduce you to the menu structure of the Starter with cal software, explain what the menu items do, and teach you how to use them. To this extent, this manual is designed to be worked through rather than simply read through.

Assumptions

This manual assumes that Starter with Cal is configured as shipped from the factory. To ensure this, if a cal.ini file (the Starter with Cal initialization file) is in the current working directory, delete it or copy the cal.ini file from the distribution disk.

Conventions

The following conventions are used in this manual to help distinguish command line keystrokes from surrounding text.

ccc	Hydra and Starter with Cal command names are represented as all lowercase characters. However, these commands can be entered as any combination of uppercase and lowercase characters. Example: freq2 means type the command “FREQ2” in any combination of uppercase and lowercase characters.
⟨ENTER⟩	Means press the carriage return or enter key on your PC.
⟨XXX⟩	Angle brackets enclosing all uppercase characters means press the “XXX” key. Example: ⟨ESC⟩ means press the “ESC” key

How This Manual is Organized

The Starter with Cal User Manual is divided into sections that demonstrate how to perform specific, but related, tasks. Each section is summarized below:

SECTION 1. INTRODUCTION

Introduces Starter with Cal and this manual and indicates system requirements.

SECTION 2. STARTING OUT

Explains how to start Starter with Cal, get around in its menu structure, and establish a communication link with Hydra.

SECTION 3. A PRACTICE SESSION

Takes you through an interactive measurement session, using the Interact and Chart Windows to introduce you to the basics of sending commands to Hydra remotely.

SECTION 4. MENUS AND WINDOWS

Provides a reference guide to the menus and sub-menus.

Section 2
Starting Out

INTRODUCTION

Section 2 explains how to load and run Starter with Cal software, move around the menu structure, and establish a communication link with Hydra.

At each stage of the menu structure, a help message for the currently highlighted menu item or active data entry window is displayed when you press the F1 key. The help text selected is dependent on the current selection in the menu (context sensitive help). When you are done with the help screen, press any key on the keyboard (<space> is convenient) to return to the menu.

WHAT YOU SHOULD KNOW

Starter with Cal is easier to master if you are already familiar with the general operation of Hydra and the IBM Personal Computer.

You should be able to do the following:

- Locate and interconnect the serial ports (EIA-232-D interface connector) on the PC and Hydra.
- Plug in and turn on the PC.
- Specify a path and file name (e.g., 'c:\hsp\cal.exe').
- Specify a pattern for matching (e.g., 'dir a:\*.tst').
- Change the active drive.

You should also be able to use these DOS commands effectively:

- md (make directory, e.g., 'md c:\hydra')
- dir (show directory listing)
- copy (copy a file, e.g., 'copy a:\*.* c:\hydra')
- cd (change working directory, e.g., 'cd c:\hydra')

If you do not know how to perform the actions and use the DOS commands indicated above, refer to the appropriate sections of your computer's operation manual.

SETTING UP

First, make a backup copy of the Starter with Cal disk. Then store the original for safekeeping. Use the copy for day-to-day operations.

CAUTION

Memory Resident programs may cause a loss of serial data when running Starter with Cal. Your ‘autoexec.bat’ file may be executing a program that stays active after returning to DOS (a terminate and stay resident program). It may be necessary to edit the ‘autoexec.bat’ file and reboot.

Connect the IBM PC serial port to Hydra using an appropriate cable.

- Use the Fluke RS40 terminal interface cable (DB-9 to DB-25 female connector) to connect Hydra to a PC, PC/XT, or PS/2.
- Use the Fluke RS41 modem cable (DB-9 to DB-25 male pins) if Hydra is connected to a modem.
- Use both the Fluke RS40 and RS41 cables to connect Hydra to a PC/AT.

Installing Starter with Cal

Install Starter with Cal on a hard disk by performing the following procedure:

1. Change the default drive to the hard disk.
2. Make a directory on the hard disk by entering the DOS command line

   ```
   md hydra ⟨ENTER⟩
   ```

3. Change to this directory

   ```
   cd hydra ⟨ENTER⟩
   ```

4. Insert the Starter with Cal disk into a drive and copy all files to the new hard disk directory. Assuming the floppy drive is drive A:, the hard drive is C:, and you have moved to the new Hydra directory, the copy command would be:

   ```
   copy a: *.* ⟨ENTER⟩
   ```

5. Start the application by typing

   ```
   Cal ⟨ENTER⟩
   ```

   If you want to execute the program from directories other than the one where the files are stored, you should add the subdirectory you created above to the path statement in your ‘autoexec.bat’ file.

   Command line arguments are supported to allow start up from a batch file (such as ‘autoexec.bat’) or to customize the operation of the program. These are as follows:

/g	Startup data collection without Setup Menu.
/fname	Use “name” as the setup configuration file.
/tnumber	Delay “number” seconds before starting.
/m	Use monochrome mode.
/l	Inhibit display of the logo screen at startup.

/d	Dial the modem at data collection startup.
/u	Start up memory upload without Setup Menu.
/uc	Start up memory upload without Setup Menu, then clear memory.

When /g is included on the command line, data collection is entered without any user interaction (the logo and Main Menu screens are not displayed.) Either the default setup file or the file specified in the /f argument is used. The /t argument is used to delay data collection startup until equipment used in the test setup is warmed up and ready.

The /m switch is used to force the use of monochrome display format on a color display adapter. This makes the menu somewhat easier to read on black and white monitors used with a color-capable display adapter (CGA, EGA, or VGA).

The /l switch is used to inhibit the display of the startup logo screen.

The /d switch is used in conjunction with the /g switch to force the program to dial a preselected phone number on an attached modem.

The /u and /uc switches are used to upload the contents of a Hydra Logging Memory without user interaction. Either the default setup file or the setup file specified in the /f argument is used. If /uc is used, the logging memory is cleared after the upload is completed. (When using /u with Hydra Main Firmware version 5.4 or before, the logging memory is always cleared after an upload.)

As an example, you could start data collection (without the Setup Menu) using 'startup.ini' as the configuration file after a 100-second wait with the following command:

```
cal /g /fstartup.ini /t100
```

6. At the opening message, press any key to go to the Main Menu.

MENUS AND ENTRY WINDOWS

The following paragraphs describe how to move around the menus and entry fields in Starter with Cal. The menus are arranged in the order that you will probably use to set up the program. When you first go to the Main Menu, the Setup Menu is displayed. The Setup Menu selections are shown in Figure 2-1.

At the top of the screen is the Main Menu bar. At the bottom of the screen are two lines of text. The first line is a short description of the item currently highlighted; the last line displays the commands that you could perform at this point.

Selecting From a Menu

To select an item within a menu or submenu, do one of the following:

- Use the up/down arrow keys to move the cursor to the desired selection, then press ⟨ENTER⟩.
- Press the key that corresponds to the highlighted letter in the selection, then press ⟨ENTER⟩.

To exit from a menu, press ⟨ESC⟩

There are three types of menu items in Starter with Cal:

- Items with a small arrow displayed next to them will display a lower level menu when that item is selected.
- Items that toggle functions will display a check mark to indicate the choice you have made.
- Items that open a data entry window when they are selected. These windows are described in more detail below.

Once data collection is started, the menu screen is replaced with the data collection screen. You must exit from data collection to go back to the menus. Data collection is inactive during menu operations, and menu operations cannot be performed during data collection.

Data Entry Windows

Data entry windows allow you to enter values (such as a scan interval). To move among entry fields, use the up and down arrow keys or the ⟨TAB⟩ and ⟨SHIFT⟩ ⟨TAB⟩ keys.

An entry field is a field in a submenu in which you can enter or edit information (i.e., file names) or numerical values. Entry fields are easily identified because they are highlighted and prompt you to enter a number, file name, or some other string of characters.

To change an entry, either type an entire new entry, or use the left and right arrow keys to move the cursor to the position of the characters to be changed, and overtype. The ⟨INS⟩ key may be used to toggle character insert mode. If you make a mistake, re-enter the value, or press the ⟨ESC⟩ key to cancel all the entries made during this time.

When you have finished making all entries in a data entry window, type ⟨ENTER⟩ to save the new information, or ⟨ESC⟩ to escape back to the previous menu (⟨ESC⟩ cancels all new entries).

PROBLEMS OPENING STARTER

If the Starter with Cal opening message window does not appear, make sure that you have done the following:

- Loaded DOS Version 2.1 or later.
- Placed the 'cal.exe' file in either your current working directory or in the PC's path list.
- Used the correct command to start up Starter with Cal (cal ⟨ENTER⟩).

Until Starter with Cal is running, error messages originate from the operating system.

USING ON-LINE HELP

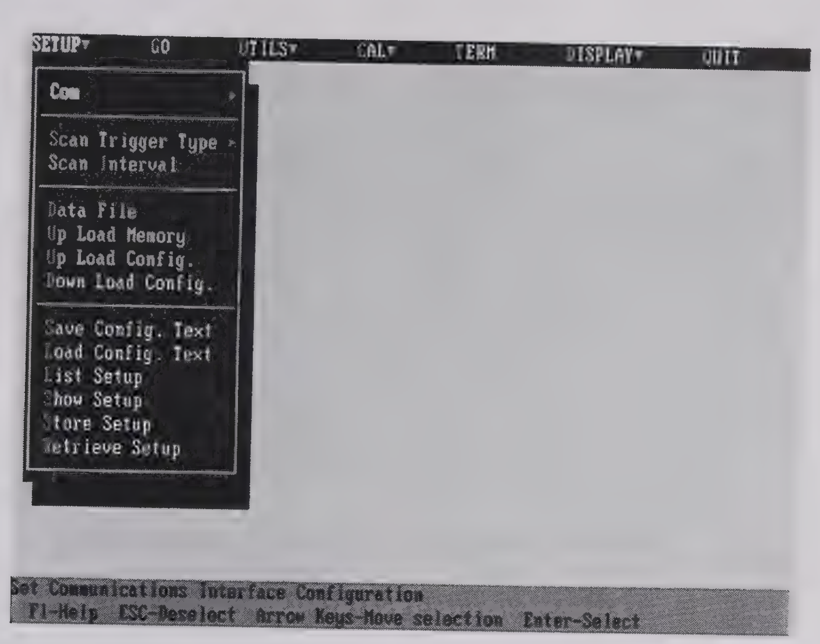
On-line help is available for most of the menu items and data entry windows.

Press <F1> to display an appropriate Help screen for the menu item or window.

Press any key to remove the help message and return to the previous screen.

LINKING THE PC AND HYDRA

Starter with Cal supports one Hydra at a time. Be sure that the EIA-232-D (COM1 or COM2) port on the PC is cabled to the EIA-232-D connector on the Hydra rear panel, then proceed as follows:


SETUP
GO
UTILS
CAL
TERM
DISPLAY
QUIT
Com
Scan Trigger Type
Scan Interval
Data File
Up Load Memory
Up Load Config.
Down Load Config.
Save Config. Text
Load Config. Text
List Setup
Show Setup
Store Setup
Retrieve Setup

Set Communications Interface Configuration
F1-Help ESC-Deselect Arrow Keys-Move selection Enter-Select

Figure 2-1. Setup Screen

1. Turn Hydra ON.
2. Select ‘Com’ from the Setup Menu by pressing ⟨ENTER⟩,
3. Select ‘COM1’ or ‘COM2’ with the up or down arrow key, then press ⟨ENTER⟩.
4. When you enter your choice the next menu appears; select the desired baud rate and parity or ‘Autobaud’. If you select a specific baud rate and parity, these must match those selected on Hydra.

USING A MODEM TO LINK THE PC AND HYDRA

If you are using a modem pair to connect the PC and Hydra, you will need to setup the modem parameters immediately after selecting the COM port parameters. You can select the phone number to dial, the dialing mode, originate mode, and dialing times. Before using the connection, you must select the “Dial” menu entry to establish communication.

Section 3
A Practice Session

INTRODUCTION

Section 3 walks you through a practice session with Starter with Cal and provides an example data collection session.

SETTING UP A SCAN

Use Hydra's front panel controls to configure several channels. Use the PC to control scanning, data collection, and communications.

From the Main Menu you can configure the data collection process of Hydra and view configuration information. You can transfer configuration to and from Hydra, and you can store or retrieve configuration information from files on the PC disk.

NOTE

Section 2 describes how to choose and select menu items.

SETUP Menu

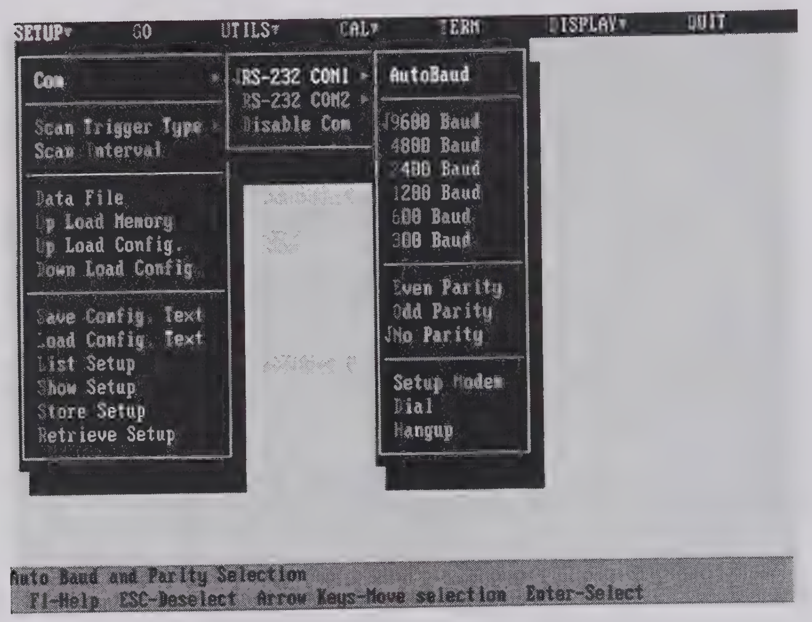
NOTE

When you are storing, retrieving, or loading configuration information, be aware of the following distinctions: 1. Configuration data covers only the settings for Hydra (channel definitions, etc.) 2. Setup data includes both the Hydra configuration data and all other settings for this experiment (scan trigger type, data file name, etc.).

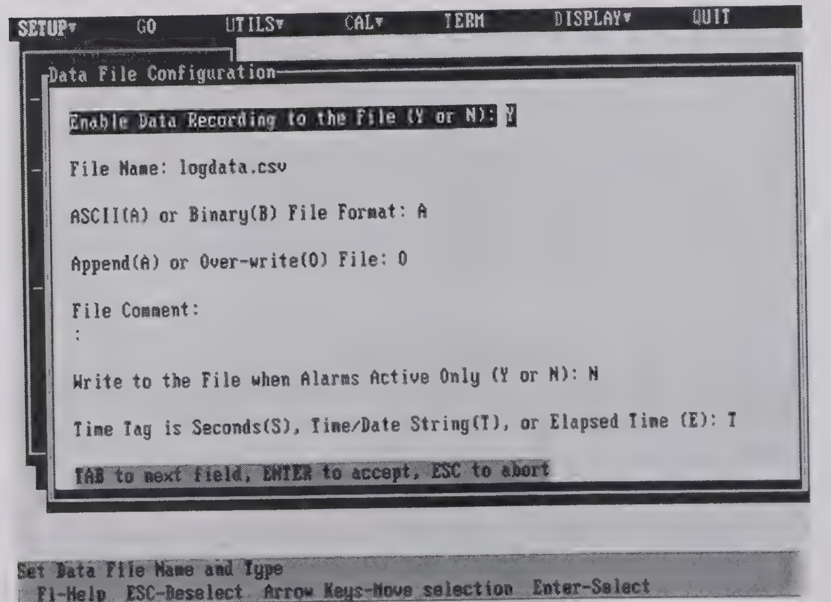
Make sure that Hydra is properly connected to the PC before turning both Hydra and the PC on, then check the communication port setup. Use the 'Com' item in the Setup Menu. Figure 3-1 shows an example of setting Hydra to communicate with the PC via EIA-232-D COM1 on 9600 baud and no parity. Note that a check flags each chosen selection.

Alternatively, you may select 'AutoBaud' and allow the program to automatically adapt to the baud rate and parity set in Hydra. However, if you are using a modem or other active communication device, you should select a specific baud rate and parity. Some communication devices have problems when Starter with Cal tries different baud rates while executing the AutoBaud algorithm.

Next, set up the data file that will be used during data collection. To do this, select 'Data File' from the Setup Menu to open an entry window. Refer to Figure 3-2.


SETUP
GO
UTILS
CAL
TERM
DISPLAY
QUIT
Com
Scan Trigger Type
Scan Interval
Data File
Up Load Memory
Up Load Config.
Down Load Config.
Save Config. Text
Load Config. Text
List Setup
Show Setup
Store Setup
Retrieve Setup
RS-232 COM1
RS-232 COM2
Disable Com
AutoBaud
9600 Baud
4800 Baud
2400 Baud
1200 Baud
600 Baud
300 Baud
Even Parity
Odd Parity
No Parity
Setup Modem
Dial
Hangup

Auto Baud and Parity Selection
F1-Help ESC-Deselect Arrow Keys-Move selection Enter-Select


SETUP
GO
UTILS
CAL
TERM
DISPLAY
QUIT

Data File Configuration

Enable Data Recording to the File (Y or N): Y

File Name: logdata.csv

ASCII(A) or Binary(B) File Format: A

Append(A) or Over-write(O) File: O

File Comment:
:

Write to the File when Alarms Active Only (Y or N): N

Time Tag is Seconds(S), Time/Date String(T), or Elapsed Time (E): T

TAB to next field, ENTER to accept, ESC to abort

Set Data File Name and Type
F1-Help ESC-Deselect Arrow Keys-Move selection Enter-Select

Figure 3-2. Data File Configuration Entry Window

Use the up and down arrow keys or the TAB key to select the entry to change. Then either overtype the entire entry or move to the character you wish to change and insert the new text. When complete, press ⟨ENTER⟩ to change the data base entries. If you make a mistake, press ⟨ESC⟩ to cancel the changes.

Save this configuration for future use by selecting the 'Store Setup' menu item. The entry window prompts you for a configuration file name. Enter any file name you wish, or just press ⟨ENTER⟩ to use the defaults. Instrument configuration can be retrieved for later use by selecting the 'Retrieve' menu item.

GO Menu

When the Hydra configuration setup is complete, select GO from the Main Menu to start data collection. During data collection, the display shows the most recent set of readings from Hydra. See Figure 3-3.

Channels in alarm are displayed in red or are highlighted on a monochrome monitor.

The last line of collection information shows the totalizer reading and the current state of the alarms and digital I/O lines.

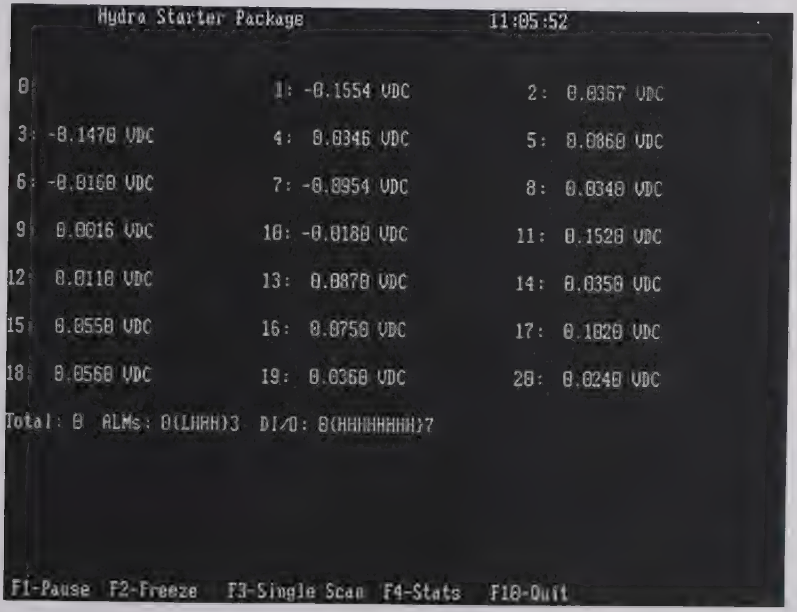
The PC function keys that are functional during data collection are also displayed on the bottom line of the screen. The keys and their functions are as follows:

F1 Pause

Pauses data collection; no additional readings are taken until a key is pressed.

F2 Freeze

Freezes the display; readings are still being taken and stored in the data file while in this mode.



```
        Hydra Starter Package                        11:05:52

 0:                     1: -0.1554 VDC          2:  0.0367 VDC

 3: -0.1470 VDC         4:  0.0346 VDC          5:  0.0860 VDC

 6: -0.0160 VDC         7: -0.0954 VDC          8:  0.0340 VDC

 9:  0.0016 VDC        10: -0.0180 VDC         11:  0.1520 VDC

12:  0.0110 VDC        13:  0.0870 VDC         14:  0.0350 VDC

15:  0.0550 VDC        16:  0.0750 VDC         17:  0.1020 VDC

18:  0.0560 VDC        19:  0.0360 VDC         20:  0.0240 VDC

Total: 0  ALMs: 0(LHHH)3  DI/O: 0(HHHHHHHH)7




F1-Pause  F2-Freeze   F3-Single Scan  F4-Stats   F10-Quit
```

Figure 3-3. Data Collection Screen

F3 Single Scan

Performs a single scan. During a long interval between scans, F3 can be used to force an immediate scan without interfering with the existing interval countdown.

F4 Stats

Displays data collection statistics.

F10 Quit

Quits data collection and returns to the Main Menu.

UTILS Menu

After completing the scan, convert the data to a different format. Open the UTILS Menu to perform file maintenance functions. Refer to Figure 3-4.

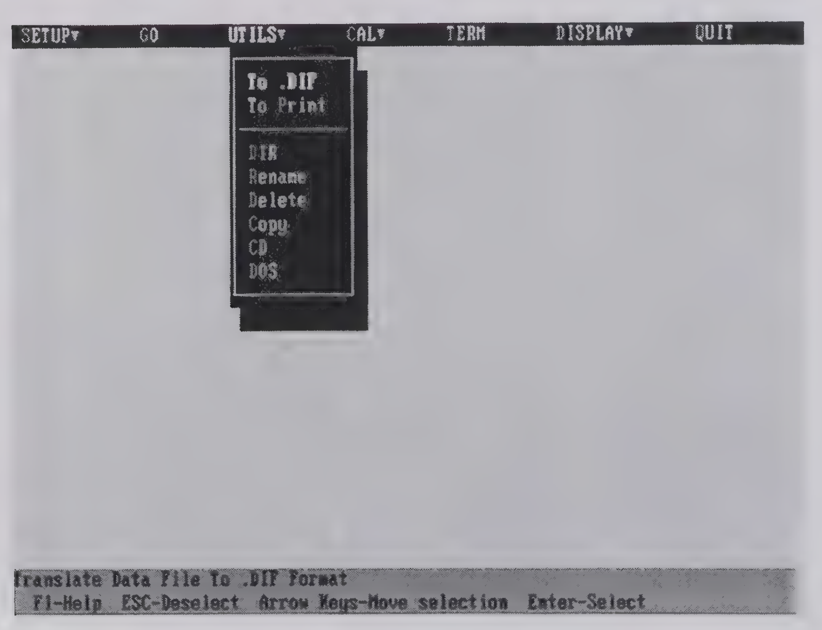
The 'To .DIF' and 'To Print' items are used to translate the data file to these formats. The other items in this menu are general file-management tools that function like their DOS equivalents.

CAL Menu

This menu is used to calibrate the Hydra. To initiate calibration, first put the Hydra instrument into calibration mode, then select the calibration section from the Cal Menu.

When calibration is completed for a section, you are asked if you would like to continue on to the next section. If a complete calibration is desired, select Cal Volts DC as the first calibration section.

You must supply calibration signals to the instrument via channel 1 (and channel 11 for Resistance Cal). Be sure your calibration source and wiring is ready before starting calibration. (See CALIBRATION procedure in section 4 of this service manual).



Translate Data File To .DIF Format
F1-Help ESC-Deselect Arrow Keys-Move selection Enter-Select

Figure 3-4. Utilities Menu

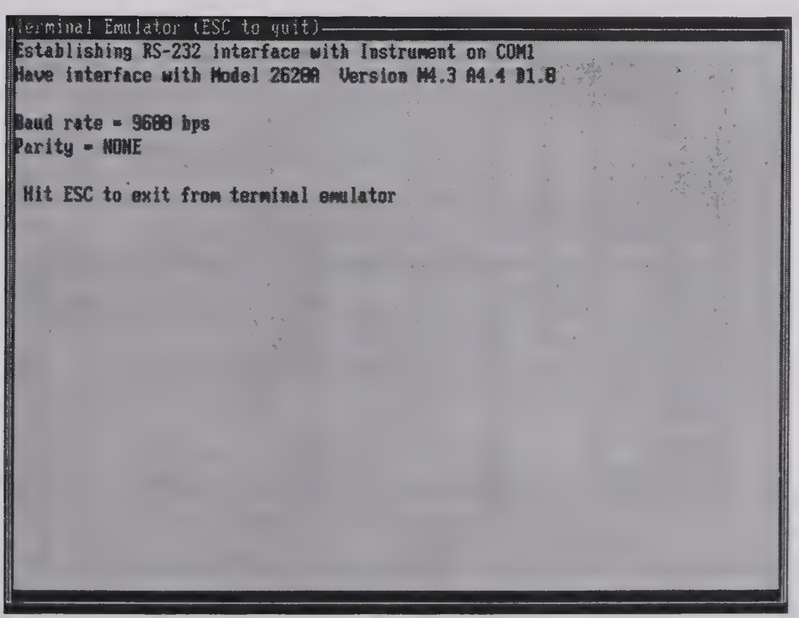
TERM Menu

If a communication problem occurs between the PC and Hydra, or if you want to try direct communication with Hydra using the Hydra Computer Interface Commands, use the Terminal Emulator. When activated, the emulator does extensive testing of the communication interface and, if communication is successfully established, the screen shown in Figure 3-5 is displayed.

Before using the emulator, be sure the communication parameters and the modem (if in use) are properly set up. Once this screen is displayed, you may type commands (e.g., *IDN?). Refer to Section 4 of the Hydra User Manual for complete descriptions of computer interface commands. These commands are sent to Hydra and the response from Hydra is displayed on the screen. Press ⟨ESC⟩ to return to the Main Menu.

QUIT Menu

When you are ready to exit from Starter with Cal, select QUIT from the Main Menu. If you have changed any configuration parameters during the session, you are prompted to save the changes before quitting.



```
Establishing RS-232 interface with Instrument on COM1
Have interface with Model 2620A  Version M4.3 A4.4 D1.0

Baud rate = 9600 bps
Parity = NONE

 Hit ESC to exit from terminal emulator
```

Figure 3-5. Terminal Emulator Screen

Section 4
Menus and Windows

INTRODUCTION

Section 4 is a reference guide to the windows and pull-down menus you will encounter while operating Starter with Cal.

MAIN MENU

The pull-down menus on the menu bar are described below. When a Main Menu selection is made, a lower level menu or data entry box is displayed. As the highlight bar is moved to each menu entry, a short description of the entry is also displayed near the bottom of the screen. (Refer to Section 2 for more information about how to select menu entries and enter data into fields.)

SETUP

Com

Set Communications Interface Configuration. Opens submenus. Press ⟨ENTER⟩ to select the communication port (COM1 or COM2) Hydra is connected to. This selection opens a third submenu that provides baud, parity, and modem settings.

Scan Trigger Type

Select Scan Triggering Type. Sets the method for scan triggering. The following choices are available:

- Interval Scan Trigger: enables/disables interval scan triggering.
- Ext./Mon. Trigger Off: disables both external and monitor alarm trigger methods. Does not affect interval scan triggering.
- External Trigger: enables triggering scans on the external trigger input signal.
- Monitor Alarm Trigger: enables triggering scans when the monitor channel is in alarm.

External Trigger and Monitor Alarm Trigger methods are mutually exclusive. However, Interval triggering can be combined with External or Monitor Alarm triggering methods. See the Hydra User Manual for more details.

Scan Interval

Set Scanning Interval. Open a window with a time field for you to enter the time interval between measurement scans. If you do not have Interval scan triggering enabled and you do have either Monitor Alarm or External triggering enabled, scans will not start until the trigger condition is satisfied. (Refer to the External or Monitor Alarm Trigger help screens).

Data File

Set up the Data File. Open a data entry window to set the data collection file name, format (ASCII, or binary), function (Overwrite or Append), a file comment (if desired), and time tag format.

Up Load Memory

Transfer the contents of the 2625A logging memory to a data file. The file created is the same as if the data was collected in real time from scans. You are prompted to enter the name of the data file to create.

Since the data memory in Hydra may contain over 2000 sets of scan readings, it may take a substantial period of time to complete this transfer.

Up Load Config.

Upload Configuration from the Instrument. Automatically loads the PC with all the instrument and channels configuration that you entered via the Hydra front panel. A message window opens to tell you whether or not the upload was successful. Note that this information is then stored in PC RAM memory; it has not been stored in a disk file yet.

Down Load Config.

Download Configuration to Hydra. Allows you to transfer the instrument and channels configuration from the PC memory that you previously uploaded or loaded from a disk file.

Save Config. Text

Save Configuration to a text file. Allows you to save the instrument and channels configuration to a text file. A window prompts you for the file name. If you press ⟨ENTER⟩, the program assigns a default name. If you enter a name without an extension (no period "." in the name), a default extension of '.cfg' is assigned. A message window tells you whether or not the save was successful.

Load Config. Text

Text Load Configuration from a text file. Allows you to load the instrument and channels configuration into the PC from an ASCII text file on the PC disk. The window prompts you for the file name. If you press ⟨ENTER⟩, the program assigns a default name. If you enter a name without an extension (no period "." in the name), a default extension of '.cfg' is assigned. A message window tells you whether or not the load was successful.

List Setup

Make a Configuration Listing File. This selection allows you to write the instrument and channels configuration to a file in a listing format that is easy to read. A window opens and prompts you for the file name. If you press ⟨ENTER⟩, the program assigns a default name. If you enter a name without an extension (no period "." in the name), a default extension of '.lst' is assigned. A message window tells you whether or not the write operation was successful.

Show Setup

Display the Program and Instrument Setup. Selecting this entry brings up a display of the program and instrument configuration parameters. Be sure to upload the configuration from the instrument or "Retrieve Setup" from a file on the disk before selecting this item. Use the PgUp and PgDn and arrow keys on the PC to see the entire listing.

Store Setup

Store the Program Setup. Causes the program and instrument configuration to be stored in a file on the PC disk. A window opens and prompts you for a file name. If you press ⟨ENTER⟩, the program assigns a default name. If you enter a name without an extension (no period "." in the name), a default extension of '.ini' is assigned. The file name 'cal.ini' is loaded when you run the program unless the /fname switch is included in the startup command line.

Retrieve Setup

Retrieve the Program Setup. This entry causes the program and instrument configuration to be retrieved from a file on the computer disk. A window opens and asks you to enter a file name into the selected field. If you press ⟨ENTER⟩, the program is assigned a default name. If you enter a name without an extension (no period "." in the name), a default extension of '.ini' is assigned.

GO

Configure Hydra via the front panel, or use the 'Load Config. Text' and 'Down Load' facilities, to set up Hydra before selecting GO. Remember to enable interval scanning or some type of scan trigger because no data will be transferred to the PC until a scan is performed.

This menu selection opens a window with the prompt to press 'y' or 'n' to confirm entry to the data collection mode.

Press 'y' to start data collection. When you begin data collection, the PC does the following: initializes the interface, establishes communication with Hydra, uploads the present Hydra configuration, starts data acquisition, and displays the data acquisition screen.

During data collection, the Hydra front-panel keys are locked to prevent changes to the configuration during the run, and the latest scan readings taken by Hydra are displayed on the PC.

When data collection is started, new data appended to an existing data file is checked for format consistency. If the format of the file is inconsistent with the format of the new data, the format already established for the data file is used.

The data is appended to the data file after each scan. The file is closed after each scan pass to prevent data loss due to power failure or computer malfunction.

Function keys (listed at the bottom of the screen) allow you to freeze or pause the scan, perform a single scan, view the statistics of the scan, or quit scanning.

If no Hydra is attached to the PC, or if communication is disabled at the time data collection is started, the program will ask if you want to run in simulation mode. In this mode, data is collected from a simulated instrument. The data represents a saw-tooth shaped sequence with the maximum = 1.0 and the minimum = -1.0.

UTILS

Each of the UTILS Menu selections accesses a submenu. The following utilities function in the same way as their DOS equivalents: DIR, Rename, Delete, Copy, and CD.

To .DIF

Translate data file to .DIF format. This selection allows you to translate a data file into .DIF (data interchange format). This format is used by spreadsheet and data analysis programs for data importation.

To Print

Translate Data File to Print Format. Converts the data file from a data acquisition run to a printable format. This format is suitable for printing or importation to a word processor.

DIR

Display Current Directory. When selected, displays the files and subdirectories in the current directory.

Rename

Rename a File. This allows you to change the name of a file.

Delete

Delete a File. Select this to delete a file from the DOS directory structure.

Copy

Copy a File. Select this to copy an existing file into a new file. The original file is not changed or deleted.

CD

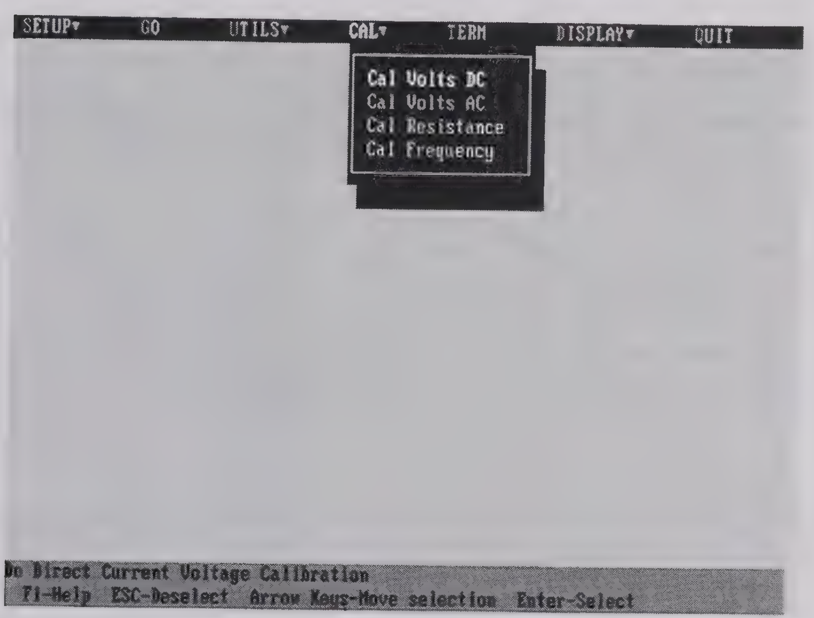
Change Directory. Select this to change to a different current subdirectory.

DOS

Execute DOS Command. Allows you to enter a single DOS command and view the results.

CAL

This menu selection allows you to calibrate the Hydra Instrument. Hydra calibration is divided into 4 sections, as shown in Figure 4-1. Each Cal section is independent of the others. For example, you may calibrate the Resistance measurement section without calibrating the other three sections.



Dc Direct Current Voltage Calibration
F1-Help ESC-Deselect Arrow Keys-Move selection Enter-Select

Figure 4-1. Calibration Menu Screen

NOTE

Hydra must be in calibration mode before selecting the calibration menu section.

After a calibration section is selected, Starter with Cal checks if the Hydra is in calibration mode, then prompts for the ideal calibration signals. If your calibration source is incapable of supplying the requested signal, select a signal (voltage, frequency, resistance) that is close and enter the value of the signal actually being supplied.

When entering values, the character "K" may be used for E+3 and the character "M" for E+6.

See CALIBRATION procedure in section 4 of this service manual for more information on preferred calibration signal values and wiring diagrams.

Once a calibration section is completed, you are given the opportunity to proceed into the next section or terminate calibration.

All calibration steps in a section must be completed before the calibration parameters become effective. If you terminate calibration before the last step in a section is complete, the entire section is invalidated.

TERM

This menu selection allows you to enter a terminal emulator mode to communicate directly with Hydra via the computer interface. The Hydra computer interface command set can be used in emulator mode.

Terminal emulation can be used to diagnose problems with the computer/Hydra interface and to display the Hydra model and software versions.

You must set up the communication method, port number, baud rate, parity, and modem (if in use) before using the terminal emulator.

When the terminal emulator is active, everything you type on the PC keyboard is sent to Hydra, and everything Hydra sends is displayed on the screen.

Press ⟨ESC⟩ to exit from terminal emulator mode.

DISPLAY

Light Background:	Displays characters on a light backgound.
Dark Background:	Displays character on a dark backgound.
European Format:	Displays commas (,) instead of decimal points (.) in number displays.

QUIT

Allows you to exit to the operating system. When selected, a window opens and asks if you are sure you really want to quit. You must answer y before you may exit.

If you have changed any of the configuration setup parameters during the session, and have not yet saved the setup (selected ‘Store’ under the Setup Menu), you are asked if you want to save the setup before exiting the program.

Appendix A
File Formats

THE DATA FILE

The data file is maintained in either binary or comma-separated ASCII format, as selected during setup. The binary format is much more compact than the ASCII format, but ASCII format is needed for compatibility with data analysis and management tools running simultaneously in other computers on a network.

Data files are opened in SHARED mode with write blocked. This enables network reads but prevents writes of the data file while scan data is being recorded. Between scans, the file is closed, allowing full network access to the file (including delete if allowed by the security level enabled on the PC). If the file disappears between one scan and the next, a new file (including header and with the previous file name) is created automatically before the next set of scan data is recorded.

Binary File Format

The binary file format is as follows:

FILE HEADER

TAG -	1 byte (contents = FF hex)
File Name -	81 character string
Time Count -	4 bytes (long integer - seconds
Comment -	80-byte string
Hydra Count -	1 byte (1)
Spare -	1 byte (to get word alignment)
Units -	23 9-byte strings.

DATA RECORDS (One for each Scan recorded)

Time Count -	4 bytes (long integer - seconds past midnight 1/1/70
Channel Readings -	84 bytes (21, single precision (4 byte), IEEE format, floating point numbers)
Totalizer -	4 bytes (long integer - the extended totalizer maintained by the logger software)
Digital and Alarms I/O -	2 bytes (a 16 bit integer with bits 0-7 bits representing the digital I/O state and bits 8-11 the

Each scan record consists of the current time (a 32-bit integer) plus 21 floating-point numbers (84 bytes) reflecting the readings from all channels. The readings section is followed by a floating-point number (4 bytes) for the totalizer, followed by a 16-bit (2-byte) integer for the Digital Input/Output. If a measurement channel is off, 0.0 is recorded for the reading.

In this format, slightly less than 100 bytes will be consumed for each scan recorded, so 10,000 scans can be recorded in a 1-Meg file.

Comma-Separated ASCII File Format

The comma-separated ASCII file format is as follows (⟨EOL⟩ means "end of line marker"):

- File name string (<64-character string) ⟨EOL⟩
- Date and time file was created⟨EOL⟩
- File comment (<80-character string) ⟨EOL⟩
- Number of Hydras being logged (1 character) ⟨EOL⟩
- Channel Units string (21 comma-separated strings) ⟨EOL⟩
- Scan Record 1⟨EOL⟩
- Scan Record n⟨EOL⟩

Each scan record consists of the time (in seconds past midnight, 1/1/70, or ASCII time/date string) and a comma separated list of channel readings (including the totalizer and digital input/output). The strings are surrounded by quotes so they can be directly imported to Lotus 1-2-3TM and other data analysis and presentation packages.

In this format, each scan consumes about 250 bytes. A 1-Meg file can hold about 4,000 scans.

CHANNELS AND INSTRUMENT CONFIGURATION TEXT FORMAT

This file is an image of the Hydra commands necessary to configure all 21 channels in Hydra. It is an ASCII text format and can be read or edited by the user. It contains the Hydra computer interface commands necessary to fully configure Hydra.

PROGRAM SETUP FILE FORMAT

This file is used to save the user-entered data collection setup parameters. The file is in binary format and is read during program startup to set the default values for the session.

You may overwrite this file with the current setups via functions in the Setup menu. You may also restore the setups to what is in the file by the same means.

Until a setup file is retrieved from the disk, the following setup defaults will be active:

Setup File Name:	'cal.ini'
Data File Name:	'logdata.dat'
Conf. Text File:	'config.cfg'
Format:	ASCII
Function:	append
Comment:	blank
Trigger Type:	Interval (external and mon alarm disabled)
Scan Interval:	10 seconds
Interface;	EIA-232-D (COM1)
Baud Rate:	9600
Parity:	None

Manual Supplement

Manual Title:	Hydra Service	Supplement Issue:	**1**
Part Number:	889589	Issue Date:	7/96
Print Date:	May 1991	Page Count	24
Revision/Date:	3, 9/94		

This supplement contains information necessary to ensure the accuracy of the above manual. Enter the corrections in the manual if either of the following conditions exist:

1. No Rev. letter is provided at the beginning of the change.
2. The Rev. letter of the indicated pca is equal to or higher than that given with each change.

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CHANGE #1 - 50360

On page 6-25, Table 6-5,

ADD:	W1/WIRE, JUMPER, TEF, 22AWG, WHT, .300/528257/89536/528257/1 NOTES: 1. W1 is not installed on 2620A and 2625A instruments.

On pages 6-26 and 8-21, Figures 6-5 and 8-3 (2620A-4002), add W1 as shown in Figure A.

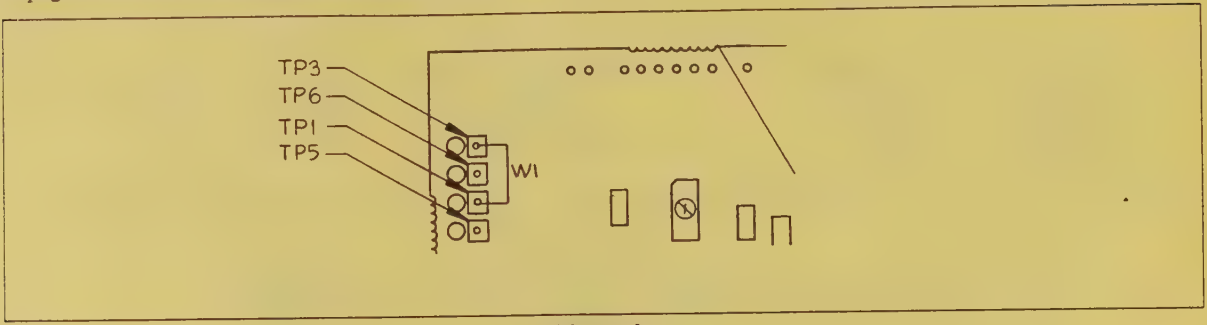
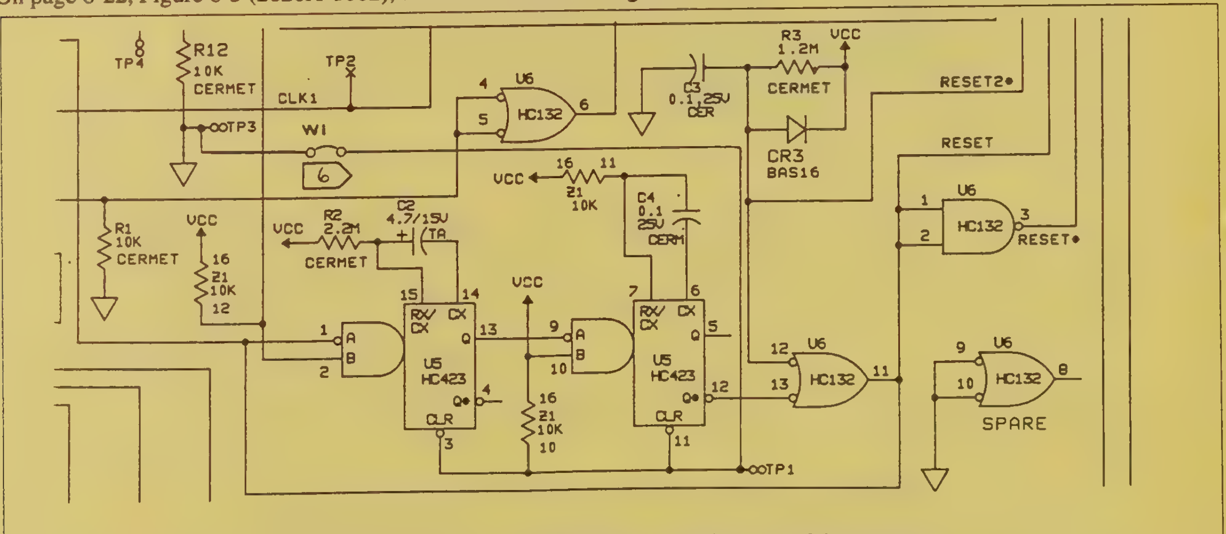

TP3
TP6
TP1
TP5
W1

Figure A.

On page 8-22, Figure 8-3 (2620A-1002), add W1 as shown in Figure B.


TP4
R12
10K
CERMET
TP2
CLK1
TP3
W1
6
U6
HC132
4
5
6
R3
1.2M
VCC
C3
0.1,25V
CER
CERMET
CR3
BAS16
RESET2*
RESET
VCC
16
11
21
10K
C4
0.1
25V
CERM
R1
10K
CERMET
VCC
16
21
10K
12
VCC
R2
2.2M
CERMET
C2
4.7/15V
TA
15
14
1
2
A
B
RX/CX
CX
Q
Q*
CLR
U5
HC423
13
4
3
VCC
9
10
16
21
10K
10
7
6
5
12
11
TP1
12
13
11
1
2
3
RESET*
9
10
8
SPARE

Flag note 6 = W1 is not installed on 2620A or 2625A instruments.

Figure B.

CHANGE #2 - 50593

Rev. -C, A4 Analog Input PCA(2620A-4004)

On page 6-30, Table 6-7, add L1 and make the following changes:

ADD:	L1/CORE, BALUN, FERRITE, .136,.079,.093/106184/89536/106184/1
CHANGE:	C1/CAP,CER,0.047UF, +-10%,50V,X7R/572263/04222/SR215C473KAA/1
TO:	C1/CAP,CER,1000PF,+-5%,50V,C0G,1206/867408/89536/867408/1
CHANGE:	H55/SCREW, PH,P,THD CUT, SS,4-24,.375/183574/889536/183574/2
TO:	H55/RIVET,S-TUB,OVAL,STL,.087,.375/106473/89536/106473/1

On pages 6-31 and 8-29, Figures 6-7 and 8-5 (2620A-1604), add L1 as shown in Figure C.

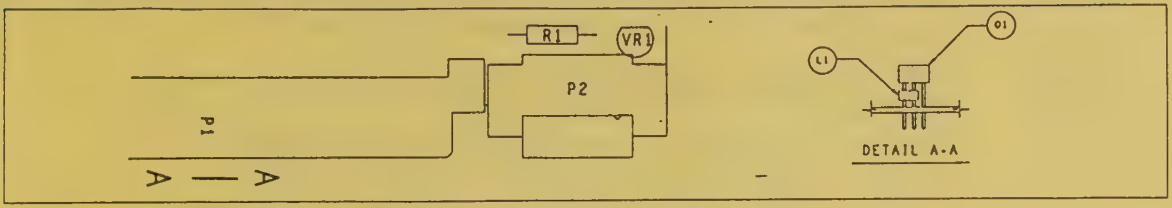

R1
VR1
P2
P1
A — A
L1
Q1
DETAIL A-A

Figure C.

On page 8-30, replace part of Figure 8-5 (2620A-1004) as shown in Figure D.

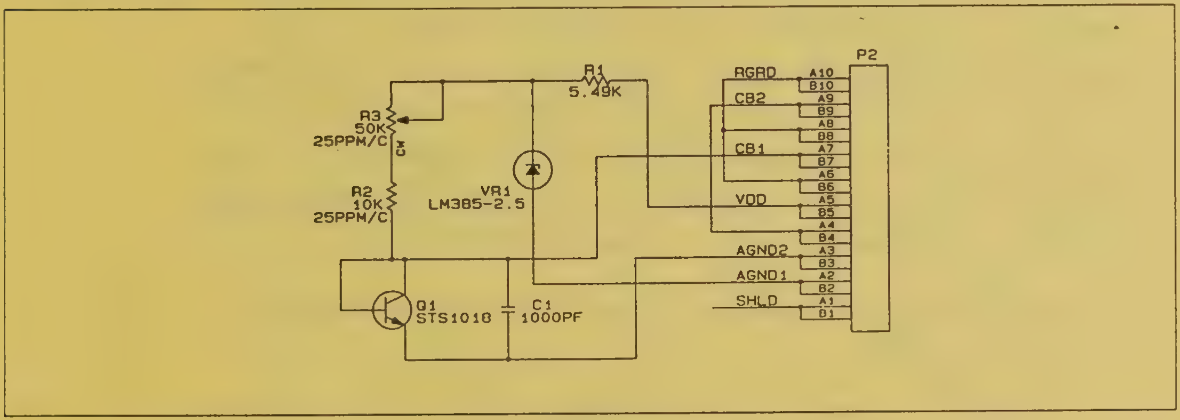

P2
R1
5.49K
RGRD
CB2
CB1
VDD
AGND2
AGND1
SHLD
A10
B10
A9
B9
A8
B8
A7
B7
A6
B6
A5
B5
A4
B4
A3
B3
A2
B2
A1
B1
R3
50K
25PPM/C
CW
R2
10K
25PPM/C
VR1
LM385-2.5
Q1
STS1018
C1
1000PF

Figure D.

CHANGE #3 - 50651

On page 6-12, Table 6-2,

CHANGE:	H53/SCREW,FHU,P,LOCK,SS,6-32,.250/769893/73734/6-32X1-4FHUCPS2A/1
TO:	H53/SCREW,FHU,P,LOCK,SS,6-32,.250/**320093/89536/320093**/1

CHANGE #4- 51298

Rev. -B, A1 2635A Main PCA (2635A-4001)

On pages 6-21 and 6-22, Table 6-4, add C1,18 and make the following changes:

ADD:	C1,18/CAP,AL,220UF,20%,35V,SOLV PROOF/929708/89536/929708/2
CHANGE:	C1,4,5,32,34/CAP/AL/1UF,+-20%/50V,SOLV PROOF/782805/62643/KMA50105M4X7LL/5
TO:	C,4,5,32,34/CAP/AL/1UF,+-20%/50V,SOLV PROOF/782805/62643/KMA50105M4X7LL/4
CHANGE:	CR1,10/DIODE,SI,100 PIV,3.3 AMPS, SCHOTTKY/837740/59993/30WQ10F/2
TO:	CR1,10/DIODE,SI,60 PIV,3A, SCHOTTKY/943097/89536/943097/2
CHANGE:	C11,15,16,19,22-25,..../CAP,CER,0.1UF,+-10%,25V,.../747287/04222/12065C104KATBA/29
TO:	C11,15,16,19,21-25,..../CAP,CER,0.1UF,+-10%,25V,.../747287/04222/12065C104KATBA/30
CHANGE:	R23/RES,CF,220K,+-5%,0.25W/851837/59124/CF1/4 224J/1
TO:	R19,31/RES,CERM,11K,1%,.1W,100PPM,0805/928796/89536/928796/2
CHANGE:	R26/RES,CERM,10.5K,+-1%,.125W,100PPM,1206/851852/91637/CRCW1206-1052FB/1
TO:	R26/RES,CERM,100, 5%,.125W,200PPM,1206/746297/89536/746297/1

CHANGE: R29-31/RES,CF,0.50, +-5%,0.25W/830646/59124/CF1/4 R 50J/3
TO: R30/RES,CERM,45.3K,1%,100PPM,0805/930201/89536/930201/1

CHANGE: U8/IC,OP AMP,DUAL,LOW POWER,SOIC/867932/6E570/LM358D/1
TO: U8,28/IC,OP AMP,DUAL,LOW POWER,SOIC/867932/6E570/LM358D/2

CHANGE: U9/IC,VOLT REG,ADJ,SWITCHING REGULATOR/867135/27014/LM2579T/1
TO: U9/IC,VOLT REG,ADJ,SWITCHING 100KHZ,5A/929591/89536/929591/1

DELETE: C18/CAP,CER,33PF,+-10%,50V,C0G,1206/769240/04222/12065A330KATBA/1

DELETE: C20/CAP,CER,1800PF,+-10%,50V,C0G,1206/769786/04222/12065A182KATBA/1

DELETE: C21/CAP,CER,820PF,+-5%,50V,C0G,1206/867403/04222/12065A821JATBA/1

DELETE: R17/RES,CF,1M,+-5%,0.25W/649970/59124/CF1/4 105J/1

DELETE: R18/RES,CERM,10M,+-5%,0.125W,.../783274/91637/CRCW1206-1005JB02/1

DELETE: R19/RES,CERM,11K,+-1%,0.125W,.../867291/91637/CRCW1206-1102FB/1

DELETE: R24/RES,CERM,64.9K,+-1%,.125W,.../876086/91637/CRCW1206-6492FB/1

DELETE: R27/RES,CERM,220K,+-5%,.125W,.../746750/91637/CRCW1206-2203JB02/1

DELETE: R32,33/RES,CF,1,+-5%,0.25W/867866/59124/CF1/4 1ROJ0/2

On pages 6-24 and 8-11 through 8-19, replace Figures 6-4 and 8-2 (2635A-1601) with Figure E.

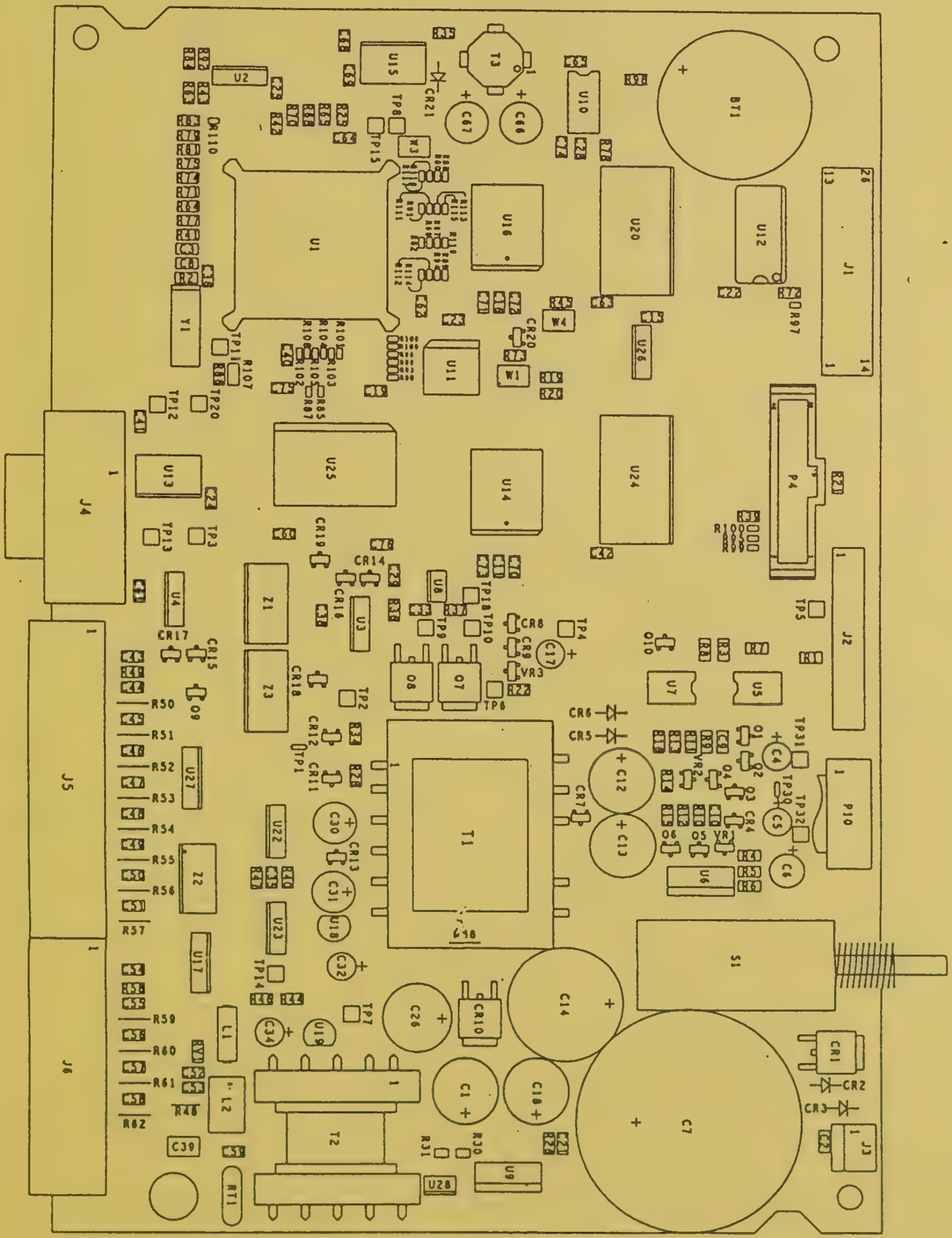

U2
U15
T3
C67
C66
CR21
TP8
TP15
W3
U10
BT1
+
CR110
U1
U16
U20
U12
J1
26
13
14
1
Y1
TP11
R107
TP20
TP12
R101
R103
R105
R104
R102
R106
R87
U11
W4
W1
CR20
U26
R97
J4
1
U13
TP13
TP3
U25
CR19
U14
U24
P4
R100
CR14
U4
CR17
CR15
Z1
CR16
U8
U3
TP18
TP10
TP9
CR8
CR9
C17
VR3
TP4
Q10
J2
TP5
Q8
Q7
TP6
Z3
CR18
TP2
U7
U5
J5
R50
Q9
R51
R52
U27
R53
CR12
TP1
CR11
C30
U22
CR13
T1
CR6
CR5
C12
C13
CR7
Q1
C4
TP31
VR2
Q4
Q2
Q3
CR4
C5
TP30
TP32
P10
Q6
Q5
VR1
C6
U6
R54
R55
Z2
R56
R57
C31
U18
U23
648
TP14
C32
S1
U17
R59
C26
CR10
C14
TP7
U19
C34
L1
R60
R61
R46
L2
T2
C1
C18
C7
CR1
CR2
CR3
J3
R31
R30
U9
U28
C39
RT1
R62

Figure E.

On page 8-12, replace Figure 8-2 (2635A-1001) with Figure F.

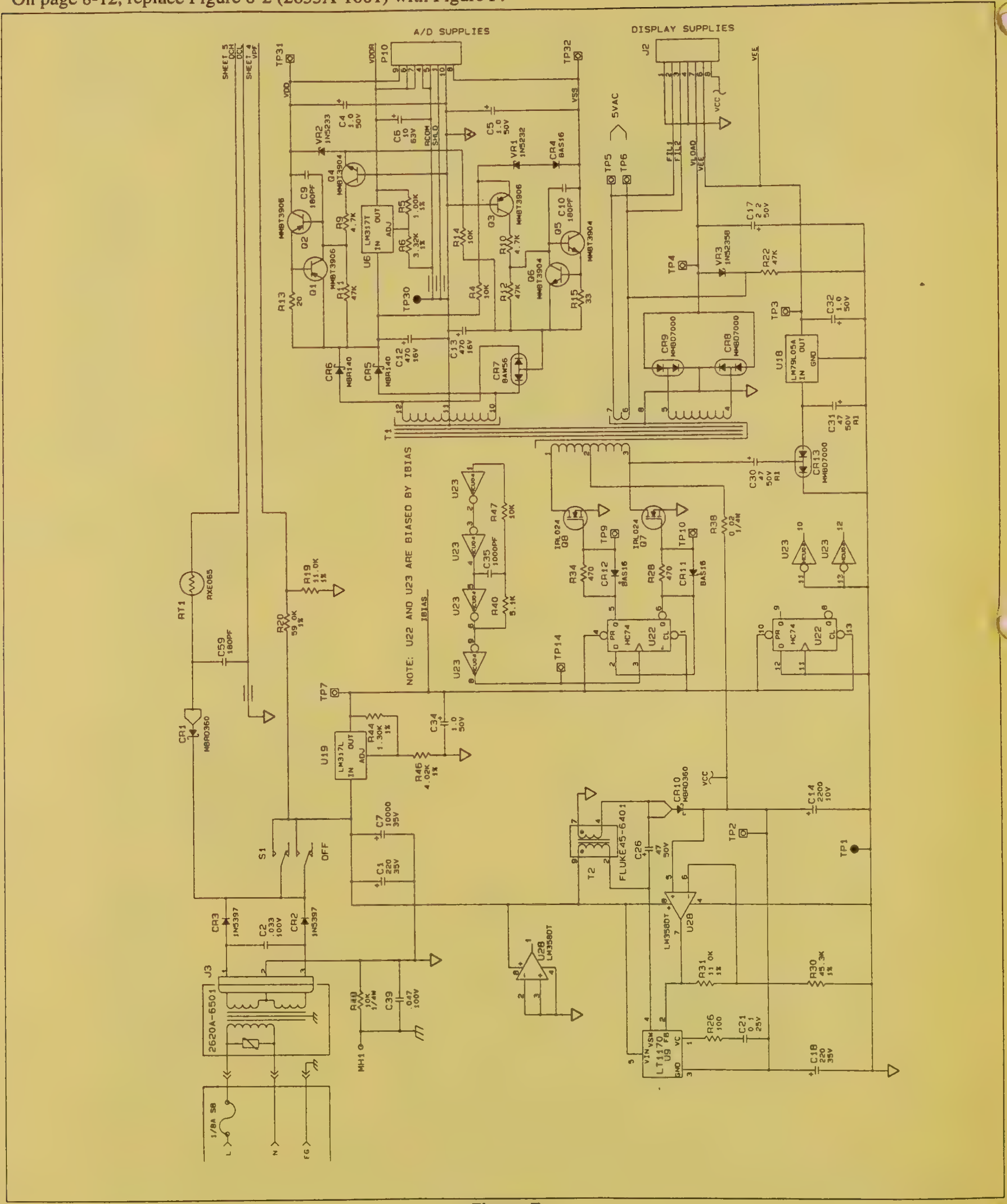

A/D SUPPLIES
DISPLAY SUPPLIES
SHEET 5 DCH DCL
SHEET 4 VPF
TP31
TP32
P10
VDDR
VDD
VSS
J2
VEE
VCC
5VAC
TP5
TP6
FIL1
FIL2
VLOAD
VEE
VR2 1N5233
C4 1.0 50V
C6 10 63V
RCOM SHLD
C5 1.0 50V
VR1 1N5232
CR4 BAS16
Q4 MMBT3904
C9 180PF
Q2 MMBT3906
Q1 MMBT3906
R13 20
R11 47K
R9 4.7K
U6 LM317T IN OUT ADJ
R5 1.00K 1%
R6 3.32K 1%
TP30
R14 10K
Q3 MMBT3906
R4 10K
R10 4.7K
R12 47K
Q6 MMBT3904
Q5 MMBT3904
C10 180PF
R15 33
CR6 MBR140
CR5 MBR140
C12 470 16V
C13 470 16V
CR7 BAW56
T1
C17 2.2 50V
VR3 1N5235B
R22 47K
TP4
TP3
C32 1.0 50V
CR9 MMBD7000
CR8 MMBD7000
U18 LM79L05A IN OUT GND
C31 47 50V R1
C30 47 50V R1
CR13 MMBD7000
NOTE: U22 AND U23 ARE BIASED BY IBIAS
IBIAS
U23
R47 10K
C35 1000PF
R40 5.1K
Q8 IRL024
Q7 IRL024
TP9
TP10
R34 470
CR12 BAS16
R28 470
CR11 BAS16
R38 0.02 1/4W
U22 HC74 D PR Q CL
TP14
TP7
RT1 RXE065
C59 180PF
R19 11.0K 1%
R20 59.0K 1%
CR1 MBR0360
U19 LM317L IN OUT ADJ
R44 1.30K 1%
C34 1.0 50V
R46 4.02K 1%
S1 OFF
C7 10000 35V
C1 220 35V
CR3 1N5397
C2 .033 100V
CR2 1N5397
J3
2620A-6501
R48 10K 1/4W
C39 .047 100V
MH1
1/8A SB
L N FG
T2 FLUKE 45-6401
C26 47 50V
CR10 MBR0360
VCC
C14 2200 10V
TP2
TP1
U28 LM358DT
R31 11.0K 1%
R30 45.3K 1%
R26 100
C21 0.1 25V
C18 220 35V
U9 LT1170 VIN VSW FB VC GND

Figure F.

CHANGE #5- 51582

Rev. -E, A1 2620A/2625A Main PCA (2620A-4001)

On pages 6-17 and 6-18, Table 6-3, make the following changes:

CHANGE: AR1/IC,OP AMP,DUAL,LOW POWER,SOIC/867932/6E570/LM358D/1
TO: AR1,U31/IC,OP AMP,DUAL,LOW POWER,SOIC/867932/6E570/LM358D/2

CHANGE: C1,3,8,11,19,22-25.../CAP,CER,0.1UF,.../747287/04222/12065C104KATBA/19
TO: C1,3,8,11,19,21,22-25.../CAP,CER,0.1UF,.../747287/04222/12065C104KATBA/**20**

CHANGE: C15,16,18/CAP,CER,33PF,.../769240/04222/12065A330KATBA/3
TO: C15,16/CAP,CER,33PF,.../769240/04222/12065A330KATBA/2

CHANGE: C20/CAP,CER,1800PF,+-10%,50V,C0G,1206/769786/04222/12065A182KATBA/1
TO: C18,20/CAP,CER,220UF,+-10%,50V,C0G,1206/929708/89536/929708/2

CHANGE: CR1,10/DIODE,SI,100 PIV,3.3 AMPS,SCHOTTKY/837740/59993/30WQ10F/2
TO: CR1,10/DIODE,SI,100 PIV,3.3 AMPS,SCHOTTKY/943097/89536/943097/2

CHANGE: R23/RES,CF,220K,+-5%,0.25W/851837/59124/CF1/4 224J/1
TO: R31/RES,CF,11K,+-5%,0.25W/928796/89536/928796/1

CHANGE: R26/RES,CERM,10.5K,+-1%,.125W,100PPM,1206/851852/91637/CRCW1206-1052FB/1
TO: R26/RES,CERM,47K,+-1%,.125W,100PPM,1206/746297/89536/746297/1

CHANGE: R29-31/RES,CF,0.50,+-5%,0.25W/830646/59124/CF1/4 R50J/3
TO: R30/RES,CF,3K,+-5%,0.25W/930201/89536/930201/1

CHANGE: U9/IC,VOLT REG,ADJ,SWITCHING REGULATOR/867135/27014/LM2579T/1
TO: U9/IC,VOLT REG,ADJ,SWITCHING REGULATOR/929591/89536/929591/1

DELETE: C21/CAP,CER,820PF,+-5%,50V,C0G,1206/867403/04222/12065A821JATBA/1

DELETE: R17/RES,CF,1M,+-5%,0.25W/649970/59124/CF1/4 105J/1

DELETE: R18/RES,CERM,10M,+-5%,.125W,300PPM,1206/783274/91637/CRCW4519-1005JB02/1

DELETE: R24/RES,CERM,64.9K,+-1%,.125W,100PPM,1206/876086/91637/CRCW1206-6492FB/1

DELETE: R27/RES,CERM,220K,+-5%,0.125W,200PPM,1206/746750/91637/CRCW1206-2203JB02/1

DELETE: R32,33/RES,CF,1,+-5%,0.25W/867866/59124/CF1/4 1R0J/2

On pages 6-20 and 8-5 through 8-9, replace Figures 6-3 and 8-1 (2620-1601) with Figure G.

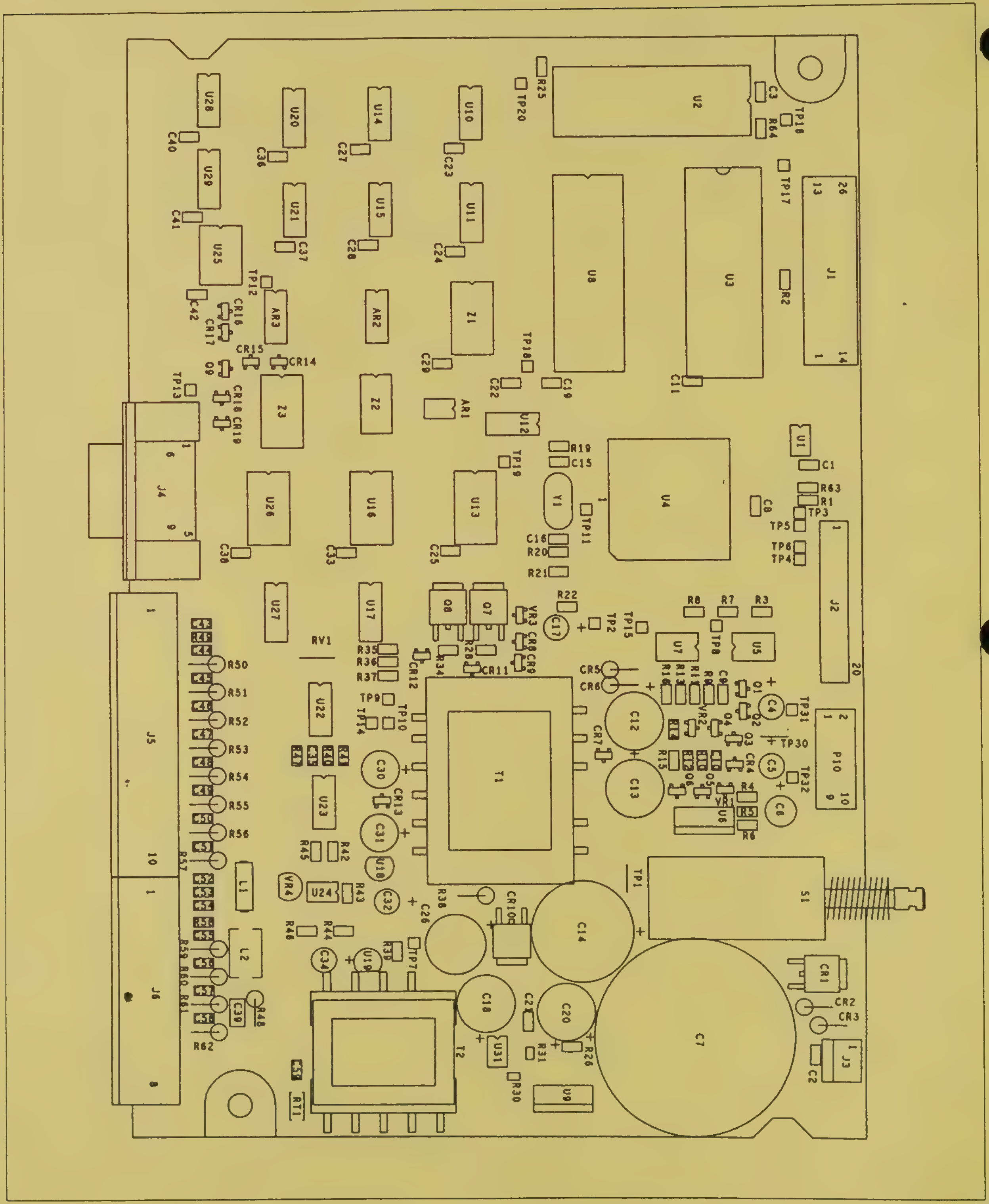

U28
C40
U29
C41
U25
C42
CR16
CR17
TP12
U20
C36
U21
C37
AR3
CR15
CR14
Q9
TP13
CR18
CR19
Z3
U14
C27
U15
C28
AR2
Z2
U10
C23
U11
C24
Z1
C29
AR1
TP20
R25
TP18
C22
C19
U12
U2
C3
TP16
R64
TP17
U8
U3
R2
J1
26
13
1
14
C11
U1
C1
R63
R1
TP3
TP5
TP6
TP4
J2
20
R19
C15
TP19
Y1
TP11
U4
C8
C16
R20
R21
J4
6
9
5
U26
C38
U16
C33
U13
C25
U27
U17
Q8
Q7
VR3
CR8
CR9
C17
R22
TP2
TP15
R8
R7
R3
U7
TP8
U5
RV1
R35
R36
R37
R34
R28
CR12
CR11
CR5
CR6
R16
R13
R9
C9
Q1
C4
TP31
J5
R50
R51
R52
R53
R54
R55
R56
R57
10
U22
TP9
TP10
TP14
C30
CR13
C31
U23
R45
R42
T1
CR7
C12
VR2
Q4
Q2
Q3
R15
CR4
C5
Q6
Q5
TP30
P10
2
9
TP32
R4
VR1
U6
R5
R6
C6
C13
L1
VR4
U24
R43
U18
C32
R38
C26
CR10
TP1
S1
C14
R46
R44
L2
C34
U19
R39
TP7
J6
R59 R60 R61
C39
R48
R62
8
T2
C18
C21
C20
U31
R31
R26
C7
CR1
CR2
CR3
J3
C2
R30
U9
RT1
C59

Figure G.

On page 8-6, replace the first sheet of Figure 8-1 (2620A-1001) with Figure H.

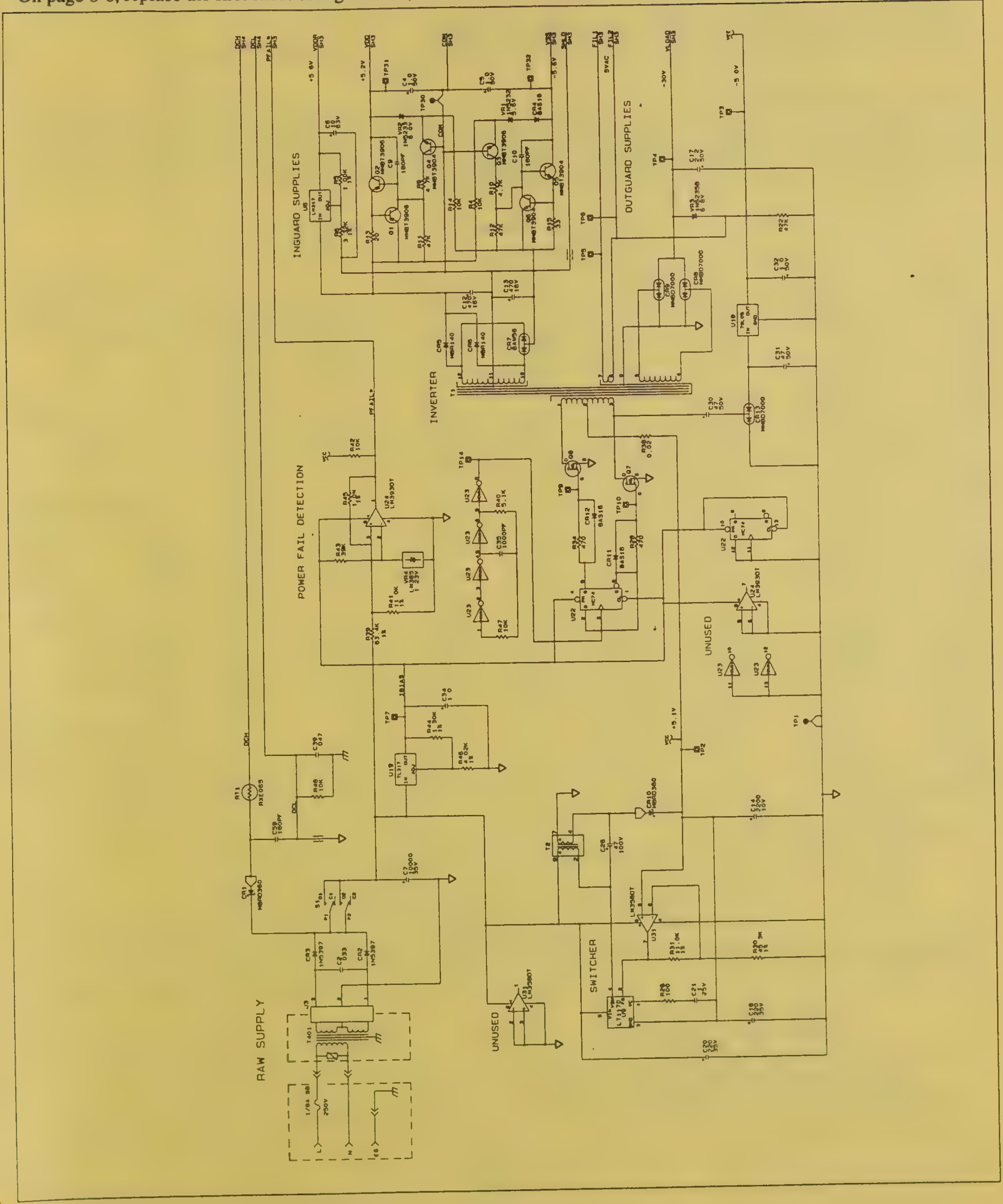

INGUARD SUPPLIES
OUTGUARD SUPPLIES
INVERTER
POWER FAIL DETECTION
UNUSED
RAW SUPPLY
UNUSED
SWITCHER

Figure H.

CHANGE #6- 52048, 52398

Rev. -G & H, A3 A/D Converter PCA (2620A-4003)

On page 1-15 and 1-29, Table 1-3 and 1-4, replace the TYPICAL SCANNING RATE table with:

TYPICAL SCANNING RATE

See the table below. The measurement conditions are: averaged rate over 20 scans; continuous scanning; alarm limits and Mx+B scanning set on all channels; logging data to memory card (for the 2635A) or internal memory (for 2620A and 2625A); and RS-232 communications set at 9600 baud. Measurements were taken with short-circuit inputs on all channels, except frequency, which was taken with 5V at 15 Hz on all channels.

		SLOW			FAST		
	Channels:	**1**	**10**	**20**	**1**	**10**	**20**
Function	**Range**						
VDC	300 mV	1.7	3.6	3.8	2.2	10.3	12.9
VDC	3V	1.7	3.6	3.8	2.2	10.3	12.9
VDC	30V	1.7	3.6	3.8	2.2	10.3	12.9
VDC	150/300V	1.7	3.5	3.8	2.2	10.2	12.8
VDC	AUTO	1.7	3.4	3.6	2.2	8.9	10.7
Temperature	J	1.0	3.1	3.5	1.9	9.5	12.1
Temperature	PT	1.5	2.5	2.6	1.7	4.2	4.5
VAC	300 mV	1.0	1.5	1.5	1.3	2.3	2.4
VAC	3V	1.0	1.5	1.5	1.3	2.3	2.4
VAC	30V	1.0	1.5	1.5	1.3	2.3	2.4
VAC	150/300V	1.0	1.5	1.5	1.3	2.3	2.4
VAC	AUTO	1.0	1.4	1.5	1.3	2.3	2.4
Ohms	300Ω	1.5	2.5	2.6	1.8	4.2	4.5
Ohms	3 kΩ	1.5	2.5	2.6	1.7	4.2	4.5
Ohms	30 kΩ	1.5	2.5	2.6	1.7	4.2	4.5
Ohms	300 kΩ	1.0	1.5	1.5	1.4	2.8	2.9
Ohms	3 MΩ	1.0	1.5	1.5	1.4	2.7	2.9
Ohms	10 MΩ	1.0	1.5	1.5	1.4	2.7	2.9
Ohms	AUTO	1.5	2.5	2.6	1.7	4.2	4.5
Frequency	any	0.5	0.6	0.7	0.6	0.7	0.7

On pages 6-27 and 6-28, Table 6-6,

ADD:	R45, 46/RES,MF,10K,5%, 200PPM,0.1W/601432/89536/601432/2
CHANGE:	U9/2620A PROGRAMMED MICROPROCESSOR/886986/62786/886986/1
TO:	U9/IC,CMOS,**MCU,8BIT,1 MHZ,PROGRMD,PLCC68/601317/89536/601317/1**

On pages 6-29 and 8-23 through 8-27, Figures 6-6 and 8-4 (2620A-1603), add R45, 46 as shown in Figure I.

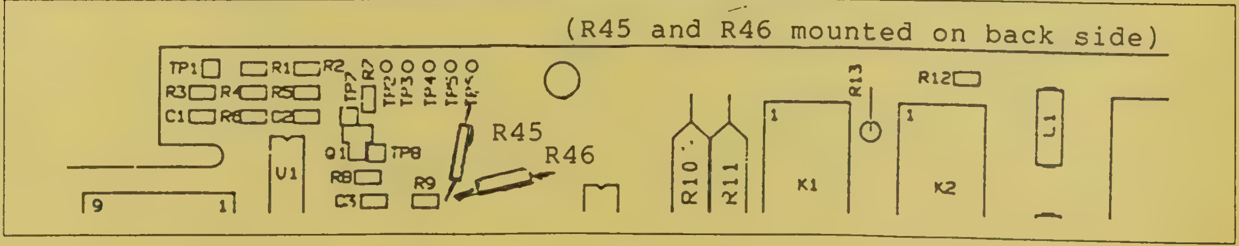


Figure I.

On page 8-27/28, Figure 8-4 (2620A-1003), add R45 amd R46 as shown in Figure J.

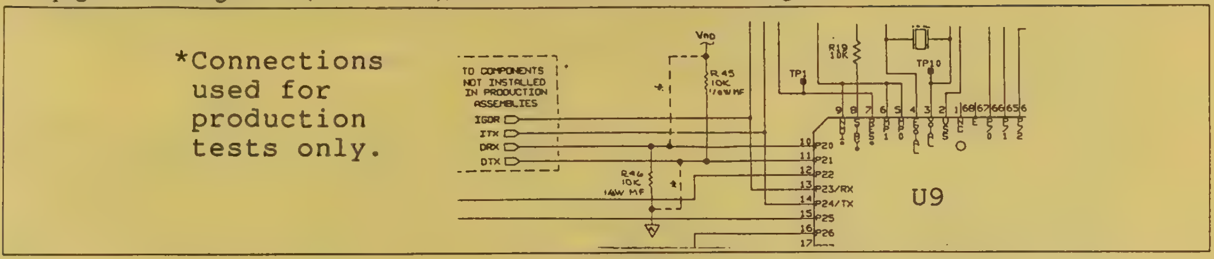


Figure J.

CHANGE #7

On pages 1-11 and 1-25, under **2-Wire Accuracy,**

CHANGE:	...accuracy an additional 4° for channels 1 to 20...
TO:	...accuracy an additional **11°** for channels 1 to 20...

On pages 1-14 and 1-28, under **2-Wire Accuracy,**

CHANGE:	Add 1.5Ω to accuracy specifications for channels 1 to 20...
TO:	Add 4.0Ω to accuracy specifications for channels 1 to 20...

CHANGE #8

On page 4-12, Table 4-5, change the headings under the Simulated Degree C Temperature

FROM:	**before M5.6***	and	**after M5.5***
TO:	**2620A/2625A***	and	**2635A***

Replace the first footnote with:

* RTD temperature linearizations changed between the 2620A/2625A and 2635A Hydra Instrument firmware. The 2620A and 2625A Hydra Instruments are based on the International Practical Temperature Scale of 1968 (IPTS-68). The 2635A Hydra Instrument is based on the International Temperature Scale of 1990 (ITS-90).

CHANGE #9

On page 2-8, change the 2-27 heading and add a paragraph to the section as follows:

5V Switcher (Revision D1 and below main boards) 2-27A.

There are two versions of the 5V switcher circuitry used in the 2620A/2625A instruments. Earlier versions (main board revision D1 and below) use the LM2579 as the A1U9 switching regulator IC. Newer versions (main board revision E and above) use the LT1170 as the A1U9 switching regulator.

On page 2-9, add:

5V Switcher (Revision E and higher main boards) 2-27B.

The 5V switcher supply uses a switcher supply controller/switch device A1U9 and related circuitry. The 7.5V dc to35V dc input is regulated to 5.1V dc (VCC) through pulse-width modulation at a nominal switching frequency of 100 kHz.

The output voltage of the switcher supply is controlled by varying the duty cycle (ON time) of the switching transistor in the controller/switch device A1U9. A1U9 contains the supply reference, oscillator, switch transistor, pulse-width modulator comparator, switch drive circuit, current-limit comparator, current-limit reference, and thermal limit. Dual inductor A1T2 regulates the current that flows from the raw supply to the load as the switching transistor in A1U9 is turned on and off. Complementary switch A1CR10 conducts when the switching transistor is off.

The pulse-width modulator comparator in A1U9 compares the output to the reference and sets the ON-time/OFF-time ratio to regulate the output to 5.1V dc. A1C26 is the input filter capacitor, and A1C14 is the output filter capacitor. Proper inductor and capacitor values set the filter frequency response to ensure best overall system stability. Circuitry consisting of A1R26, A1C21, and A1C18 ensure that the switcher supply remains stable and operating in the continuous mode. Resistors A1R30 and A1R31 set the output voltage to within 5% of 5.1V. Capacitor A1C21 sets the operating frequency of the switcher at approximately 100 kHz.

Resistors A1R30 and A1R31 form a voltage divider that operates in conjunction with amplifier A1U31, which is configured as a voltage follower. A1U31-5 samples the 5.1V dc output, while A1U31-6 is the voltage divider input. The effect is to maintain the junction of R30 and R31 at 5.1V dc, resulting in an A1U31-7 output level of 6.34V dc, or 1.24V dc above the output. This feedback voltage is applied to A1U9-2, which A1U9 interprets as 1.24V dc because A1U9-3 (ground) is connected to the 5.1V dc output.

On page 2A-8, change the 2A-26 heading and add a paragraph to the section as follows:

5V Switcher (Revision A3 and below main boards) 2A-26A.

There are two versions of the 5V switcher circuitry used in the 2635A instruments. Earlier versions (main board revision A3 and below) use the LM2579 as the A1U9 switching regulator IC. Newer versions (main board revision B and above) use the LT1170 as the A1U9 switching regulator.

On page 2A-9, add:

5V Switcher (Revision B and above main boards) 2A-26B.

The 5V switcher supply uses a switcher supply controller/switch device A1U9 and related circuitry. The 7.5V dc to 35V dc input is regulated to 5.1V dc (VCC) through pulse-width modulation at a nominal switching frequency of 100 kHz.

The output voltage of the switcher supply is controlled by varying the duty cycle (ON time) of the switching transistor in the controller/switch device A1U9. A1U9 contains the supply reference, oscillator, switch transistor, pulse-width modulator comparator, switch drive circuit, current-limit comparator, current-limit reference, and thermal limit. Dual inductor A1T2 regulates the current that flows from the raw supply to the load as the switching transistor in A1U9 is turned on and off. Complementary switch A1CR10 conducts when the switching transistor is off.

The pulse-width modulator comparator in A1U9 compares the output to the reference and sets the ON-time/OFF-time ratio to regulate the output to 5.1V dc. A1C26 is the input filter capacitor, and A1C14 is the output filter capacitor. Proper inductor and capacitor values set the filter frequency response to ensure best overall system stability. Circuitry consisting of A1R26, A1C21, and A1C18 ensure that the switcher supply remains stable and operating in the continuous mode. Resistors A1R30 and A1R31 set the output voltage to within 5% of 5.1V. Capacitor A1C21 sets the operating frequency of the switcher at approximately 100 kHz.

Resistors A1R30 and A1R31 form a voltage divider that operates in conjunction with amplifier A1U28, which is configured as a voltage follower. A1U28-5 samples the 5.1V dc output, while A1U28-6 is the voltage divider input. The effect is to maintain the junction of R30 and R31 at 5.1V dc, resulting in an A1U28-7 output level of 6.34V dc, or 1.24V dc above the output. This feedback voltage is applied to A1U9-2, which A1U9 interprets as 1.24V dc because A1U9-3 (ground) is connected to the 5.1V dc output.

A1U9 maintains the feedback and reference voltages at 1.24V dc and thus regulates the 5.1V dc source.

On page 5-7, replace Figure 5-1. with:

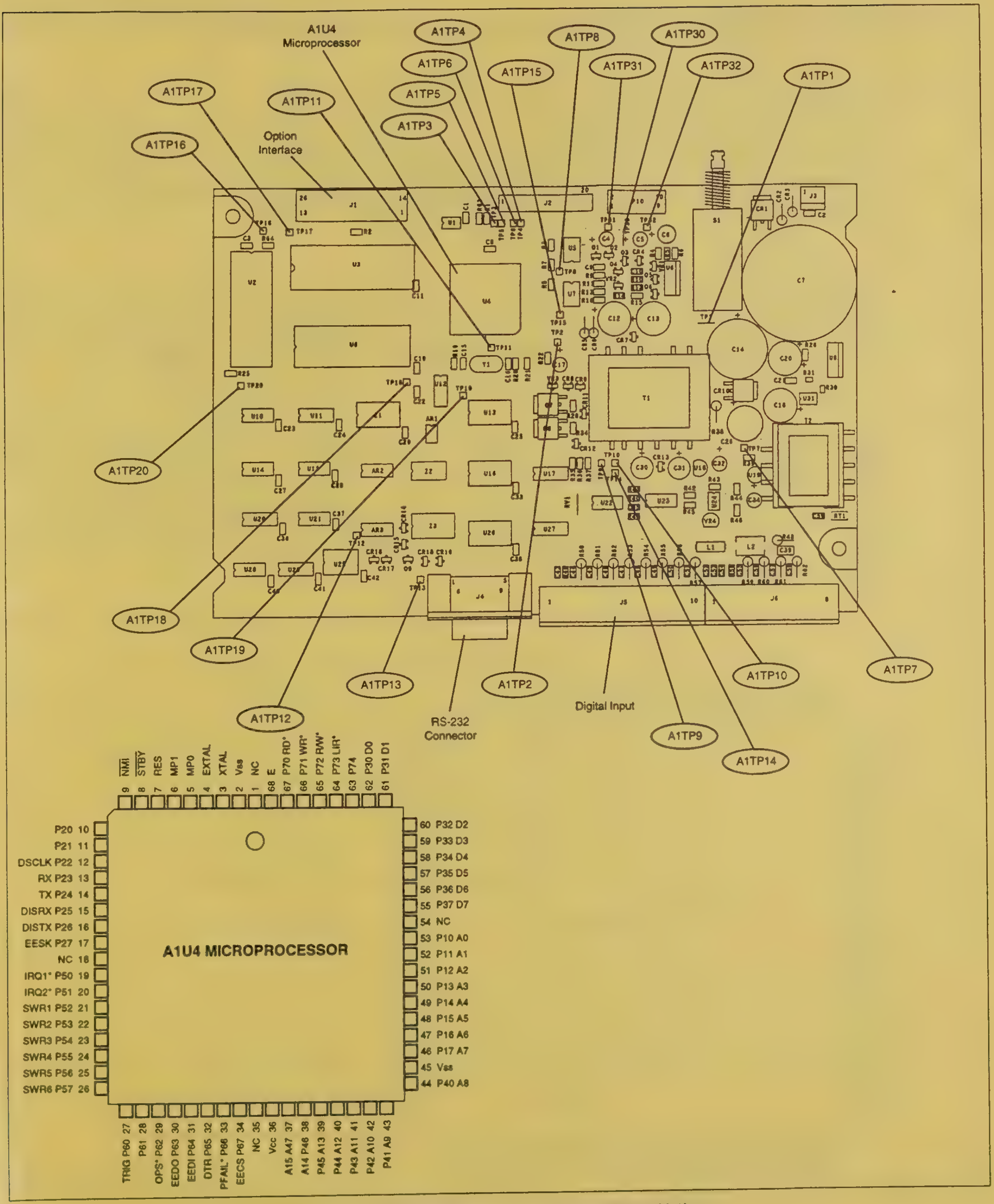

A1U4 Microprocessor
Option Interface
A1TP4
A1TP8
A1TP30
A1TP6
A1TP15
A1TP31
A1TP32
A1TP1
A1TP5
A1TP17
A1TP11
A1TP3
A1TP16
A1TP20
A1TP18
A1TP19
A1TP13
A1TP2
A1TP10
A1TP7
A1TP12
RS-232 Connector
Digital Input
A1TP9
A1TP14
A1U4 MICROPROCESSOR
9 NMI
8 STBY
7 RES
6 MP1
5 MP0
4 EXTAL
3 XTAL
2 Vss
1 NC
68 E
67 P70 RD*
66 P71 WR*
65 P72 R/W*
64 P73 LIR*
63 P74
62 P30 D0
61 P31 D1
P20 10
P21 11
DSCLK P22 12
RX P23 13
TX P24 14
DISRX P25 15
DISTX P26 16
EESK P27 17
NC 18
IRQ1* P50 19
IRQ2* P51 20
SWR1 P52 21
SWR2 P53 22
SWR3 P54 23
SWR4 P55 24
SWR5 P56 25
SWR6 P57 26
60 P32 D2
59 P33 D3
58 P34 D4
57 P35 D5
56 P36 D6
55 P37 D7
54 NC
53 P10 A0
52 P11 A1
51 P12 A2
50 P13 A3
49 P14 A4
48 P15 A5
47 P16 A6
46 P17 A7
45 Vss
44 P40 A8
TRIG P60 27
P61 28
OPS* P62 29
EEDO P63 30
EEDI P64 31
DTR P65 32
PFAIL* P66 33
EECS P67 34
NC 35
Vcc 36
A15 A47 37
A14 P46 38
P45 A13 39
P44 A12 40
P43 A11 41
P42 A10 42
P41 A9 43

Figure 5-1. Test Point Locator, Main PCA (A1)

On page 5-8, step 5-8, change the 5-8 heading to:

5-Volt Switching Supply (Revision D1 and below main boards) 5-8A.

On page 5-10, prior to section 5-9, add:

5V Switching Supply (Revision E and above main boards) 5-8B.

Use an oscilloscope to troubleshoot the 5-volt switching supply. With the oscilloscope common connected to A1TP1, check the waveform at either A1U9, pin 4 or A1T1, pin 2 to determine the loading on the 5-volt switching supply. The output voltage of the 5-volt switching supply at A1TP2 (VCC) is normally about 5.1V dc with respect to A1TP1 (GND). Note that a fault in the load (high or low resistance) can appear as a faulty output voltage of the 5-volt switching supply.

- Normal Load:

The signal at A1U9-4 (with respect to A1TP1) is a square wave with a period of 9 us to 11 us and an ON (voltage is low) duty ratio of about 0.38 with the line voltage at 120V ac. The amplitude is usually about 15V p-p. The positive-going edge will be "fuzzy" as the duty ratio is varying to compensate for the ripple of the raw supply and the pulsing load of the inverter supply. See Figure 5-2A (NORMAL LOAD).

- Very Heavy Load:

Under heavy load (example: A3 A/D Converter PCA has a short circuit) it could load down the power supply voltage such that the current limiting feature is folding the supply back. For example, if the supply is folded back due to excessive current draw, unplug the ribbon cable at A3J10 on the A/D Converter PCA. When tracking down power supply loads, use a sensitive voltmeter and look for resistive drops across filter chokes, low value decoupling resistors, and circuit traces. Also check for devices that are too warm. On the A3 A/D Converter PCA, all devices run cool except A3U5 microprocessor and A3U8 FPGA, which run warm, but not hot.

ADD:

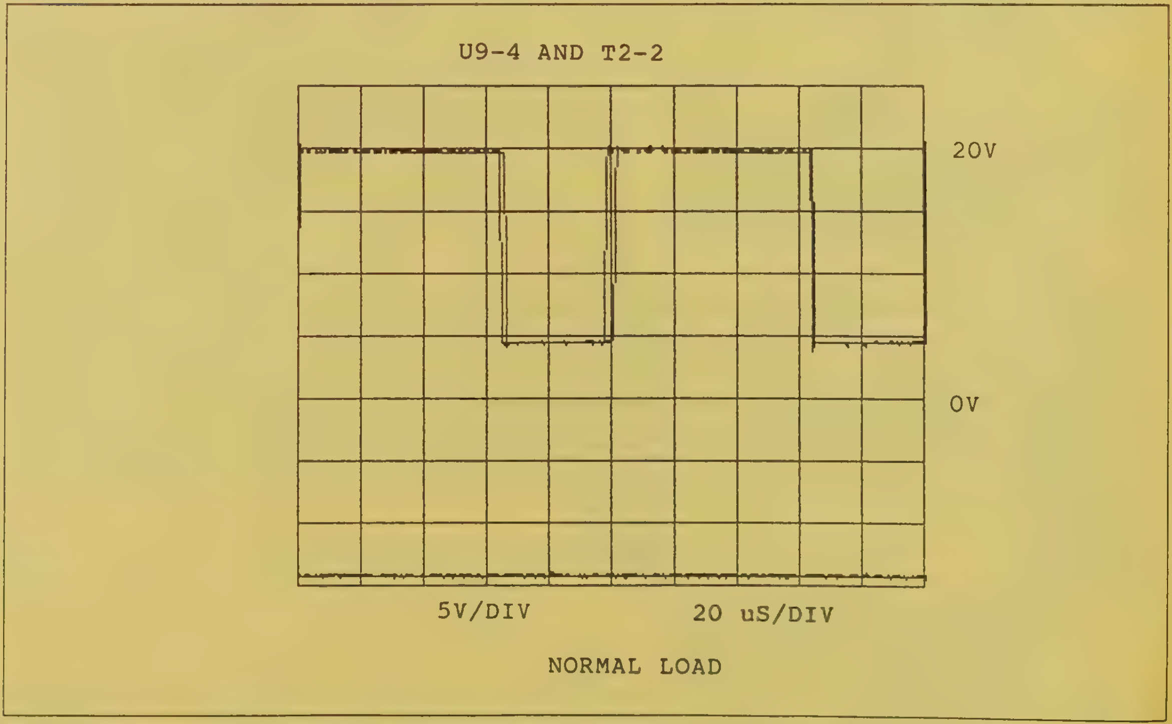


Figure 5-2A. 5-Volt Switching Supply (Revision E Main PCA)

On page 5A-7, replace Figure 5A-1.

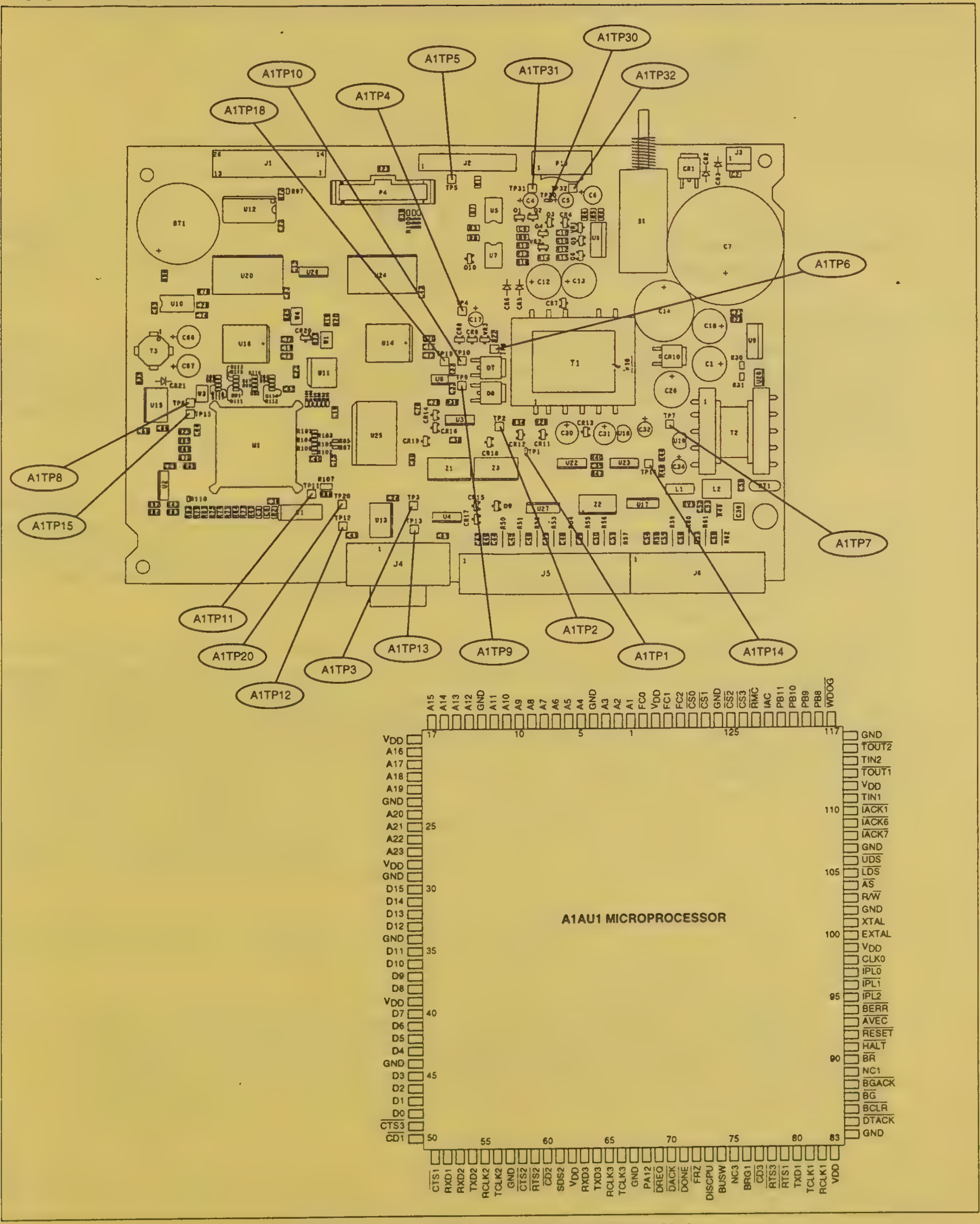

A1TP30
A1TP5
A1TP31
A1TP32
A1TP10
A1TP4
A1TP18
A1TP6
A1TP8
A1TP15
A1TP7
A1TP11
A1TP20
A1TP12
A1TP3
A1TP13
A1TP9
A1TP2
A1TP1
A1TP14
J1
J2
J3
J4
J5
J6
P4
T1
T2
C7
S1
BT1
U1
U12
U20
U24
U25
A1AU1 MICROPROCESSOR
A15
A14
A13
A12
GND
A11
A10
A9
A8
A7
A6
A5
A4
GND
A3
A2
A1
FC0
VDD
FC1
FC2
CS0
CS1
GND
CS2
CS3
RMC
IAC
PB11
PB10
PB9
PB8
WDOG
17
10
5
1
125
117
VDD
A16
A17
A18
A19
GND
A20
A21
A22
A23
VDD
GND
D15
D14
D13
D12
GND
D11
D10
D9
D8
VDD
D7
D6
D5
D4
GND
D3
D2
D1
D0
CTS3
CD1
25
30
35
40
45
50
GND
TOUT2
TIN2
TOUT1
VDD
TIN1
IACK1
IACK6
IACK7
GND
UDS
LDS
AS
R/W
GND
XTAL
EXTAL
VDD
CLKO
IPL0
IPL1
IPL2
BERR
AVEC
RESET
HALT
BR
NC1
BGACK
BG
BCLR
DTACK
GND
110
105
100
95
90
83
55
60
65
70
75
80
CTS1
RXD1
RXD2
TXD2
RCLK2
TCLK2
GND
CTS2
RTS2
CD2
SDS2
VDD
RXD3
TXD3
RCLK3
TCLK3
GND
PA12
DREQ
DACK
DONE
FRZ
DISCPU
BUSW
NC3
BRG1
CD3
RTS3
RTS1
TXD1
TCLK1
RCLK1
VDD

Figure 5A-1. Test Point Locator, Main PCA (A1)

On page 5A-8, Table 5A-2, replace the **PREREGULATED VOLTAGE** column and make the following changes:

PREREGULATED VOLTAGE
-8.9V
-30.9V
+9.2V
-8.6V

CHANGE: ***5-Volt Switching Supply*** ***5A-8.***
TO: ***5-Volt Switching Supply (Revision A3 and below main boards)*** ***5A-8A.***

On page 5A-9, prior to section 5A-9, add:

5V Switching Supply (Revision B and above main boards) *5A-8B.*

Use an oscilloscope to troubleshoot the 5-volt switching supply. With the oscilloscope common connected to A1TP1, check the waveform at either A1U9, pin 4 or A1T1, pin 2 to determine the loading on the 5-volt switching supply. The output voltage of the 5-volt switching supply at A1TP2 (VCC) is normally about 5.0V dc with respect to A1TP1 (GND).

- Normal Load:

The signal at A1U9-4 (with respect to A1TP1) is a square wave with a period of 9 us to 11 us and an ON (voltage is low) duty ratio of about 0.38 with the line voltage at 120V ac. The amplitude is usually about 15V p-p. The positive-going edge will be "fuzzy" as the duty ratio is varying to compensate for the ripple of the raw supply and the pulsing load of the inverter supply. See Figure 5A-2A (NORMAL LOAD).

- Very Heavy Load:

Under heavy load (example: A3 A/D Converter PCA has a short circuit) it could load down the power supply voltage such that the current limiting feature is folding the supply back. For example, if the supply is folded back due to excessive current draw, unplug the ribbon cable at A3J10 on the A/D Converter PCA. When tracking down power supply loads, use a sensitive voltmeter and look for resistive drops across filter chokes, low value decoupling resistors, and circuit traces. Also check for devices that are too warm. On the A3 A/D Converter PCA, all devices run cool except A3U5 microprocessor and A3U8 FPGA, which run warm, but not hot.

ADD:

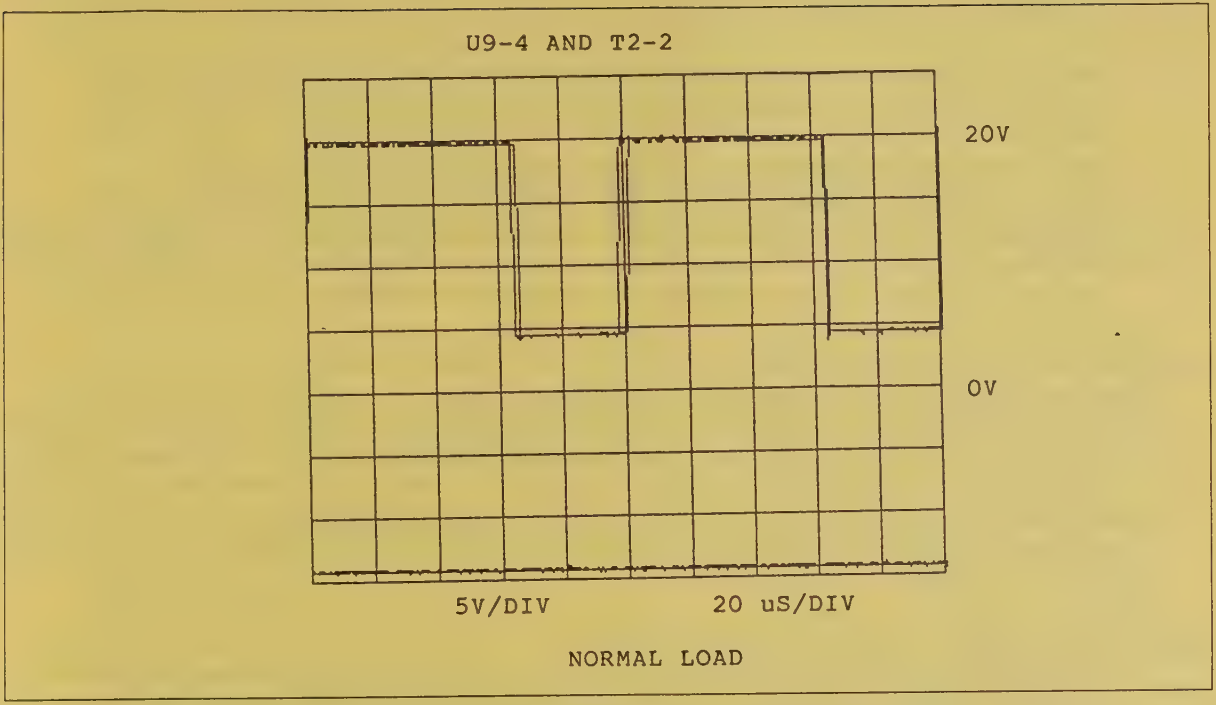


Figure 5A-2A. 5-Volt Switching Supply (Revision B Main PCA)

Change #10

On page 6-30, Table 6-7, add the following note to the bottom of the table:

Refer to Table 6-1 for ordering information on the Case Top, Case Bottom, and decal.

Change #11 - 52529

Rev.B, A6 Memory Card Interface PCA (2635A-4006)

On page 2A-37, make the following changes:

Change the 2A-70 heading and add a note as follows:

2A-70. Memory Card Interface PCA (Revision A2 and below)

Note

There are two versions of the Memory Card Interface PCA used in the 2635A Hydra Data Bucket instrument. Earlier versions (Rev.A2 and below) are designed using a Fujitsu MF86301PF memory card controller IC (A6U1). Newer versions (Rev.B and higher) are designed using a Xilinx XC3030A-7PQ100C gate array as the memory card controller (A6U1). This section covers the Rev.A2 and below. See section 2A-75 for theory on Rev.B and higher.

On page 2A-39, add the following:

2A-75. Memory Card Interface PCA (Revision B and higher)

Note

There are two versions of the Memory Card Interface PCA used in the 2635A Hydra Data Bucket instrument. Earlier versions (Rev.A2 and below) are designed using a Fujitsu MF86301PF memory card controller IC (A6U1). Newer versions (Rev.B and higher) are designed using a Xilinx XC3030A-7PQ100C gate array as the memory card controller (A6U1). This section covers the Rev.B and higher. See section 2A-70 for Rev.A2 and below.

The Memory Card Interface Assembly operation is composed of four functional circuit blocks: the Main PCA Connector, the Microprocessor Interface, the Memory Card Controller, and the PCMCIA Memory Card Connector. These blocks are described in the following paragraphs.

2A-76. MAIN PCA CONNECTOR

The Memory Card Interface PCA interfaces to the Main PCA through a 40-pin, right angle connector (A6P2). This connector routes eight bits of the Microprocessor data bus, the lower four bits of the address bus, memory control, interrupt and address decode signals from the Main PCA to the Memory Card Interface PCA. The Memory Card Interface PCA is powered by the +5.0V dc power supply (VCC). The pinout of the high density ribbon cable that connects the Main PCA to the Memory Card Interface PCA is carefully selected to prevent cross-talk between signals and to provide low impedance connections to the VCC power supply.

2A-77. MICROPROCESSOR INTERFACE

The timing of Microprocessor read and write accesses to the Memory Card Controller (A6U1) are controlled internally by the Memory Card Controller which determines whether wait states are required when the Microprocessor accesses one of its internal registers.

When a register in the Memory Card Controller (A6U1) is read, the four address bits select one of the internal registers to read and then the XMCARD* signal (A6U1-49) is driven to a low level by the Microprocessor. The XRDU* signal (A6U1-50) is then driven low by A1U11-14 to enable the data outputs from the Memory Card Controller (D8 through D15). At the end of the read access, both XMCARD* and XRDU* are driven high again.

When a register in the Memory Card Controller (A6U1) is written, the four address bits select one of the internal registers to write and then the XMCARD* signal (A6U1-49) is driven to a low level by the Microprocessor. The XWRU* signal (A6U1-51) is then driven low by A1U11-13 to initiate the transfer of the data bus inputs on the Memory Card Controller (D8 through D15) to the internal register. At the end of the write access, both XMCARD* and XRDU* are driven high again and the data is latched into the internal register.

If no wait states are required, the DTACK* signal (A6U1-58) will be driven low after the next low to high transition of the system clock (A6U1-30) to indicate to the Microprocessor that the data transfer has been acknowledged and the read or write access may be completed. The DTACK* signal is a tri-state bus that is pulled up to VCC by resistor A1R83 and pulled low by devices being accessed by the Microprocessor.

If wait states are required, the DTACK* signal (A6U1-58) will not go low until the proper number of wait states have been inserted. The Memory Card Controller counts cycles of the system clock (A6U1-30) and when the correct number of wait states have been done, the DTACK* signal will go low.

Accesses to internal registers should be done with no wait states, and accesses through the Memory Card Controller to the Memory Card automatically add two wait states.

2A-78. MEMORY CARD CONTROLLER

The Memory Card Controller (A6U1) is a Field Programmable Gate Array (FPGA) that automatically loads its configuration upon power-up from a serial memory device (A6U3). While it is configuring, the FPGA holds the memory CE input (A6U3-4) low and toggles the CLK input (A6U3-2) to serially shift the configuration data out of the memory on the D output (A6U3-1) and into the FPGA. When configuration is complete, the FPGA should release the CE input(A6U3-4) allowing it to be pulled high by resistor A6R8.

The Memory Card Controller provides a register based interface for the Microprocessor to use to access data stored on industry standard PCMCIA memory cards. A 26 bit counter controls the address bus (CA<0> through CA<25>) to the PCMCIA Memory Card Connector (A6P1). An eight bit data bus(CD<0> through CD<7>) and memory card control signals (REG*, CE1*, CRD*, and CWR*) control accesses to memory on the card.

The REG* signal (A6U1-8) is like an additional address bit. When REG* is slow (A6U1-8), read and write accesses go to "attribute" memory on the card. Attribute memory is typically a small EEPROM on the memory card that contains special information that specifies the manufacturer of the card, type and size of memory on the card, memory speed, etc. When REG* is high, read and write accesses go to the "common" memory on the card. Common memory is the Static RAM on the memory cards used in this instrument.

Typically, information is read and written to the memory card in a sequential manner where the address counter automatically increments after the end of each read or write cycle. When the Memory Card Controller reads data from the memory card data bus (CD<0> through CD<7>), CE1* (A6U1-62) goes low followed by CRD* (A6U1-63) going low. The data from the memory card then goes through the Memory Card controller and is read by the Microprocessor on the D8 through D15 data bus lines. Data is written to the memory card in a similar manner, except that the data goes from the Microprocessor through the memory Card Controller and to the Memory Card with CWR* (A6U2-64) going low to enable the writing of the data to the memory. The purpose of A6U2 and resistors A6R2, A6R5, and A6R7 is to ensure that data on the Memory Card is not accidentally modified during the time that the instrument is being powered up or down. Each of the Memory Card data bus lines (CD<0> through CD<7>) has a series resistor (A6Z2) that helps ensure that the instrument meets EMI/EMC performance requirements.

The Memory Card Controller detects the insertion and removal of a Memory Card and interrupts the microprocessor by driving the MCINT* signal(A6U1-60) low. When a Memory Card is inserted in the PCMCIA Memory Card Connector, the CD1 (A6U1-19) and CD2 (A6U1-21) inputs on the Memory Card Controller are driven to 0V dc and Microprocessor (A1U1) is interrupted. The Microprocessor then powers up the Memory Card by setting A6U1-26 low, which turns on FET A6Q1 by driving the gate low through resistor A6R13. When FET A6Q1 is turned on the Memory Card power (CVCC and CVPP) is approximately +5.0V dc. When the Microprocessor has completed a data transfer with the Memory Card, FET A6Q1 is turned off again by driving A6U1-26 high.

When a Memory Card is inserted and powered up, the Memory Card outputs some status signals to the Memory Card Controller. If the Memory Card write protect switch is protecting data on the card, the WP signal (A6U1-22) is high. The status of the Memory Card battery is output on the BVD1 (A6P1-18) and BVD2 (A6P1-20) pins of the Memory Card Connector. If either of these battery status signals is low when the Memory Card is powered up, then the Microprocessor will turn on LED A6DS2 by driving A6U1-24 low. The Busy status LED (A6DS1) is turned on by driving A6U1-25 low when the Microprocessor has powered up the Memory Card and is transferring data to or from the card.

2A-79. PCMCIA MEMORY CARD CONNECTOR

The PCMCIA Memory Card Connector (A6P1) is a 68 pin connector that meets the requirements of the Personal Computer Memory Card International Association. This connector has pins that are three different lengths: the card detection pins (CD1 and CD2) are the shortest, the power and ground pins are the longest, and the rest of the pins are a length in between. This ensures that on memory card insertion, the power and ground pins are mated first followed by the reset of the input / output signals with the card detection signals mating last. This sequence is reversed on memory card removal.

The PCMCIA Memory Card Connector has a metal shell that is connected to chassis ground to help ensure that the instrument meets EMI/EMC and ESD performance requirements. A push-button mechanism is included to allow easy ejection of the Memory Card.

On page 5A-31, change the 5A-25 heading and add a note as follows:

5A-26. MEMORY CARD INTERFACE ASSEMBLY (A6) TROUBLESHOOTING (Revision A2 and below)

Note

There are two versions of the Memory Card Interface PCA used in the 2635A Hydra Data Bucket instrument. Earlier versions (Rev.A2 and below) are designed using a Fujitsu MF86301PF memory card controller IC (A6U1). Newer versions (Rev.B and higher) are designed using a Xilinx XC3030A-7PQ100C gate array as the memory card controller (A6U1). This section covers Rev.A2 and below. See section 5A-33 for troubleshooting information on Rev.B and higher.

On page 52A-32, at the bottom of the page, Enabled should be L and Disabled should be H.

On page 5A-34, add the following:

5A-33. MEMORY CARD INTERFACE ASSEMBLY (A6) TROUBLESHOOTING (Revision B and higher)

Note

There are two versions of the Memory Card Interface PCA used in the 2635A Hydra Data Bucket instrument. Earlier versions (Rev.A2 and below) are designed using a Fujitsu MF86301PF memory card controller IC (A6U1). Newer versions (Rev.B and higher) are designed using a Xilinx XC3030A-7PQ100C gate array as the memory card controller (A6U1). This section covers the Rev.B and higher. See section 5A-26 for troubleshooting information on Rev.A2 and below.

5A-34. Power-Up Problems

The following discussion identifies probable fault areas if the installation of a Memory Card Interface Assembly PCA causes power-up failure for the instrument. The problem is probably a short on A6P2; the Microprocessor on the Main Assembly is prevented from accessing Flash Memory and NVRAM correctly. Make the following checks:

- First check for a GND-to-VCC short on the Memory Card Interface Assembly PCA.
- There may also be a short between an interface signal and VCC, GND, or another interface signal. Check signals D8 .. D15, A1 .. A4, XRDU*, XWRU*, MCARD*, XSCLK, DTACK*, MCINT*, and RESET*.
- The short may be due to a CMOS input that has been damaged due to static discharge; the short is then detectable only when the circuit is powered up. Use an oscilloscope to check activity on each of the interface signals. Verify that signals are able to transition normally between 0 and 5.0V dc (VCC).

5A-35. FAILURE TO DETECT MEMORY CARD INTERFACE PC

Proper detection of the Memory Card Interface depends on the FPGA (A6U1) being properly configured at power-up. Proper FPGA configuration is indicated by a low to high transition on A6U1-80 shortly after power-up. Normally A6U1-80 should be high before RESET* (A6U1-78) goes high. If the Memory Card Interface is not installed properly, an "ERROR d" is displayed by the Microprocessor during power-up. The Microprocessor checks for the presence of the Memory Card Interface by attempting to read one of the registers in the Memory Card Controller (A6U1). If A6U1-58 fails to drive the DTACK* signal low during the read access, the Microprocessor will abort the memory cycle and report the Memory Card Interface as being not installed.

Verify the RESET*, XMCARD*, XRDU*, XSCLK, and DTACK* signals on the Memory Card Interface. RESET* (A6U1-78) must be high. Using a storage oscilloscope, verify that DTACK* (A6U1-58) goes low while XMCARD* (A6U1-49) is low for the first read memory cycle to the Memory Card Controller (A6U1) during instrument power-up. It may be necessary to cycle the power on the instrument several times to verify this operation.

5A-36. FAILURE TO DETECT INSERTION OF MEMORY CARD

When a Memory Card is inserted into the Memory Card Interface, the card detect signals (CD1 and CD2; A6U1-19 and A6U1-21) are driven low. Verify that the Memory Card Controller detects this and interrupts the Microprocessor (A1U1) by driving the MCINT* signal (A6U1-60) low. Failure to generate the interrupt may be due to problems with the data bus (D8..D15), the address bus (A1..A4), or one of the control signals (XSCLK, XMCARD*, XWRU*, XRDU*, and RESET*). Consult the schematics found in Section 8 of this manual and verify these interconnections. Consider the ribbon cable that connects the Main Assembly (A1) to the Memory Card Interface Assembly (A6) as a possible source of the problem as well. It may be necessary to repeatedly insert and remove the card to observe the behavior of these signals.

5A-37. FAILURE TO POWER CARD / ILLUMINATE THE BUSY LED

When a Memory Card is properly inserted and then detected by the Microprocessor (A1U1), the Memory Card should be powered up and the BUSY LED should be illuminated for a short period of time. If the BUSY LED is not visibly illuminated when the card is inserted, verify the following things using a storage oscilloscope. Verify that the gate of transistor A6Q1 is driven low by A6U1-26 (check both ends of resistor A6R13). When the gate of A6Q1 is near 0 volts dc, the drain of transistor (A6Q1-5 through A6Q1-8) should be near 5 volts dc.

Approximately 50 milliseconds after the transistor drain pins (A6Q1-5 through A6Q1-8) go to about 5 volts dc, the BUSY LED should be turned on by A6U1-25 going low to sink current through the LED (A6DS1) and current limiting resistor (A6R10). When the Microprocessor (A1U1) is done accessing data on the memory card, A6U1-25 and A6U1-26 will both go high again to turn off the BUSY LED and the card power supply. If the 50 millisecond delay between the memory card power being turned on and the BUSY LED being turned on may be extended up to a total of 250 milliseconds if the RDY/BSY signal (A6U1-23) is being held low by the memory card.

5A-38. FAILURE TO ILLUMINATE THE BATTERY LED

The yellow BATTERY LED is controlled by a Memory Card Controller output (A6U1-24). The Microprocessor checks the BVD1 and BVD2 outputs (A6U1-18 and A6U1-20 respectively) from the memory card about 50 milliseconds after it is powered up. The BATTERY LED is turned on by A6U1-24 going low to sink current through the LED (A6DS2) and current limiting resistor (A6R11).

Verify that the BATTERY LED state matches the state of the BVD1 and BVD2 signals as shown in the following table (H = 5 volts dc, L = 0 volts dc).

BATTERY LED	BVD1	BVD2
OFF	H	H
ON	H	L
ON	L	H
ON	L	L

5A-39. FAILURE TO WRITE TO MEMORY CARD

The installed memory card controls the state of the write protect (WP) signal that is an input to the Memory Card Controller (A6U1-22). This signal must be near 0 volts dc when the memory card is powered up and any operation requiring write access to the memory card is done. Verify that the state of the WP signal (A6U1-22) correctly follows the state of the write protect switch on the memory card as indicated in the following table (H = 5 volts dc, L = 0 volts dc).

Write Protect	WP (A6U1-22)
Enabled	L
Disabled	H

If the problem with the interface has not been isolated yet, the problem is probably in the card address (CA<0> .. CA<25>, REG*), card data (CD<0> .. CD<7>), and control signals (CE1*, CRD*, CWR*). The card data (CD<0> .. CD<7>) signals each go through a series termination resistor (Z2) so verify these series resistances. The control signals (CE1*, CRD*, CWR*) each go from the Memory Card Controller (A6U1) through an analog switch (A6U2) as they go to the Memory Card Connector (A6P1), so verify that each control signal functions properly. The card read (CRD*) and card write (CWR*) signals must go low for read and write cycles respectively. The following table describes the memory card access modes to "attribute" memory (only read accesses are done by the instrument).

Memory Card Access Modes

Transfer Mode	REG*	CE1*	CRD*	CWR*	Data Direction
No Operation	x	H	H	H	
Attribute Byte Read	L	L	L	H	CD -> D
Common Byte Read	H	L	L	H	CD -> D
Common Byte Write	H	L	H	L	D -> CD

5A-40. WRITE / READ MEMORY CARD TEST (DESTRUCTIVE)

The instrument has a special computer interface command that may be used gain diagnostic information about what is failing to function correctly in the Memory Card Interface.

WARNING

USE OF THE FOLLOWING COMMAND WILL DESTROY ANY DATA STORED ON THE MEMORY CARD THAT IS INSTALLED IN THE INSTRUMENT. AFTER COMPLETION OF THE TROUBLESHOOTING AND REPAIR OF THE MEMORY CARD INTERFACE, THE MEMORY CARD USED MUST BE FORMATTED AGAIN BEFORE IT MAY BE USED AGAIN FOR DATA STORAGE.

To make use of this command, connect a terminal or computer to the RS-232 interface and set the instrument communication parameters as follows:

- Press SHIFT and then LIST(COMM).
- With 'BAUd' displayed, use the UP or DOWN arrow key to select the desired baud rate. Then press ENTER.
- With 'PAR' (parity) displayed, use the UP or DOWN arrow key to select the parity. Then press ENTER.
- With 'CtS' (Clear to Send) displayed, use the UP or DOWN arrow key to select 'OFF'. Then press ENTER.
- With 'ECHO' displayed, use the UP or DOWN arrow key to select 'ON'. Then press ENTER. Communications setup for Hydra is now complete.

Assuming that the RS-232 interface is functional, send a carriage return or line feed character to the instrument and it should send back a prompt. With a Static RAM memory card installed in the instrument, send the following command followed by a carriage return or line feed:

MCARD_DESTRUCTIVE_TEST? <size> where the <size> parameter is the number of kbytes (1024 bytes) of the card to test. Use <size> = 256 for a 256 kbyte card and <size> = 1024 for a 1 Mbyte card.<end>

This command writes data to the memory card and then reads and compares the data to the pattern that was written. A maximum of twenty lines of output will be generated, but all locations on the card are sequentially written and then read. The messages output by this command are summarized below:

```
MEMORY CARD IS NOT INSERTED!
```

The Memory Card Controller doesn't recognize that the memory card is inserted in connector A6P1. Verify that A6U1-19 and A6U1-21 are both near 0 volts dc.

```
MEMORY CARD IS WRITE PROTECTED!
```

The Memory Card Controller is indicating that the memory card is write protected. Verify that the switch on the rear edge of the memory card is in the proper position and that A6U1-22 is near 0 volts dc when the memory card is powered up.

```
MEMORY CARD TEST PASSED.
```

The memory card test passed without detecting any errors.

```
ADDRESS 0x000000: DATA WAS 0x14, EXPECTED 0xC9
ADDRESS 0x000001: DATA WAS 0x3D, EXPECTED 0x2D
ADDRESS 0x000002: DATA WAS 0xAB, EXPECTED 0xBD
```

These are typical errors indicating in hexadecimal the address, the data that was read from the card and the data that was expected. It may be possible to get some indication of which address or data signals to probe with an oscilloscope to determine where the fault is.

When probing signals to detect activity, it may be useful to change the <size> parameter to be 16384 so that it will attempt to test the card as if it is a 16 Mbyte memory card. This guarantees that error messages will be output, but it will take longer to complete the test thus allowing more time to probe signals before having to send the memory card test command again.

On page 6-36, Table 6-10, make the following changes (rev.B pca's and higher only):

CHANGE: R1,13..2
TO: R13..1

CHANGE: R3,4..2
TO: R1,3,4,8..4

DELETE: R8,9..............

CHANGE: R10,11..2
TO: R6,10,11..3

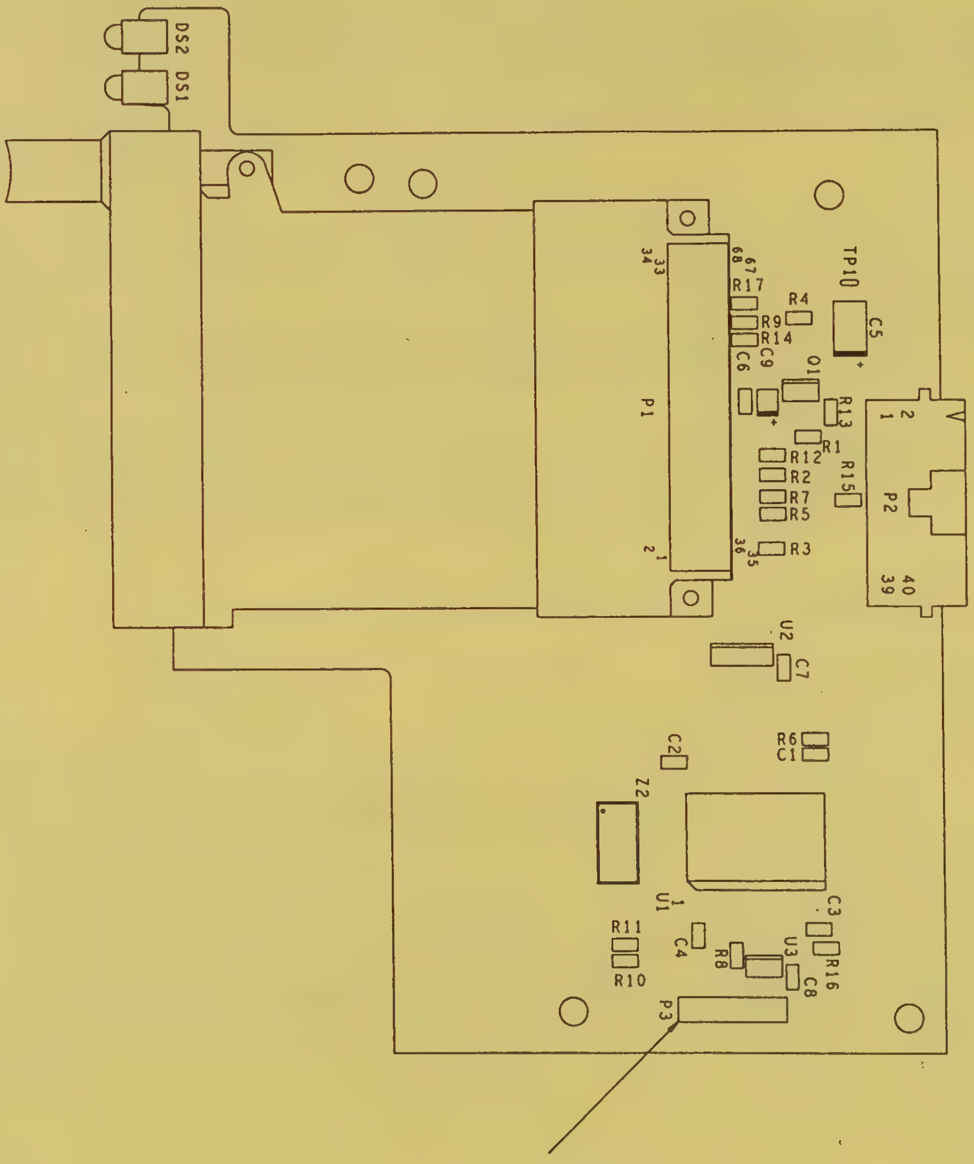
CHANGE: U1 | ....
TO: U1|IC,PROG GATE ARRAY, 3000 G, 70 MHZ,PQFP | 601275 | 89536 | 601275 | 1

CHANGE: U3 | ....
TO: U3 | IC,EPROM, 36KBIT SERIAL CONFIG,OTP,S08 | 601267 | 89536 | 601267 | 1

CHANGE: Z2,3..2
TO: Z2..1

On pages 6-37 and 8-35/8-36, replace the component location drawing (2635A-1606) with Figure K.

On page 8-35/8-36, replace the schematic (2635A-1006) with Figure L.


DS2
DS1
P1
33
34
67
68
R17
R4
R9
R14
C9
C6
TP10
C5
Q1
R13
R1
R12
R2
R7
R5
R15
R3
35
36
1
2
P2
2
1
40
39
U2
C7
R6
C1
C2
Z2
U1
1
C3
R11
R10
C4
R8
U3
R16
C8
P3

Not Installed

2635A-1606

Figure K. A6 Memory Card I/F PCA (Rev.B) Component Locations

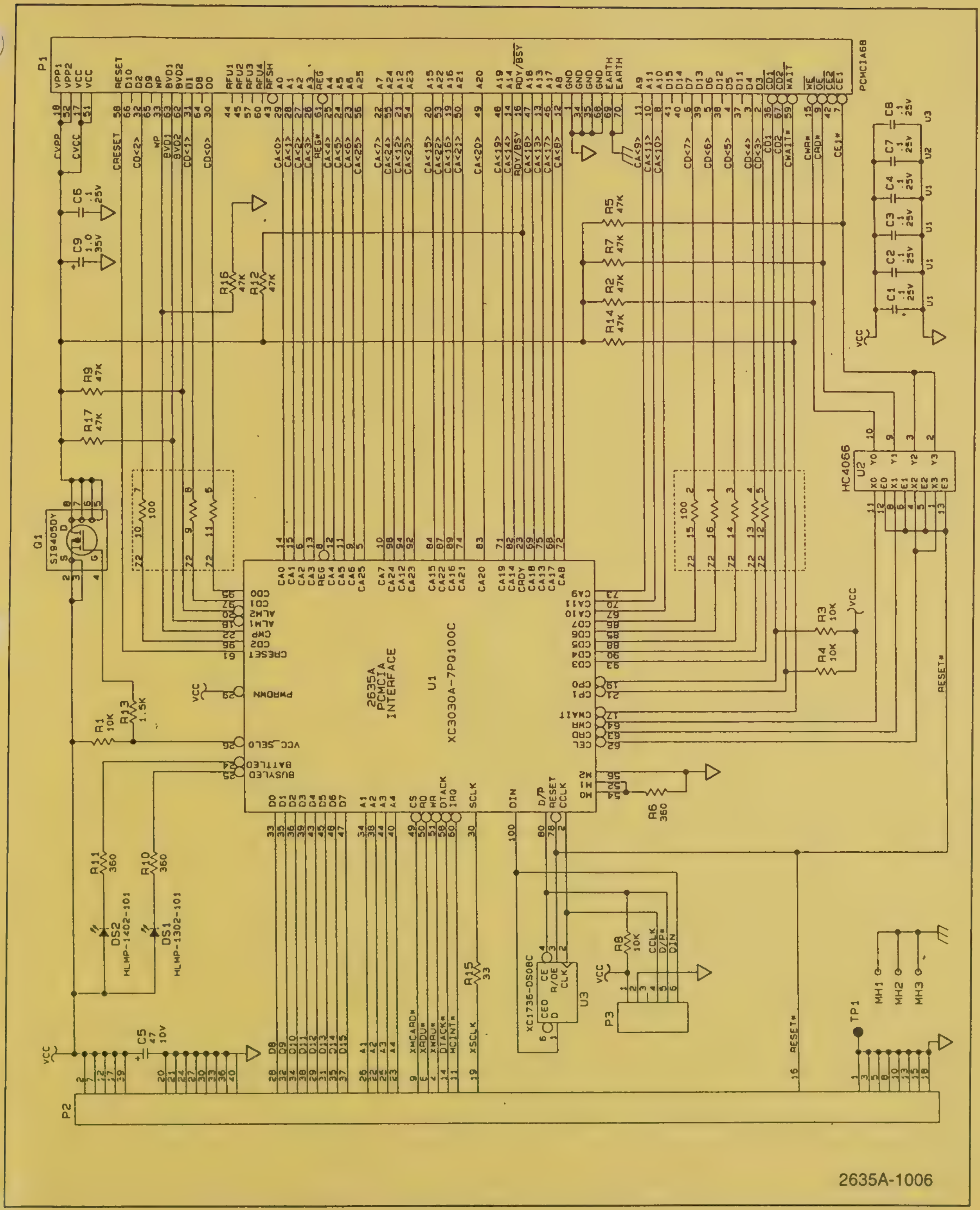

P1
PCMCIA68
P2
P3
U1
2635A PCMCIA INTERFACE
XC3030A-7PQ100C
U2
HC4066
U3
XC1736-DS08C
Q1
SI9405DY
DS1
HLMP-1302-101
DS2
HLMP-1402-101
R1 10K
R2 47K
R3 10K
R4 10K
R5 47K
R6 360
R7 47K
R8 10K
R9 47K
R10 360
R11 360
R12 47K
R13 1.5K
R14 47K
R15 33
R16 47K
R17 47K
C1 .1 25V
C2 .1 25V
C3 .1 25V
C4 .1 25V
C5 47 10V
C6 .1 25V
C7 .1 25V
C8 .1 25V
C9 1.0 35V
VCC
RESET*
TP1
MH1
MH2
MH3
2635A-1006

Figure L. A6 Memory Card I/F PCA (Rev.B) Schematic